Lifetime Prediction Model for Analog Devices Based on Drain Conductance Degradation due to Hot Carrier Injection

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Abstract

MOSFET degradation due to hot carrier injection is the most important reliability issue in realizing submicron ultra-large scaled integrated circuits. This degradation has been widely studied and lifetime simulators have also been developed for digital circuit operation [1]-[2]. On the other hand, the degradation of analog device parameters such as drain conductance due to hot carrier injection are not clearly understood and modeled. In this paper, we propose, for the first time, a physical model of analog drain conductance, g_d degradation based on mobility reduction due to hot carrier generated interface states and show a reliability design guideline for analog devices.

Fig. 1 shows gain degradation of a single MOSFET amplifier with a constant current source (Fig. 2) as a function of DC stress time. Since the gain of the amplifier is given by gain=g_m/g_d, g_m and g_d were also measured and $dg_m=|g_{mo}-g_m|$ and $dg_d=|g_{do}-g_d|$ were plotted in Fig. 1. It has been found that the main cause of the gain degradation was g_d degradation rather than g_m degradation.

Our model of g_d degradation is based on the gradual channel approximation (GCA) and mobility reduction due to interface states generated by hot carrier injection [3]. When distribution of interface states generated by hot carrier injection is assumed to be a step function over the damaged region, the generated interface state density, N_{its}, is given by [4]

$$N_{its}=(L_{eff}/L_{dmg})((g_{mo}-g_m)/g_m)/\alpha \qquad (1)$$

where L_{eff} is the effective gate length, L_{dmg} the length of the damaged region and α the mobility reduction factor. In the saturation region, a depletion region is formed between the pinch-off point and the drain as shown in Fig. 3. The drain current equation in the saturation region is given by

$$\int_0^{L_{effx}}(\mu_o I_d/\mu L_{effx})dy = (\mu_o W/L_{effx})\int_0^{V_{dsat}} C_{ox}(V_{gs}-V_{to}-V(y))dV-(\mu_o W/L_{effx})\int_0^{V_{dsat}} qN_{it}(y)dV \qquad (2)$$

where μ_o and μ are the mobility in non-damaged and damaged region respectively, W the channel width, and L_{effx} the effective channel length in the saturation region. Integrating (2) from the source to the pinch-off point and differentiating with respect to V_{ds} yield

$$g_d \cong (1+\alpha N_{its})g_{do} \qquad (3)$$

when $L_{dmgx} << L_{effx}$. By substituting (1) into (3), the basic equation of g_d degradation is then obtained as

$$(g_d-g_{do})/g_{do}=(L_{eff}/L_{dmg})((g_{mo}-g_m)/g_m) \qquad (4).$$

By using (4), g_d degradation can be calculated from gm degradation.

The substrate current, I_{sub}, is the best monitor parameter of device degradation due to hot carrier injection and the g_m degradation lifetime, τ_{gm}, follows a log-log relationship with I_{sub} [6] as

$$\log(\tau_{gm})=C_1\log(I_{sub})+C_2 \qquad (5)$$

where C_1 and C_2 are constants. Using (4), (5), and the power law relationship between $(g_{mo}-g_m)/g_{mo}$ and stress time, the g_d degradation lifetime, τ_{gd}, is given by

$$\log(\tau_{gd}) = C_1\log(I_{sub})+C_2+(1/n)(\log(\beta L_{dmg}/(L_{eff}+\beta L_{dmg}))+1) \qquad (6)$$

where β is the degradation ratio of g_d, $(g_d-g_{do})/g_d$, for the lifetime definition and n the coefficient of the power law relationship ($\cong$0.5). Fig. 4 shows measured and calculated values of τ_{gd} for L=1.0μm and 2.0μm as a function of I_{sub}. The calculated τ_{gd} fits the measured τ_{gd} well. Fig. 5 shows acceptable values of L_{eff} which permit 10 year operation based on I_{sub} values. These curves are then guidelines for the reliable design of analog devices.

In conclusion, we propose, for the first time, the physical model of drain conductance, g_d, degradation due to hot carrier injection. The relationship between the g_d degradation lifetime and substrate current is also reported. This model is then very useful for lifetime prediction of analog devices.

References

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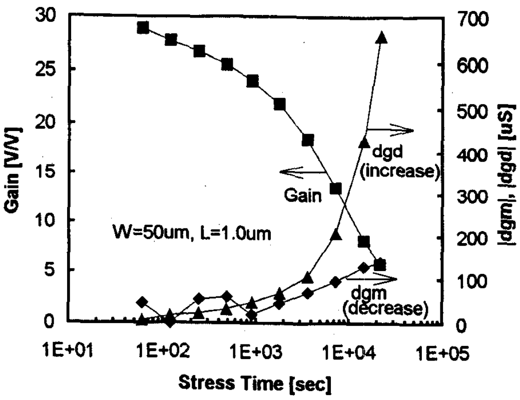

Fig. 1 Gain, g_m, and g_d degradation of a single MOSFET amplifier.

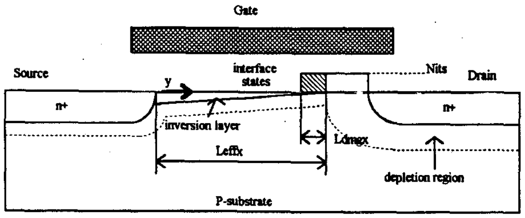

Fig. 3 Schematic cross-section of the damaged MOSFET in the saturation region.

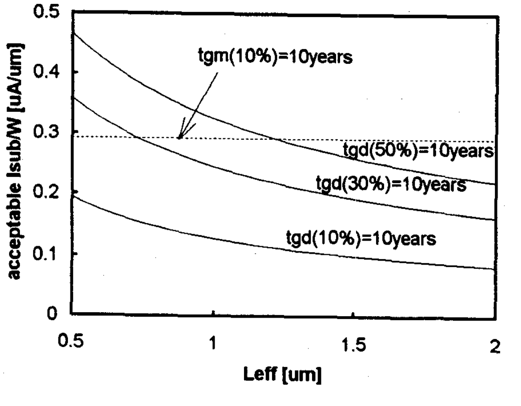

Fig. 5 Acceptable values of L_{eff} for 10 year operation.

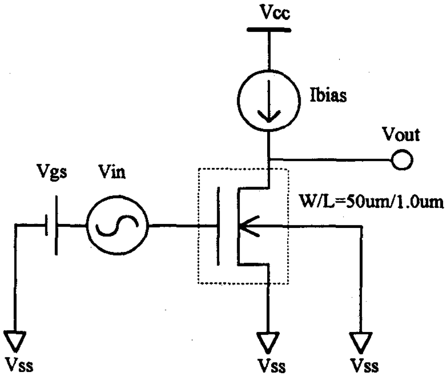

Fig. 2 Circuit diagram of the single MOSFET amplifier.

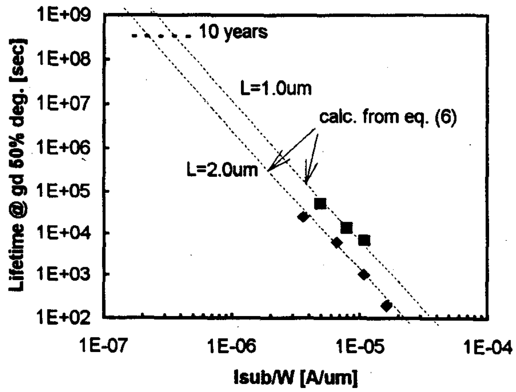

Fig. 4 Dependence of τ_{gd} on I_{sub}.