An Analytical Delayed-Turn-off Model for Buried-Channel PMOS Devices Operating at $77K$

J. H. Sim and J. B. Kuo
Rm. 526, Dept. of Electrical Eng., National Taiwan University
Roosevelt Rd. Sec. 4 #1, Taipei, Taiwan 107
FAX:886-2-363-8247, Telephone:886-2-363-5251
E-mail:kuojb@leibniz.ee.ntu.edu.tw

Abstract

Current circuit simulation programs such as SPICE do not provide a sufficient low-temperature device model for buried-channel PMOS devices biased in the delayed-turn-off region [1]. This paper presents a closed-form analytical PMOS delayed-turn-off model suitable for simulation of circuits with PMOS devices operating at the liquid nitrogen temperature. As compared to the low-temperature PISCES [2]-[4] results, the closed-form analytical PMOS delayed-turn-off model provides a much better accuracy for simulation of circuits operating at $77K$.

Summary

Recently, low temperature operation of CMOS circuits has been receiving substantial attention owing to advantages in speed performance, latchup immunity, and relaxed scaling restrictions[5]. However, the available circuit simulation programs such as SPICE do not provide accurate models for CMOS devices operating at $77K$. Especially, the delayed-turn-off phenomenon of the PMOS device with a counter-doped channel, operating at $77K$, is not included in the SPICE model. Although, device-level models describing the PMOS delayed-turn-off behavior has been reported [1] using iterative numerical methods, it is not suitable for circuit simulation. In this paper, a closed-form analytical delayed-turn-off model of the PMOS device operating at $77K$ suitable for SPICE circuit simulation is described.

Fig. 1(a) shows the cross section of a PMOS device based on a $1.2\mu m$ CMOS technology used in the study. The PMOS device has a gate oxide thickness of $250\mathring{A}$. Fig. 1(b) shows the vertical doping profile in the center of the channel with a junction depth of $0.2\mu m$. As shown in Fig. 2, based on the current SPICE model, the subthreshold IV characteristics of the PMOS device at $77K$ is very different from the PISCES results[3][4], where incomplete ionization, bandgap narrowing, concentration and E-field dependent mobilities, Shockley-Read-Hall and Auger recombinations with concentration dependent lifetimes have been included [4]. As shown in Fig. 3, at $77K$, in the PMOS device biased in the delayed-turn-off region, the potential distribution indicates a valley at the peak of the implanted channel, which implies a zero electric field. Between the peak of the implanted channel and the silicon surface, the potential difference is large for the device biased in the strong and conventional weak inversion regions. However, in the delayed-turn-off region, the voltage difference between the silicon surface and the potential valley is small, where the freeze-out effects are important. As shown in Fig. 4, a closed-form analytical delayed-turn-off model has been successfully created by solving Poisson's equation with incomplete ionization around the potential valley for the regions above and below the potential valley. As shown in Fig. 5, a good agreement between the analytical model and the PISCES results can be found in the potential distribution for the device operating in the delayed-turn-off region. Fig. 6 shows the subthreshold IV characteristics of the PMOS device with a channel implant depth of $0.2\mu m$ for three peak concentrations($5, 7, 9 \times 10^{16} cm^{-3}$) based on the analytical and PISCES results. For a higher peak concentration, the PMOS device indicates a longer delayed-turn-off interval. The analytical model demonstrates a very close fit to the 2D results in the delayed-turn-off region. Fig. 7(a) shows the subthreshold slope ($n \equiv \frac{\partial V_G}{\partial \Psi_{ch}}$) of the PMOS device with a channel implant depth of $0.2\mu m$ for three peak concentrations. In the delayed-turn-off region, as the gate voltage moves toward the positive direction, the slope is decreasing. As it reaches the weak inversion region, the slope is at minimum. Among three cases, the delayed-turn-off slope is the largest for the $9 \times 10^{16} cm^{-3}$ case, which shows the strongest delayed-turn-off phenomenon. For a peak concentration of less than $5 \times 10^{16} cm^{-3}$, the delayed-turn-off behavior almost diminishes. As shown in Fig. 7(b), in addition to the oxide capacitance, the equivalent capacitance model is composed of two depletion capacitances (C_{D1},C_{D2}) and another capacitance C_M accounting for the mobile charge in the channel. As the gate voltage is near the conventional weak inversion region, the subthreshold slope of the analytical model results is approaching $n = 1 + C_{D2}(\frac{1}{C_{D1}} + \frac{1}{C_{OX}})$, as for the room temperature case [6] since freeze-out effect is negligible. Figs. 8(a) & (b) show the interval of V_G where delayed-turn-off exists and the delayed-turn-off slope vs. the junction depth of the channel implant for various peak concentrations and gate oxide thicknesses. With a deeper channel implant, the device indicates a stronger delayed-turn-off behavior. On the other hand, with a thinner gate oxide, the device shows a less delayed-turn-off phenomenon owing to a more influence from the gate. In conclusion, a closed-form analytical delayed-turn-off model of a PMOS device operating at $77K$ has been successfully created. Compared to low-temperature PISCES results, a much better match can be identified using the analytical model, which is suitable for simulation of circuits with PMOS devices operating at $77K$.

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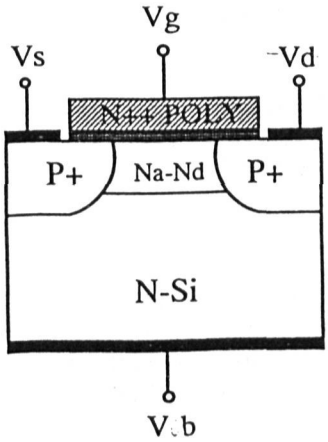


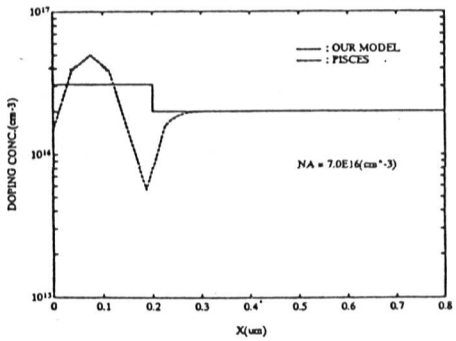


Fig.1(a) Cross section of the PMOS device under study.

(b) Doping profile

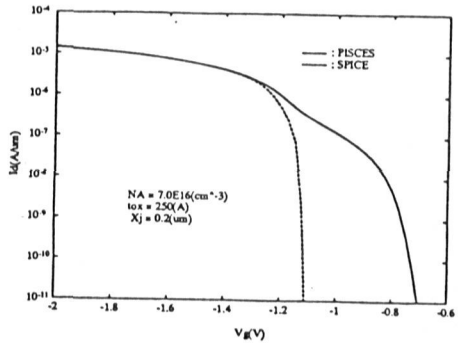


Fig.2 The subthreshold IV characteristics of the PMOS device at $77K$ based on the SPICE and PISCES.

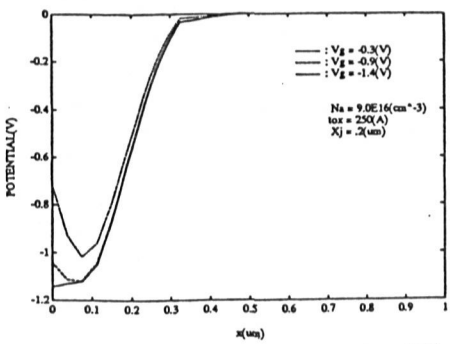


Fig. 3 Potential distributions in the PMOS device at $77K$.

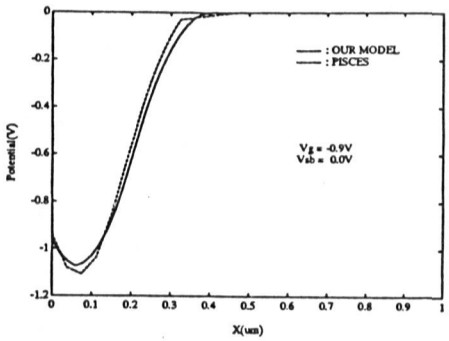


Fig. 5 Potential distribution in the PMOS device at $77K$ using the analytical model and the PISCES results.

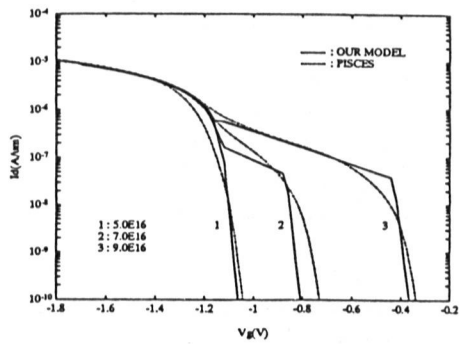
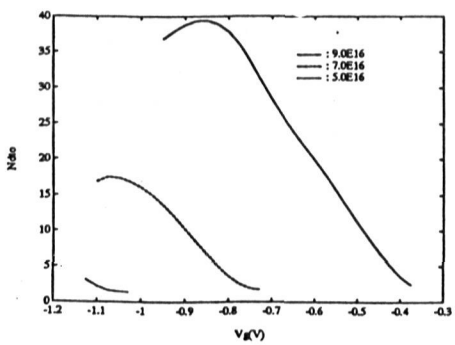


Fig. 6 Subthreshold IV characteristics of the PMOS device using the analytical model and the PISCES results.

1. $V_G = V_G(\Psi_{ch} = \Psi_{dto}) + \frac{\partial V_G}{\partial \Psi_{ch}} \Delta \Psi_{ch}$
2. $\Psi_{dto} = -(|\phi_{fp}| + |\phi_{fn}|)$
3. $n_{dto} = 1 + \frac{1}{1+(N_a-N_d)^\beta + r - 1}\left[\frac{\theta}{1+(N_a-N_d)^\beta}\left(n_p e^{-\Psi_{dto}/\frac{kT}{q}} + \frac{N_a K e^{-\Psi_{dto}/\frac{kT}{q}}}{1+Ke^{-\Psi_{dto}/\frac{kT}{q}}}\right) + \frac{C_{ox}}{2\varepsilon_{si}} r^2 (V_G - V_{FB} - \Psi_{dto} - \frac{kT}{q})\beta(\Psi_{dto})\right]$
4. $\theta = \frac{1}{C_{ox}} \sqrt{\frac{q\varepsilon_{si}}{2}} \frac{1}{U(s,\Psi_{dto})}$
5. $r = \left(\frac{C_{ox}}{2\varepsilon_{si}}(x_{ch} - x_e) + 1\right)^{-1}$
6. $K = 4e^{(E_A - E_V - \frac{E_g}{2} - q\phi_{fn})/kT}$
7. $U(\psi_{ch} = \Psi_{dto}) = \sqrt{(N_a - N_d)s - \frac{kT}{q} n_p e^{-\Psi_{dto}/\frac{kT}{q}} - N_a \frac{kT}{q}(1 + Ke^{-\Psi_{dto}/\frac{kT}{q}})}$
8. $n_p = \frac{n_i}{\xi(\frac{E_F - E_V}{kT})} e^{q\phi_{fn}/kT/q}, \xi(x) = 1 + 0.2709e^{(-0.8173x)}$
9. $\beta(\Psi_{ch}) = \frac{\partial \varepsilon_{ch}}{\partial \Psi_{ch}} - \frac{\partial \varepsilon_s}{\partial \Psi_{ch}}$

Fig. 4 Important equations in the analytical delayed-turn-off model.



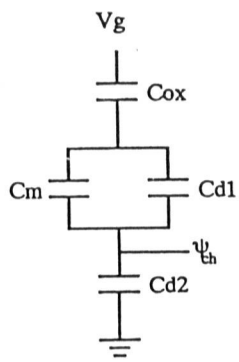
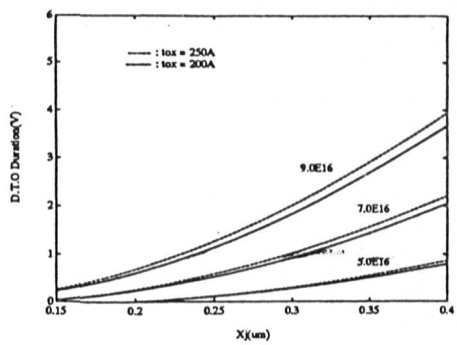


Fig. 7 (a)Subthreshold slope of the PMOS device using the analytical model and the PISCES results.
(b)Equivalent capacitance model



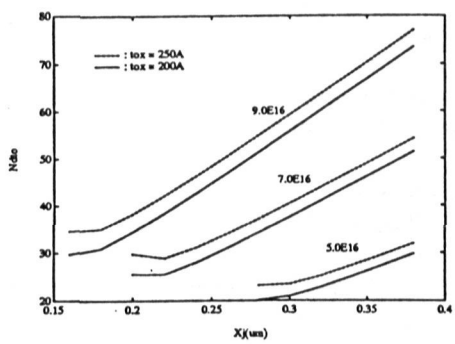


Fig. 8 (a)The voltage interval where delayed-turn-off exists
(b) n_{dto} vs. the junction depth of the channel implant