

(7B-2)

A new monitor to predict hot-carrier damage of PMOSTs.

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Hot-carrier degradation of PMOS transistors is worst at low gate voltages when electrons are injected and trapped in the gate oxide near the drain. This negative oxide charge causes an extension of the drain by an inversion layer, reducing the effective length [1,2]. Although this channel-shortening mechanism is well known, the threshold voltage or the transconductance are still used to characterize the amount of damage [2,3,4]. We propose to use the channel shortening, normalized on the oxide thickness ($\Delta L_{\text{eff}}/t_{\text{ox}}$) to characterize the damage. The normalization is motivated by the larger oxide capacitance of a thinner oxide, requiring more oxide charge to form the inversion layer that extends the drain.

The relation between the effective length and the threshold voltage (in saturation) appears to be identical for stressed and unstressed transistors (figure 1) but an extra series resistance, proportional to ΔL_{eff} , is present after degradation (figure 2). In both figures, each curve consists of characterizations made before (\diamond) and during (line) a hot-carrier stress at low gate voltage. The different curves are measured on transistors from one wafer with different initial lengths and degraded under various stress conditions. According to figures 1 and 2, a degraded (at low V_G) PMOS transistor behaves like a shorter transistor with an extra series resistance at the drain side. Minimalization of the threshold voltage shift during degradation may be achieved by optimizing short-channel effects: transistors with an optimized $L_{\text{eff}} - V_T$ relation will show less threshold voltage shift for the same channel shortening.

Figure 3 shows that the (measured) damage after 0.1 s of degradation correlates with the (measured) damage after 5000 s of degradation. The different symbols are for different transistor types with gate oxide thickness ranging from 25 nm to 8 nm with conventional drain or LDD and with either p⁺- or n⁺-polysilicon gate materials. The measurements for all transistor types show the same correlation, thus proving that $\Delta L_{\text{eff}}/t_{\text{ox}}$ is the correct measure for the amount of damage when comparing different transistor types. Note that we measured for each transistor type in figure 3 transistors of different lengths, degraded at different drain voltages and at gate voltages that cause negative charge injection ($0 > V_G > V_D/3$).

Figure 4 shows that the (measured) damages after 0.1 s and 100 s have the same relation as the (measured) damages after 10 s and 10000 s of degradation. The relation appears to be valid for a factor of 1000 extrapolation in time, independent of the total duration. These two sets in figure 4 make plausible that figure 3, relating the damage after 0.1 s with the damage after 5000 s may also be used to predict the degradation after 10 years when starting from measurements after 2 hours of degradation (extrapolating over the same factor of 50000).

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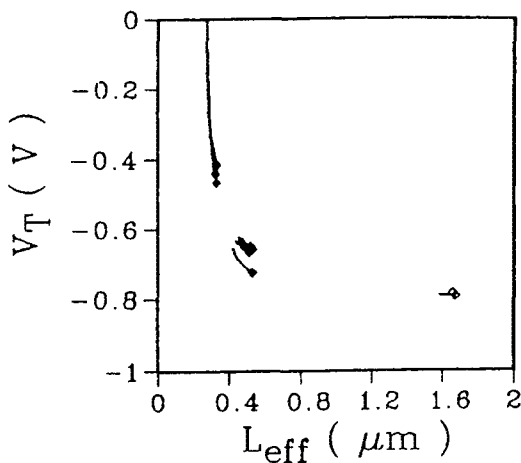


figure 1. Relation between the effective length and the threshold voltage before (\diamond) and during (line) degradation. Buried-channel transistors with 12.5 nm gate oxide thickness are degraded at $V_G = -1.5$ V with $-5 > V_D > -8$ V.

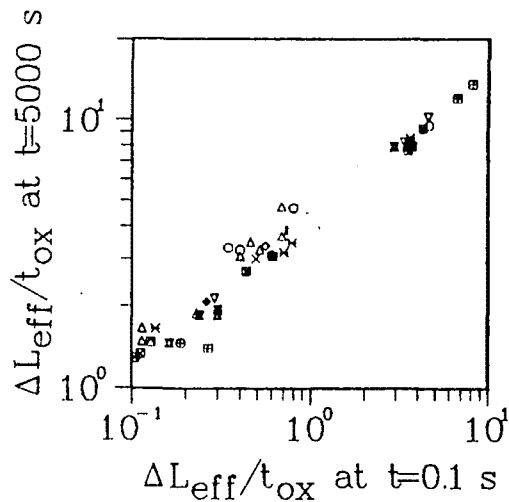


figure 3. Measured normalized channel shortening after 0.1 s of degradation plotted versus the measured normalized channel shortening after 5000 s. The different symbols are for different transistor types.

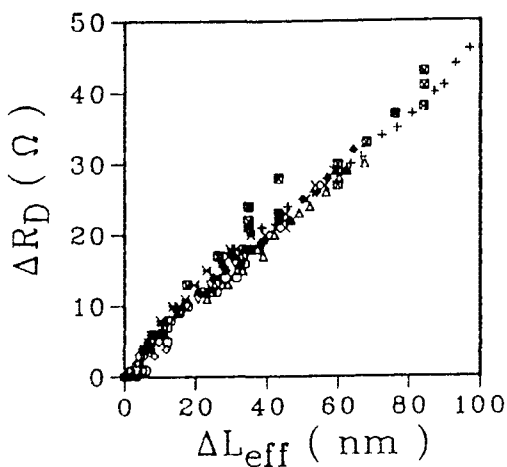


figure 2. Change in the series resistance of the drain versus the change in effective length for the experiments in figure 1. The transistor width is 10 μ m.

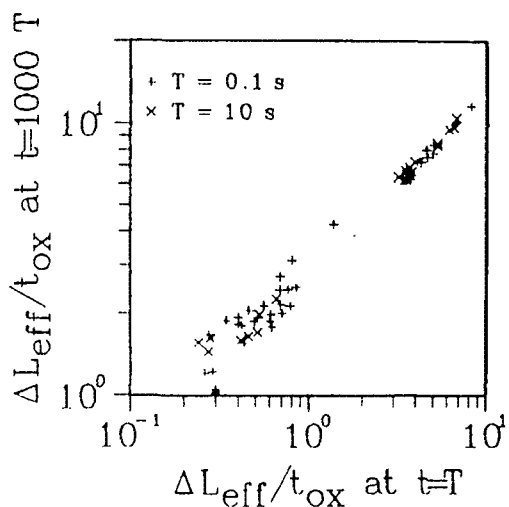


figure 4. Relation between the normalized channel shortening after 0.1 s and 100 s of degradation (+) and the same quantities after 10 s and 10000 s of stress (x).