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ANALYSIS OF PEDESTAL-COLLECTOR TRANSISTORS BY 2-D PROCESS AND DEVICE SIMULATION

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For an advanced bipolar transistor, the optimization of a base-collector doping profile is now a major concern. A highly doped collector is effective to improve cutoff frequency because it prevents a base stretching effect. However, it also increases C_{CB} and decrease BV_{CEO}. By using a newly developed 2-D process and device simulation system, we have analyzed selectively ion-implanted pedestal-collector transistors to investigate trade-off between device parameters and BV_{CEO}.

We have developed a 2-D process simulator "FIPS2", which includes the same epitaxial autodoping model as that of a 1-D process simulator FIPS [1]. FIPS2 is connected to a 2-D DC/AC bipolar device simulator "BIP2DAN". We have added an avalanche generation model to BIP2DAN in addition to the previously reported physical models [2].

Fig.1 shows the vertical doping profiles of analyzed transistors. The 2-D contour plots of impurity concentration in the collector region are shown in Fig.2. Fig.3 displays the schematic cross section of a transistor under study. Calculated device parameters and BV_{CEO} are listed in Table.1.

The base resistances and the base-collector capacitances show little difference among the pedestal-collector transistor cases. However, f_T and BV_{CEO} depend on the pedestal-collector doping profiles and there is a trade-off between these two figures. So far as the cutoff frequency is concerned, the 300-keV implantation is the best case, while it is the worst case for BV_{CEO}. Therefore, the pedestal-collector doping profile should be optimized carefully to obtain higher f_T and appropriate BV_{CEO}.

Acknowledgement

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References

[1] I.Namura et.al., JSAP Spring Conference Tech. Dig.(1987) 908 29a-G-1 (in Japanese)

[2] Y.Nagase et.al., NUPAD- II Tech. Dig.(1988) Nupad156

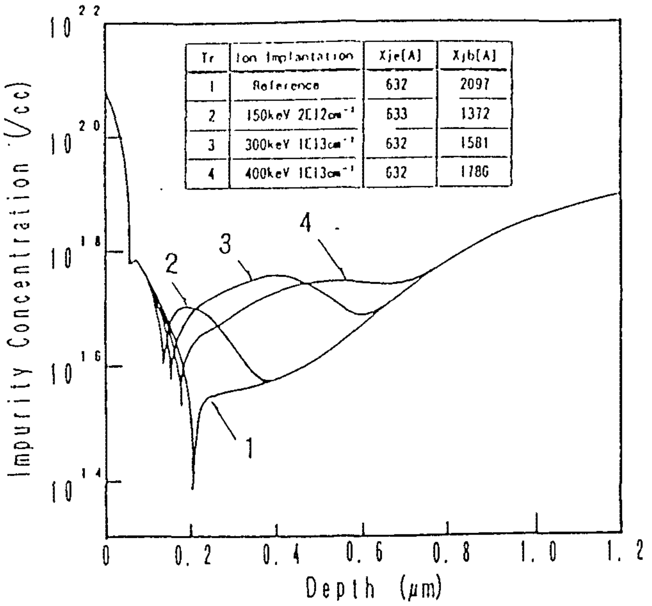

Fig. 1 Vertical doping profiles of analyzed transistors.

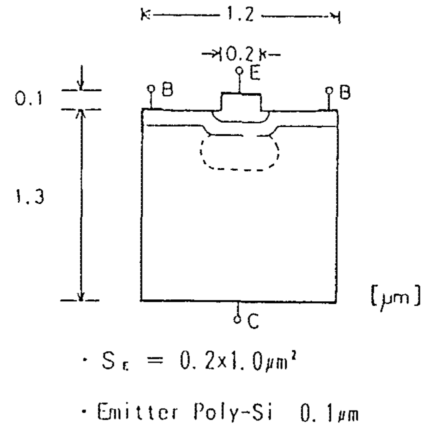

Fig. 3 Schematic cross section of a transistor under study.

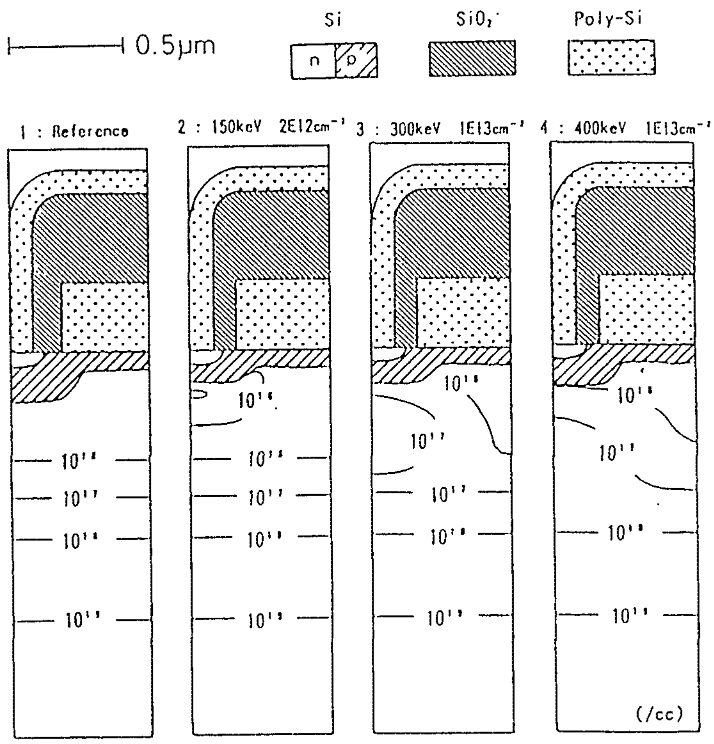

Fig. 2 Equi-contour lines corresponding to junctions and impurity concentration of the collector.

Tr	Ion Implantation	f_{Tmax} [GHz]	r_{bb}' [Ω]	C_{cb} [fF]	BV_{CEO} [V]
1	Reference	16.2	609.7	0.31	5.7
2	150keV 2E12cm^{-2}	22.0	707.9	0.58	2.2
3	300keV 1E13cm^{-2}	28.6	614.7	0.65	1.8
4	400keV 1E13cm^{-2}	24.0	600.5	0.52	2.7

Table 1 Calculated device parameters.