(4A-2)

# MONTE CARLO SIMULATION OF DEEP SUB-MICRON SI MOSFETs

K.Fukuda, S.Baba, and K.Nishi
OKI Electric Industry Co., Ltd.
550-1 Higashiasakawa, Hachioji, Tokyo 193,Japan
Phone:+81-426-63-1111, FAX:+81-426-66-7213

With the reduction of device size, various non-equilibrium transport effects have become more important in device characteristics which cannot be simulated by classical device simulators using drift-diffusion(DD) model. To analyze these effects, hydrodynamic(HD) and Monte Carlo(MC) models have been vigorously studied by many workers. Since carriers are treated as particles in the MC model, it is easy to compare physical models and to understand the results of the MC model. But it costs a lot of CPU time to simulate device structures including abrupt changes in impurity concentration like MOSFETs.

The analysis of deep sub-micron MOSFETs is performed by the MC simulator/1/ which treats only the channel region by the MC model to reduce the CPU time. To calculate the electric potential distribution in the device, carrier concentration calculated by particles of MC method is used in the channel region and carrier concentration calculated by the DD model is used in the source/drain regions. Impurity concentration is calculated by the 2-dimensional process simulator OPUS/2/, and the initial conditions of electric potential and carrier concentration are calculated by the 2-dimensional device simulator ODESA/3/.

Fig.1 shows the carrier energy in the channel region of nMOSFETs. Fig.2 shows the similar plot for pMOSFETs. The validity of the physical models is checked by comparing the simulated IV-characteristics with experimental data with various channel lengths. The effects of device scaling are investigated from various points of view such as surface potential distributions, energy distributions, and electric current paths. The actual LDD MOSFETs are used for the start point of scaling and are scaled into the deep sub-micron range (down to Leff=0.05um).

References:

/1/ K.Fukuda et al., presented at "1989 VLSI Process/Device Modeling Workshop",Osaka, 1989.
/2/ K.Nishi et al., IEEE Trans. on CAD, vol.CAD-8, pp.23, 1989.
/3/ J.Ueda et al., J. Inst. Elec. Commun. Eng. Japan, vol.J67-C, pp.825, 1984.

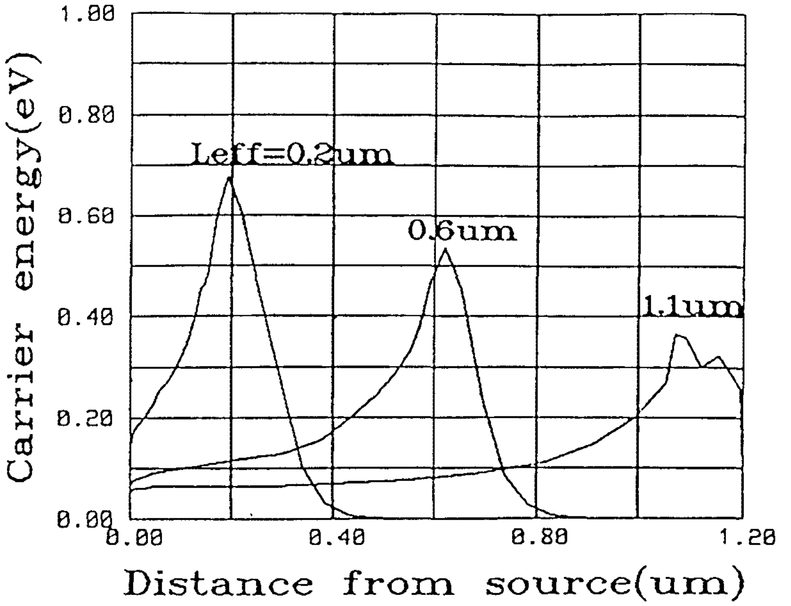


Fig.1 Carrier energy along the channel regions of LDD nMOSFETs. Total scattering rate is $10^{15}(sec^{-1})$. (Vd=Vg=5v, Vsub=-2v, Vs=0v).

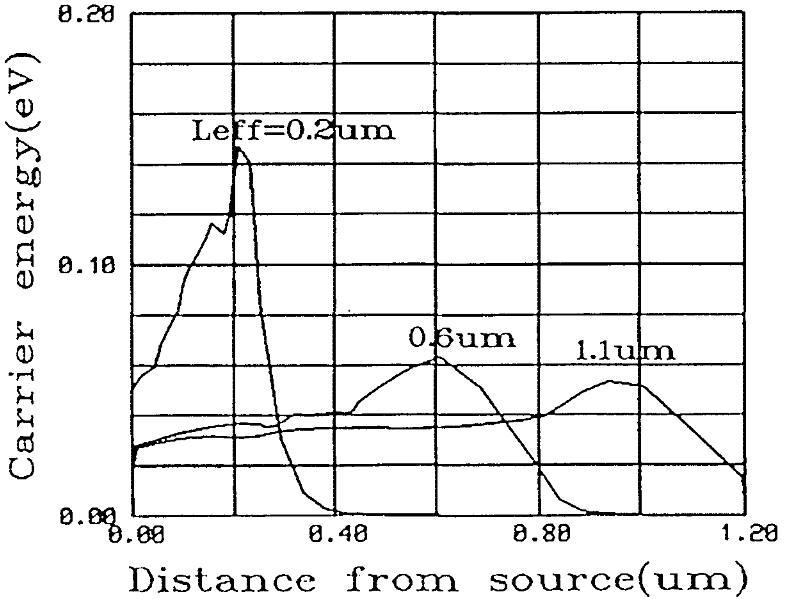


Fig.2 The similar plot to Fig.1 for LDD pMOSFETs. (Vd=Vg=-5v, Vsub=Vs=0v).