(7B-1)

ENERGY-MOMENTUM TRANSPORT COMPUTER SIMULATOR FOR VLSI DEVICE STRUCTURES

Savvas G. Chamberlain
James W. Roberts

Electrical and Computer Engineering Department
University of Waterloo,
Waterloo, Ontario, Canada, N2L 3G1
Tel: (519) 888-4598. Fax: (519) 746-6321

ABSTRACT

Application of the conventional drift-diffusion model to certain sub-micron devices may be inappropriate due to hot carrier effects. These may include localized velocity saturation overshoot and impact ionization. Silicon device models based on the conservation of carrier momentum and energy have been shown to model such effects more accurately. However, to date, these energy-momentum transport (EMT) based simulators have been limited in scope or designed for specific device application only. This paper describes the implementation of an EMT model [1] into the modular semiconductor device simulation tool CHORD [2]. The simulator fully couples energy-momentum transport equations for electrons and holes with the lattice heat equation in two space dimensions and time. Our EMT model is basically a hydrodynamics based formulation [1]. The EMT model is designed to be consistent with the general purpose nature of the CHORD simulation system [2] and thus can accommodate arbitrary device structures and bias conditions. A major strength in the CHORD system is that it allows for the addition of new models with minimal interface between the user and the simulator infrastructure. Passive elements such as resistors or capacitors can also be attached to a terminal of the device under test.

Using our EMT model we succesfully modeled small geometry MOSFET and CMOS devices including latchup. In this paper we shall describe our EMT computer model and also give some typical results on devices. The model and general expressions for carrier generation (GR), carrier energy scattering ($T_{n\,scat}$,$T_{p\,scat}$) and lattice heat loss/gain ($T_{l\,scat}$) have been developed and are listed below. In this abstract we also give a contour temperature plot of a short channel MOSFET device.

$$\nabla\cdot\mathbf{E} = p - n + N_D - N_A$$

$$\frac{\partial n}{\partial t} - \frac{1}{q}\nabla\cdot\mathbf{J}_n = GR$$

$$\frac{\partial p}{\partial t} + \frac{1}{q}\nabla\cdot\mathbf{J}_p = GR$$

$$\mathbf{J}_n = \mu_n\left(qn\mathbf{E} + k\nabla(nT_n)\right)$$

$$\mathbf{J}_p = \mu_p \left(qp\mathbf{E} - k\nabla(pT_p) \right)$$

$$\frac{\partial nT_n}{\partial t} - \frac{2}{3k}\mathbf{J}_n \cdot \mathbf{E} - \frac{5}{2q}\nabla \cdot kT_n\mathbf{J}_n - \frac{2}{3k}\nabla \cdot \kappa_n \nabla T_n = T_{n\,scat}$$

$$\frac{\partial pT_p}{\partial t} - \frac{2}{3k}\mathbf{J}_p \cdot \mathbf{E} + \frac{5}{2q}\nabla \cdot kT_n\mathbf{J}_p - \frac{2}{3k}\nabla \cdot \kappa_p \nabla T_p = T_{p\,scat}$$

$$\rho c_l \frac{\partial T_l}{\partial t} - \nabla \cdot \kappa_l \nabla T_l = T_{l\,scat}$$

$$GR = G_n + G_p - R_n - R_p + L_n - C_n$$

$$T_{n\,scat} = n\frac{T_l - T_n}{\tau_{wn}} - \frac{2}{3k}E_g G_n - T_n(C_n + R_n + R_p) + T_l(G_n + G_p + L_n)$$

$$T_{p\,scat} = p\frac{T_l - T_p}{\tau_{wp}} - \frac{2}{3k}E_g G_p - T_p(C_p + R_p + R_n) + T_l(G_n + G_p + L_p)$$

$$T_{l\,scat} = n\frac{T_n - T_l}{\tau_{wn}} + p\frac{T_p - T_l}{\tau_{wp}} + \frac{2}{3k}E_g(U + R_n + R_p) + T_n(C_n + R_n + R_p) + T_p(C_p + R_p + R_n)$$
$$- T_l(L_n + L_p + 2(G_n + G_p)) \ .$$

[1] J. W. Roberts and S. G. Chamberlain, "Energy-Momentum Transport Model for Small Geometry Silicon Device Simulation", *COMPEL, Inter. Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol. 9, no. 1, pp. 1-21, March 1990.

[2] J.R.F. McMacken and S.G. Chamberlain, "CHORD: A Modular Semiconductor Device Simulation Development Tool Incorporating External Network Models", *IEEE Trans. on Computer-Aided Design*, vol. 8, no. 8, pp. 826-836, 1989.

Figure 1: Electron temperature contour plot for an nMOS transistor with a 0.1 μm channel length. Contours represent a change in temperature of 100K. Bias voltages are shown on the figure.