

## Application of Matrix Transformation Methods in Three-Dimensional Device Simulation

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In semiconductor device simulation, both Gummel and Newton methods are used to solve the nonlinearly coupled system of Poisson and current continuity equation(s)[1]. In comparing with Gummel's method, Newton's method has the advantage of superlinear convergence when the solution is near. To avoid the large memory penalty associated with using a full Newton method, block-Newton methods have been proposed. However, performance has been reported to be not competitive with the combination of Gummel and full Newton methods[2]. Encouraged by the success of the Modified-Singular Perturbation (MSP) scheme in speeding up the convergence of the Gummel method for a 3-D one-carrier device solver, [3] we have now applied both the MSP and the Alternate-Block-Factorization (ABF)[4] schemes in conjunction with the block-Newton method. With a block matrix transformation, the system of equations for a new update is as follows :

$$A x = -F \equiv \begin{bmatrix} A_{\psi\psi} & D_{\psi\phi_s} \\ A_{\phi_s\psi} & A_{\phi_s\phi_s} \end{bmatrix} \begin{bmatrix} \delta\psi \\ \delta\Phi_n \end{bmatrix} = - \begin{bmatrix} F_\psi \\ F_{\phi_s} \end{bmatrix}$$

where  $A_{\psi\psi}$  and  $A_{\phi_s\phi_s}$  are the main matrices of Poisson and current continuity equation respectively while  $D_{\psi\phi_s}$  and  $A_{\phi_s\psi}$  are the corresponding coupling matrices. The MSP scheme applies a transformation matrix  $T_{MSP}$  to the both sides of the equations

$$T_{MSP} A x = -T_{MSP} F$$

with

$$T_{MSP} = \begin{bmatrix} I & 0 \\ -A_{\phi_s\psi} D_{\psi\psi}^{-1} & I \end{bmatrix}.$$

The ABF scheme applies  $T_{ABF}$  to the right of  $A$  thereby leaving the right hand side of the equations unchanged as shown below

$$(A T_{ABF}) (T_{ABF}^{-1} x) = -F$$

with

$$T_{ABF} = \begin{bmatrix} I & -D_{\psi\psi}^{-1} D_{\psi\phi_s} \\ -D_{\phi_s\phi_s}^{-1} D_{\phi_s\psi} & I \end{bmatrix}.$$

Given the highly nonlinear nature of the semiconductor equations, it is essential to adopt an appropriate update damping scheme with the Newton method so as to ensure the global convergence. With our improved initial guess scheme[3], the task of finding such a scheme becomes less demanding. Still, according to our experience, it is essential for the scheme to keep a tight control over the maximum error in Poisson's equation and to adaptively limit the magnitude of  $\psi$  update. To evaluate the performances of these new schemes, calculations are performed on a coarsely grided one-micron MOSFET using these two schemes as well as the traditional scheme which employs no matrix transformation. Table 1 compares the average CPU time per bias point (averaged from ten bias points with  $V_{ds}$  stepping from 0.5V to 5 V) using the traditional block-Newton (BN) method and MSP and ABF modified block-Newton methods at three values of  $V_{gs}$ . Consistent with the improvement obtained by the MSP-Gummel method over the traditional Gummel method[3], both schemes significantly improve the convergence rate in the strong inversion regime (high  $V_{gs}$ ) of MOSFET calculations. At  $V_{gs} = 5V$ , the speed-ups achieved by the new schemes are 7.5 and 5.2 respectively. Furthermore, the use of these schemes has significantly extended the convergence range of the block-Newton method. Although the traditional scheme has

difficulty to converge beyond a  $V_{ds}$  step of one volt, the new schemes converge with an initial bias as large as  $V_{ds} = 5$  V for all three  $V_{gs}$  values. Calculations are also made to compare the convergence performance of the MSP modified Gummel method and block-Newton methods modified by MSP and ABF. Table 2 shows the average CPU time per bias point as a function of  $V_{ds}$  step for the three schemes. Although the difference between the various schemes is not very significant, MSP modified block-Newton method consistently outperforms the other two schemes.

Parallel computers are cost-effective alternatives to supercomputers in solving large systems of equations such as those encountered in 3-D device simulation. The 3-D device solver is, therefore, developed on such a machine (Intel iPSC2<sup>TM</sup> hypercube, a distributed-memory parallel computer). With each processor (node) has 8M bytes of memory, the solver can handle more than 130K nodes (50 cubes in each dimension) in our 16-node system. In terms of CPU time per bias point, we have observed a performance of about every 2K nodes needing one CPU minute in a machine of about 1.5 MFLOP computation power. Having overcome the huddles in programming the more difficult distributed-memory machine, our 3-D device solver can also be adapted to shared-memory machines with minimum amount of overhead.

**References**

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3. K.-C. Wu, R. F. Lucas, Z.-Y. Wang, and R. W. Dutton, "New Approaches in A Parallel 3-D One-Carrier Device Solver," *Workshop on Numerical Modeling of Processes and Devices for Integrated Circuits -- NUPAD II: Digest of Technical Papers*, May 9-10 1988.
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Table 1  
Effects of Matrix Transformation Schemes

V <sub>gs</sub>	Average CPU (sec.)			CPU speedup	
	BN	MSP-BN	ABF-BN	MSP-BN	ABF-BN
1V	112	75.5	85.8	1.5	1.3
3V	661	134.	164.	4.9	4.0
5V	981	130.	189.	7.5	5.2

Table 2  
Comparison of Gummel and Block-Newton Schemes

V <sub>ds</sub> step	Average CPU (sec.)		
	MSP-Gum.	MSP-BN	ABF-BN
0.5V	145	113	146
1.0V	159	132	171
2.0V	200	175	224
5.0V	286	238	289