Sub-micron MOSFET Model for Circuit Simulation

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The importance of circuit simulator will increase more and more as transistor dimensions are reduced and circuits become larger in scale. In device modeling for circuit simulation, both accuracy and simplicity are necessary. Recently, a lot of researchers have presented a variety of MOS transistor models. BSIM [1,2] is one of the most well-known device models among them and is widely adopted by many circuit simulators. Certainly BSIM is simple, but it has serious drawbacks for circuit simulation. This paper points out these problems and presents a new transistor model which improves on the deficiencies of BSIM. We implemented this model in our circuit simulator MICS(MItsubishi Circuit Simulator), and obtained better results than those obtained by previous models.

The convergence problem of BSIM is not always good, because a point of discontinuity exists in the drain current model. Fig.1 shows the Ids-Vgs characteristics calculated with BSIM. Clearly, there exists a point of discontinuity at:

$$Vgs=Vcut\ (=Vth+30*Xn*Vt) \qquad (1)$$

where Vth : Threshold voltage
Xn : Sub-threshold coefficient
Vt : Thermal voltage

This discontinuity appears when Vds approaches zero volts, because in this bias condition, the drain current model in the strong inversion region(above Vcut) approaches zero amperes but the model near Vth(-Vcut $\sim$ Vcut) doesn't approach zero amperes. So if the circuit has a bi-directional transfer-gate, serious convergence problems will occur.

On the other hand, our model doesn't have a point of discontinuity. Fig.2 shows the Ids-Vgs characteristics calculated with our model using the same parameter as BSIM. A smoother curve can be achieved by our model. By removing discontinuity, better convergence can be obtained in circuit simulation.

In transient analysis, the MOS gate-capacitance model is as important as the drain current model, and the charge conservation principle must be realized in the gate-capacitance model. Consequently, the charge induced at each electrode must be defined with the function of the terminal voltages. Then, as the device size is decreased, short and narrow channel effects must be included in the gate-capacitance model. Only the short channel effect is considered in the BSIM, because of the use of the classical surface potential equation in the sub-threshold region [3]. That is:

$$\psi s=Vgb-Vfb-K_1^2\{-1+\{1+4(Vgb-Vfb)/K_1^2\}^{1/2}\}/\ 2 \qquad (2)$$

where K_1 is body constant. Our model uses the same threshold voltage equation as the drain current model, so we enhance the surface potential equation so that the charge is continuous through the different operation regions. Fig.3 and Fig.4 show the Qg-Vgs and Cgin-Vgs characteristics of our charge-oriented model. Note that the charge continuity is assured and short and narrow channel effects are reflected in these characteristics.

(References)
1.B.J.Sheu et. al,IEEE J.Solid-State Circuits,Vol.SC-22,No.4 558(1987).
2.B.J.Sheu et. al,IEEE Trans. Computer-Aided Design,Vol.CAD-7 ,No.4 520(1988).
3.J.R.Brews,Solid State Electron.,21,345(1978).

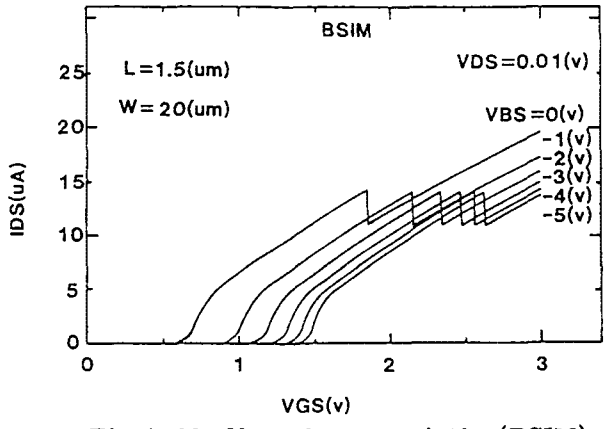


Fig.1 Ids-Vgs characteristics(BSIM)

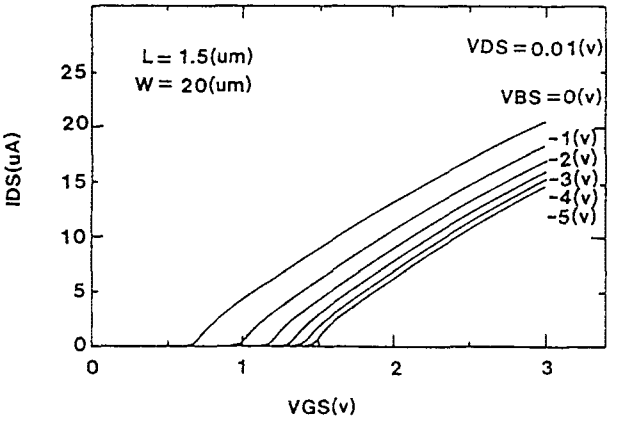
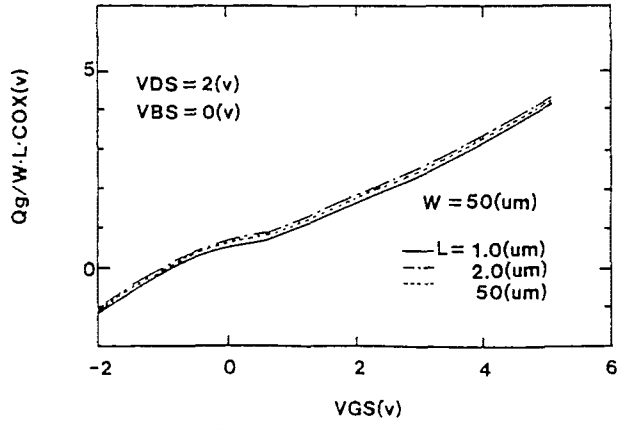
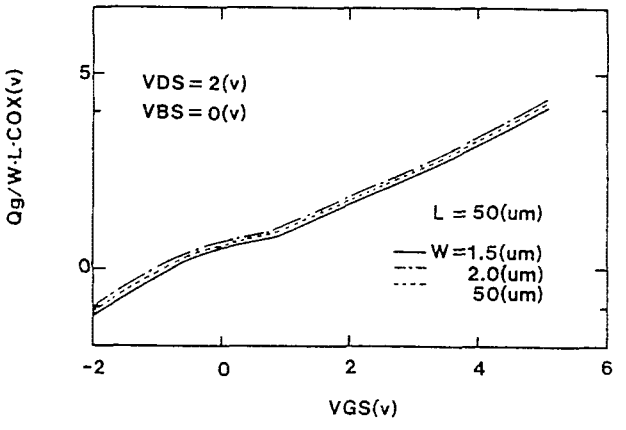


Fig.2 Ids-Vgs characteristics (Proposal model)

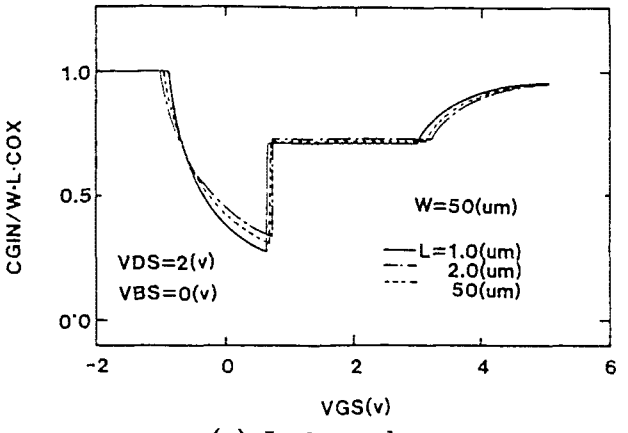


(a) L dependence

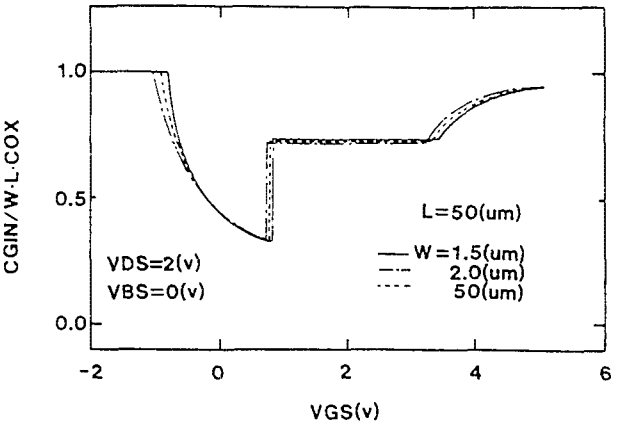


(b) W dependence

Fig.3 Qg-Vgs characteristics (Normalized by W·L·Cox)



(a) L dependence



(b) W dependence

Fig.4 Cgin-Vgs characteristics (Normalized by W·L·Cox)