

Accelerating Simulation of General Gate-All-Around Transistors via a Quasi-1D Model

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Abstract— In this study, we apply an acceleration method based on a quasi-1D model to a three-tier stacked FET. The channel and transistor directions are intentionally modified in an unconventional manner. The proposed method is applied to this modified structure to demonstrate its applicability. We compared the I–V characteristics obtained from TCAD and the initial solution calculated by the quasi-1D model for the PMOSFET and the inverter. The initial solution already shows excellent agreement with the TCAD results. The acceleration model can be applied to such an unconventional structure without any difficulty. It reduces simulation time by at least 5.7× compared to the conventional bias-ramping method.

Keywords— *technology computer-aided design (TCAD), acceleration, quasi-1D model*

I. INTRODUCTION

As technology nodes scale down to the nanometer regime with 3D transistor architectures, Design–Technology Co-Optimization (DTCO) has become increasingly critical [1]–[4]. Traditional DTCO relies on silicon validation, which is costly and time-consuming at early development stages [5]. TCAD simulations allow early-stage evaluation of device and process variations without fabrication [6]–[9]. However, increasing device complexity and process variability require extensive simulations, leading to significant computational burden.

To overcome the computational burden of extensive TCAD simulations, machine-learning (ML)-based approaches have been proposed, such as those based on convolutional neural networks (CNNs) and graph neural networks (GNNs) [10]–[15]. While these methods enable rapid prediction of device characteristics, their accuracy is limited by the range and quality of training data, making generalization to novel device structures challenging. To address this limitation, a quasi-1D model-based acceleration method was previously proposed in [16], enabling calculation of electrical characteristics at the target bias 7–39 times faster than conventional TCAD simulations for a structure with 715k mesh points.

In this work, the quasi-1D model is applied to a three-tier stacked FET structure with unconventional transistor orientations, demonstrating its applicability to highly irregular device geometries. Compared with TCAD simulations, the proposed approach accurately captures the electrical characteristics of such structures within a few percent error, confirming its robustness and extensibility beyond conventional device designs.

II. METHODOLOGY

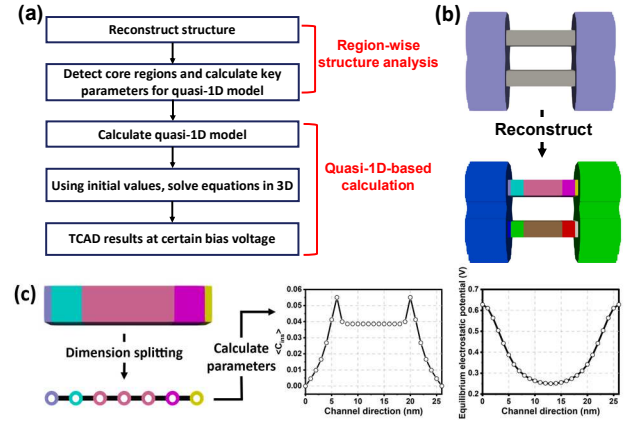


Fig. 1. (a) Flowchart of the overall acceleration method. (b) Partitioned semiconductor regions of the nanosheet FET, where distinct colors denote domains categorized by doping concentration. (c) Each transistor is reduced to a 1D line via dimension splitting, and physical parameters are extracted at discrete points along the channel.

Simulations are performed using the acceleration method proposed in [16] which combines the quasi-1D model with region-wise structure analysis to enable efficient computation of complex 3-D transistor structures. The overall flowchart of the acceleration method is illustrated in Fig. 1(a).

First, region-wise structure analysis is conducted to handle arbitrary geometries. For multi-stack devices, identifying each individual transistor is crucial because the quasi-1D model must be applied to MOSFET paths individually. As shown in Fig. 1(b), the device is partitioned into adjacent geometric elements that share the same material (e.g., Si, SiO₂, ...) and doping polarity (n- or p-type), enabling the identification of individual MOSFET paths. For example, in an n-type nanosheet FET with two stacked channels, two NMOSFETs are identified, and the quasi-1D model is solved for each.

Subsequently, key physical parameters for the quasi-1D model, such as insulator capacitance and channel perimeter, are extracted along the channel direction for the identified transistors (Fig. 1(c)). This extraction is performed using generalized coordinates, ensuring consistent application of the model regardless of the underlying device geometry or coordinate system. Moreover, when multiple paths share common source/drain (S/D) regions, an admittance matrix is calculated to account for the S/D resistance. Test functions, obtained by solving the Laplace equation, are then utilized to reconstruct the initial guess for the S/D regions. The quasi-1D model, solved at discrete points defined by generalized coordinates, couples the 1-D continuity equation

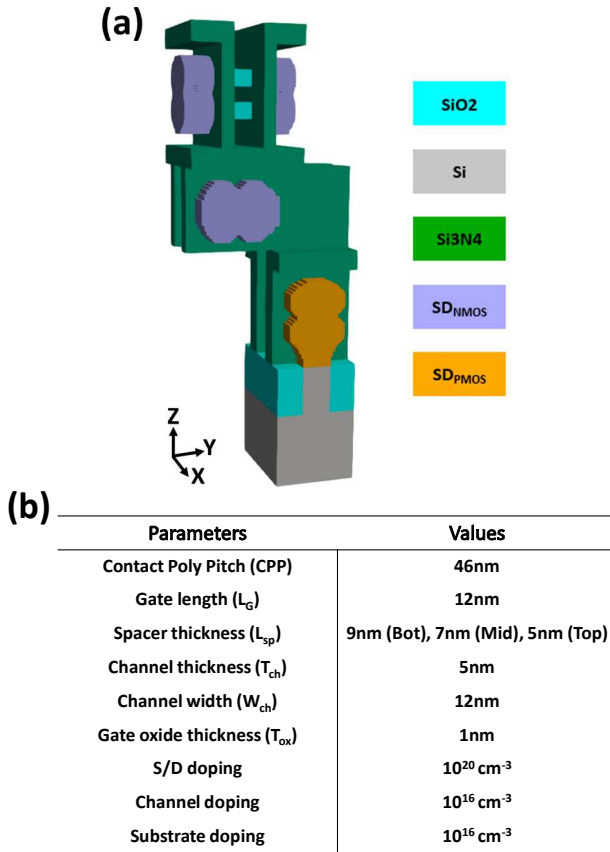


Fig. 2. (a) Modified three-tier stacked FET structure with unconventional transistor arrangement. (b) Device geometric parameters for Fig. 2(a).

with a compact charge model [17]. This compact charge model, derived from coupled Poisson and density-gradient equations, is applicable to arbitrary channel geometries. The resulting 1-D physical quantities, such as quasi-Fermi potentials, are then projected onto the 3-D device structure. The resulting projected quantities provide a robust initial guess, enabling subsequent drift-diffusion simulations to be performed directly at target bias conditions, ensuring both numerical stability and computational efficiency.

III. DEVICE STRUCTURE

To demonstrate that the quasi-1D model is applicable to a wide range of device structures, it is applied to a non-trivial, three-tier stacked transistor structure. The conventional device is intentionally modified, as shown in Fig. 2(a), to verify that the proposed method remains valid even under unconventionally transformed device geometries. The modified structure consists of a bottom PMOSFET and middle and top NMOSFETs. Each transistor in the respective tier contains two channels. The structural transformation is defined relative to the channel direction of each tier. The bottom PMOSFET has its channel direction aligned with the x-axis and the top NMOSFET with the y-axis. The middle NMOSFET also has its channel direction aligned with the x-axis, but it is rotated such that the channel width direction is aligned with the z-axis. Throughout the re-orientation, the primary design criterion is to maintain a straight channel direction for each transistor to enable dimensional reduction onto a 1-D line. This constraint ensures that the quasi-1D model can be consistently applied even when the overall device geometry is significantly transformed. Detailed geometric parameters are summarized in Fig. 2(b).

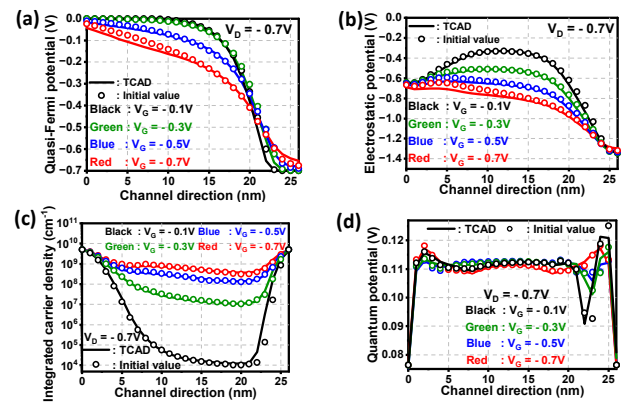


Fig. 3. Comparison of TCAD and quasi-1D results for physical quantities in a PMOSFET: (a) quasi-Fermi potential, (b) average electrostatic potential, (c) integrated carrier density, and (d) average quantum potential.

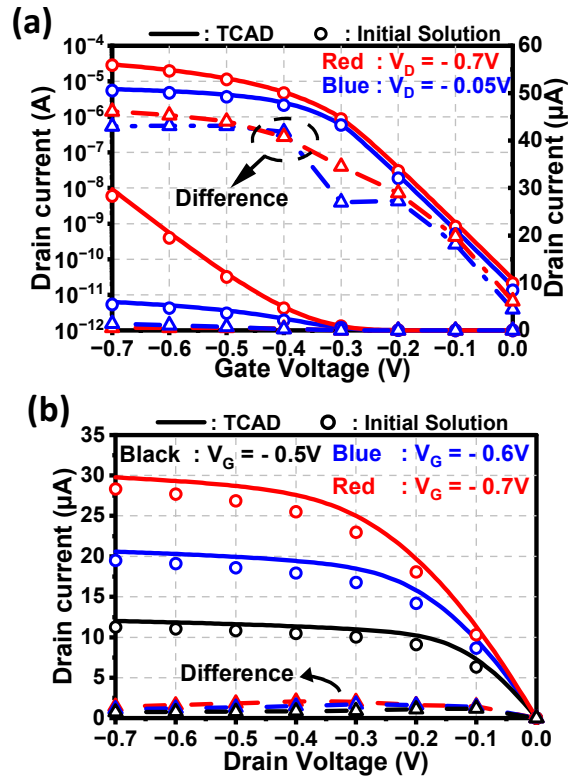


Fig. 4. Comparison of TCAD and quasi-1D results in a PMOSFET, including linear and semi-log plots and their differences: (a) transfer characteristics and (b) output characteristics.

IV. RESULTS AND DISCUSSION

Within the three-tier structure, simulations are first performed on the bottom PMOSFET. Fig. 3 compares quasi-1D and TCAD results for the upper channel path of the two PMOS channels. TCAD simulations are performed using our in-house device simulator G-device [16], [18], [19] with the Mujtaba [20] and Canali mobility models [21]. Four representative quantities calculated by the quasi-1D model are compared: quasi-Fermi potential (Fig. 3(a)), averaged electrostatic potential (Fig. 3(b)), integrated carrier density (Fig. 3(c)) and averaged quantum potential (Fig. 3(d)). All four quantities show good agreement with TCAD results, although small discrepancies are observed. Consistent with the agreement observed in the internal physical quantities, good agreement is also obtained in the electrical

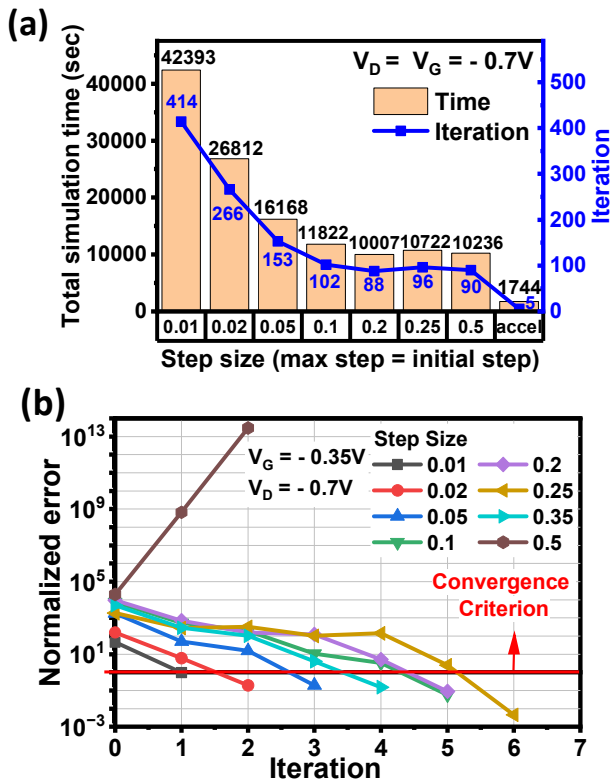


Fig. 5. (a) Comparison of the total simulation time and the number of Newton iterations for I_{ON} calculation. (b) Convergence behavior for different bias step sizes. Larger step sizes require more iterations for convergence, and divergence occurs at a step size of 0.5.

characteristics (Fig. 4(a)) and output characteristics (Fig. 4(b)). In Fig. 4(a), the relative current difference at two drain bias conditions ranges from 0.68% to 23.9%, with the larger relative errors occurring when the drain current is close to zero, where small absolute differences are amplified in terms of relative error. In Fig. 4(b), the relative drain current difference across the three gate bias conditions ranges from 4.79 % to 15.8%, excluding the $V_D = 0V$ case where the current is negligible and the corresponding relative error becomes physically insignificant. These results confirm that the quasi-1D model accurately reproduces the TCAD electrical characteristics.

In Fig. 5(a), the computational time required to extract the on-current from the I-V characteristics shown in Fig. 4 is compared between conventional TCAD and the acceleration method based on the quasi-1D model using a single CPU core. In conventional TCAD simulations, the total computation time shows dependence on the bias step size. Compared with this conventional method, reductions of 5.7–24.3× in computation time and 17.6–82.8× in Newton iterations are achieved, depending on the step size. As shown in Fig. 5(a), increasing the step size initially reduces both the total simulation time and the number of iterations. However, beyond a certain step size (≥ 0.25), the computation time increases again despite the reduced number of ramping steps. This behavior originates from the bias-ramping process inherent to conventional TCAD simulations and constitutes a dominant bottleneck in computational efficiency. Although a larger step size enables the target bias to be reached with fewer ramping steps, numerical convergence at specific bias points becomes increasingly difficult. As a result, the simulator adaptively reduces the step size and re-executes the calculations to recover convergence, which leads to an

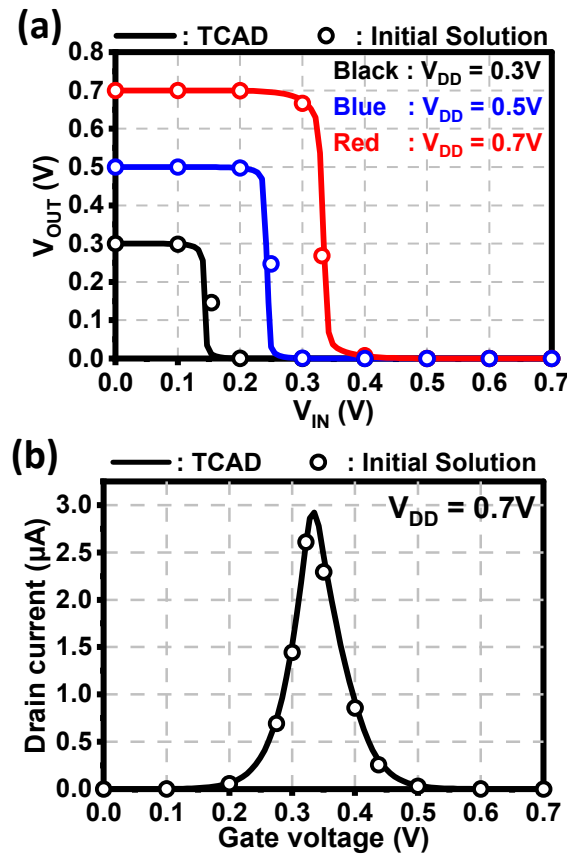


Fig. 6. (a) Voltage transfer characteristics (VTC) and (b) I-V characteristics of the inverter based on the modified structure, where the bottom two tiers operate as a PMOS/NMOS pair.

overall increase in the total simulation time. This convergence behavior is illustrated in Fig. 5(b), where the trend of the normalized error can be observed. When the step size is set to a large value, such as 0.5, the ramping process toward 0.35 V becomes non-convergent, and the normalized error does not decrease below unity, instead showing a divergent tendency. This behavior corresponds to the increased iteration count and computation time observed in Fig. 5(a). In contrast, in the proposed acceleration method, the drift-diffusion model at the target bias is solved using an initial guess obtained from the quasi-1D results, eliminating the need for bias ramping. As a result, the computational time remains nearly constant regardless of the target bias, while avoiding additional iterations caused by ramping-induced convergence issues in conventional TCAD.

Finally, the PMOSFET in the bottom tier and the middle-tier NMOSFET are connected to form an inverter, and the resulting voltage transfer characteristics (VTC) and I-V characteristics are evaluated. The quasi-1D results show close agreement with TCAD, with relative deviations of 0.02–19.3% for the three VTC and 4.8–23.9% for the I-V characteristics. In both cases, the larger relative deviations occur only when the output voltage or current approaches zero, where the corresponding absolute differences remain negligible (Fig. 6).

V. CONCLUSION

The proposed acceleration method, based on a quasi-1D model combined with region-wise structure analysis, has been applied to a modified three-tier stacked transistor structure to evaluate its performance. To further verify its applicability, the

structure is intentionally altered in an unrealistic manner. The method consistently provides accurate initial solutions in good agreement with TCAD results. As a result, the overall simulation efficiency is significantly improved, achieving a 5.7 to 24.3 times reduction in total simulation time and a 17.6 to 82.8 times reduction in Newton iterations. These results demonstrate that the method can be effectively applied even to irregular device structures, offering substantial computational benefits for advanced 3-D device structures.

Beyond the device-level acceleration demonstrated here, the quasi-1D model is expected to serve as an efficient engine for evaluating electrical performance in larger-scale design exploration. Such applications are the subject of future work.

ACKNOWLEDGMENT

This work was supported by K-CHIPS (Korea Collaborative & High-tech Initiative for Prospective Semiconductor Research) (RS-2026-25523338, 2410018350, 26085-45FC) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea).

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