

Power–Performance Assessment of 48 nm Gate-Pitch CFETs Using Experimentally Calibrated Physics-Informed ANN Models

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Abstract—This work presents the first physics-informed artificial neural network (PINN) model for 48-nm gate-pitch (GP) complementary field-effect transistor (CFET) technology, calibrated using silicon data from TSMC. The proposed model accurately reproduces the electrical characteristics of CFET devices and enables efficient circuit-level evaluation of performance and power consumption for a wide range of logic and memory applications. Owing to its computational efficiency, the model supports large-scale simulations of CFET-based integrated circuits containing more than 10^8 transistors. Benchmark studies are performed to compare the power efficiency of multiple CFET technology options, where the 48-nm GP CFET demonstrates favorable energy-efficiency characteristics. The model is further validated under various operating conditions, showing good agreement with device and circuit behavior. These results indicate that the proposed PINN framework provides a practical and scalable solution for technology exploration, design optimization, and system-level evaluation of next-generation CFET-based semiconductor technologies.

Keywords—48 nm Gate Pitch, CFET, Artificial Intelligence, Artificial Neural Network, Equivalent Circuit Model, Device Characteristics, Circuit Simulation, Power Consumption.

I. INTRODUCTION

MOSFET technology has continuously evolved from conventional planar devices to advanced three-dimensional architectures to sustain transistor scaling and improve circuit performance [1]. As conventional scaling approaches fundamental physical limits, further reduction of gate pitch (GP), enhanced electrostatic control, and vertical device integration have become key enablers for future logic technologies. Among the proposed device architectures, complementary field-effect transistors (CFETs), which vertically stack n-type and p-type transistors, have attracted significant attention as a promising extension of CMOS scaling. Recent demonstrations of 48-nm GP CFET technology reported at IEDM 2023 have further validated the feasibility of CFET integration for sub-3-nm technology nodes [2]. Despite substantial progress in CFET fabrication, process integration, and device characterization, circuit-level evaluation of CFET technologies remains relatively limited. One of the primary challenges is the lack of compact and computationally efficient models capable of accurately capturing CFET device behavior while supporting large-scale circuit simulations. Existing studies have mainly focused on device-level analysis or small-scale circuit demonstrations, which are insufficient for assessing the performance and power characteristics of large-scale integrated systems.

Recently, artificial neural network (ANN)-based device models have emerged as an effective approach for representing

the highly nonlinear electrical behavior of advanced transistors [3]–[8]. Compared with conventional analytical compact models, ANN-based approaches offer greater modeling flexibility and improved fitting capability. Furthermore, physics-informed ANN frameworks have been proposed to incorporate device physics into the learning process, thereby improving model consistency, reliability, and extrapolation performance [5]–[8]. However, most reported ANN-based device models have been developed for individual transistors or limited circuit benchmarks, and their applicability to large-scale CFET-based chip simulations has not been fully demonstrated.

In this work, a physics-informed ANN (PINN) equivalent model is developed for advanced CFET technologies using silicon measurement data. The proposed model accurately reproduces CFET electrical characteristics while maintaining computational efficiency for circuit-level simulation. The model is further integrated into a design framework that enables performance and power evaluation of logic and memory circuits as well as large-scale CFET chips containing more than 10^8 transistors. This work provides an efficient platform for CFET technology assessment, circuit design exploration, and system-level optimization for advanced semiconductor technologies.

II. MODELING METHODOLOGY

A PINN model was advanced for the 48-nm GP CFET technology with a 15-nm gate length (L_G), based on measured silicon data from fabricated TSMC CFET devices [2]. The objective of the model is to accurately reproduce device characteristics while maintaining computational efficiency suitable for large-scale circuit simulation. As shown in Fig. 1, the proposed ANN adopts a two-stage physics-informed architecture. In the first stage, the network incorporates the Grove–Frohmman (GF) model [9], which provides a physics-based description of MOSFET drain current behavior. By embedding the GF formulation into the learning framework, the model preserves current-voltage characteristics and improves prediction robustness in operating regions with limited training data coverage. This stage generates an initial estimation of the drain-to-source current based on device bias conditions. The second stage employs a residual-learning ANN to capture discrepancies between the GF-model prediction and measured silicon data. Instead of directly learning the complete device behavior, the ANN focuses on modeling the remaining nonlinear components not represented by the analytical formulation. The final drain current is obtained by combining the outputs of the two stages, resulting in a compact and physically consistent model. Key network hyperparameters and training configurations are summarized in Table I.

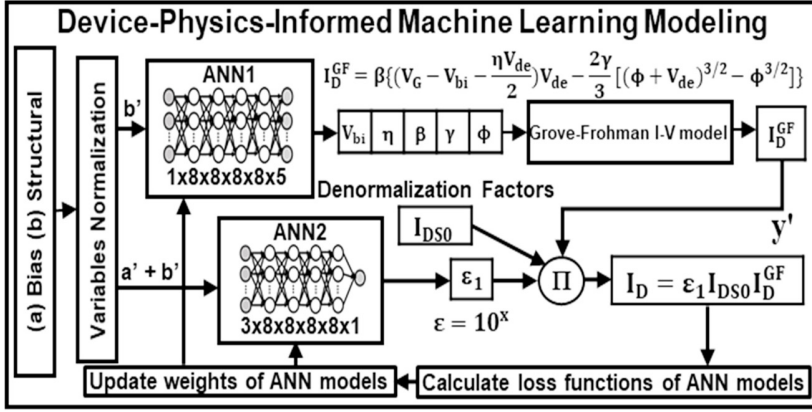


Fig. 1. Flow of the entire training process of the physics-informed AI model [3-4]. The outputs of ANN1 are used in the GF model and the ANN2 serves a correction coefficient to refine the drain current (I_D) by adjusting the output weights.

TABLE I. LIST OF THE ADOPTED HYPERPARAMETERS OF THE ANN1 AND ANN2 USED IN THE PROCESS OF TRAINING OF AI MODEL.

ANN1		ANN2	
Parameters	Value	Parameters	Value
Hidden Layers	4	Hidden Layers	4
Neurons	8, 8, 8, 8	Neurons	8, 8, 8, 8
Epochs	1200	Epochs	1200
Learning Rate	0.01	Learning Rate	0.01
Scheduler	StepLR	Scheduler	StepLR
Activation Function	tanh	Activation Function	tanh
Loss function	MSE	Loss function	MSE
Optimizer	SGD	Optimizer	SGD

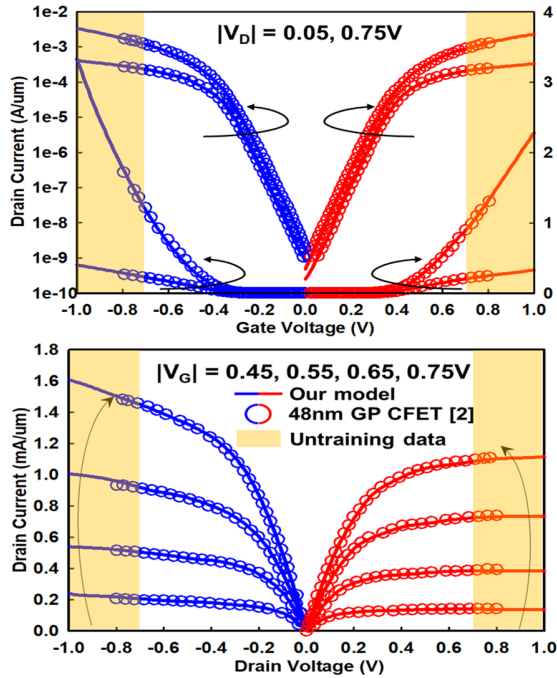


Fig. 2. Comparison of I_D - V_G and I_D - V_D characteristics between the proposed AI model and TSMC measured CFET data. The model trained from 0–0.7 V accurately extrapolates to 1 V with a maximum RMSE of 1.96×10^{-5} .

To evaluate the generality of this work, equivalent PINN models were also developed for TSRI CFET technology [10] and Intel's projected 48-nm GP CFET technology with a 16-nm gate length [11], [12]. The TSRI device represents an academic research platform, whereas the Intel device provides a reference for a highly optimized projected CFET implementation. Applying the same modeling methodology across these technology nodes enables a consistent comparison of device and circuit-level characteristics while showing the transferability of the proposed ANN framework. The extracted ANN models were subsequently integrated into circuit simulation environments for logic, memory, and large-scale system evaluations. This methodology enables efficient performance and power analysis while maintaining compatibility with conventional circuit-design workflows.

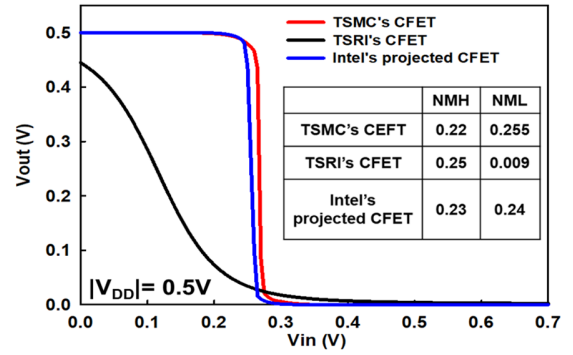


Fig. 3. Comparison of the VTC and NMH/NML of the CFET inverter among TSMC, TSRI, and Intel.

III. RESULTS AND DISCUSSION

First, we report the device-level validation. Fig. 2 compares the I_D - V_G characteristics generated by the proposed PINN model with measured data from the TSMC 48-nm GP CFET. Solid lines denote model predictions, whereas symbols represent measurement results. The model was trained using data within a gate-voltage range of 0–0.7 V and subsequently evaluated under extrapolated bias conditions up to 1.0 V. Excellent agreement is observed between the model and measurement across both the training and extrapolation regions, yielding a root mean square error (RMSE) of 1.96×10^{-5} . The results indicate that the proposed two-stage framework effectively captures the nonlinear current behavior of CFET devices while maintaining physically consistent current characteristics beyond the training range. Accurate reproduction of both subthreshold and near-threshold operation confirms the suitability of the model for circuit-level simulation.

Second, we discuss the logic circuit evaluation. The extracted ANN compact models were implemented in HSPICE for circuit-level validation and benchmarking. In addition to the TSMC 48-nm GP CFET, equivalent models were developed for TSRI CFET and Intel-projected CFET technologies under identical supply-voltage and operating-frequency conditions. Fig. 3 presents the voltage transfer characteristics (VTCs) of CFET inverters. The TSMC CFET exhibits balanced switching behavior with comparable noise margin high (NMH) and noise margin low (NML), indicating effective matching between the

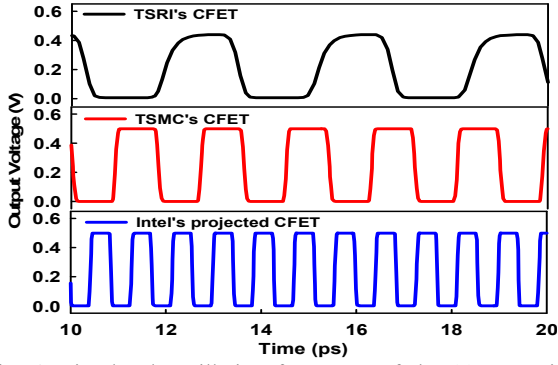


Fig. 4. Simulated oscillation frequency of the 11-stage ring oscillator for TSMC, TSRI, and Intel CFETs. The extracted frequencies are 306, 556, and 1100 GHz, respectively.

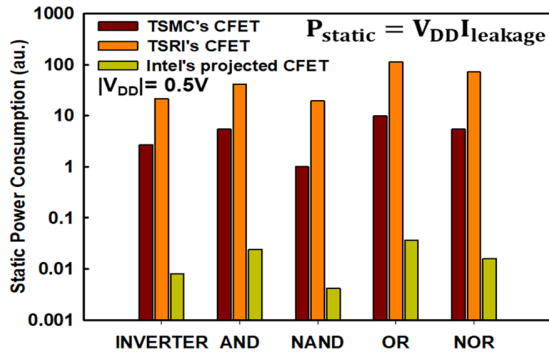


Fig. 5. Calculation of the static power consumption for various logic gates under the same supply voltage among TSMC, TSRI, and Intel.

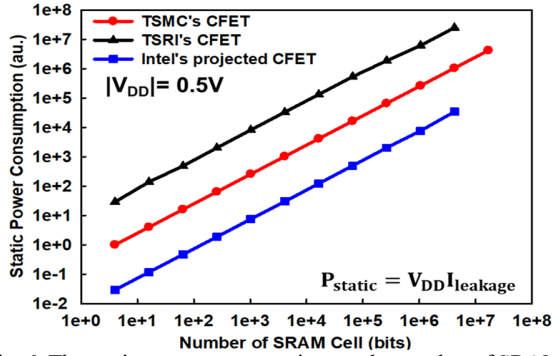


Fig. 6. The static power consumption vs. the number of SRAM cells among TSMC, TSRI, and Intel. Notably, our AI models of CFET are capable of simulating circuits containing over 100 million transistors.

stacked n-type and p-type devices. Although the Intel-projected CFET shows a steeper transition region, the simulation results demonstrate that the proposed ANN model can successfully capture technology-dependent inverter characteristics. Further validation is performed using an 11-stage ring oscillator (RO). As shown in Fig. 4, the extracted oscillation frequencies are 306 GHz, 556 GHz, and 1100 GHz for TSRI CFET, TSMC CFET, and Intel-projected CFET, respectively. The frequency trends are consistent with the expected differences in device scaling and current-driving capability. These results verify that the proposed model can accurately translate device-level characteristics into circuit-level timing behavior.

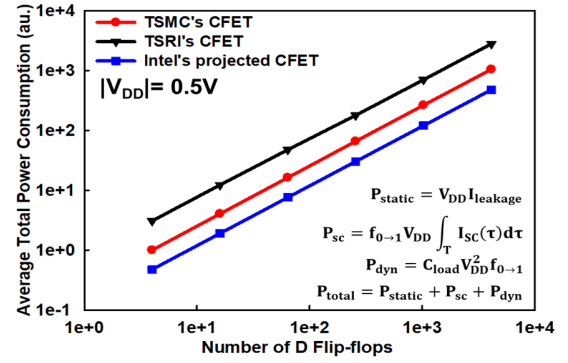


Fig. 7. The average total power consumption vs. the number of DFFs under the same supply voltage and operational frequency among TSMC, TSRI, and Intel.

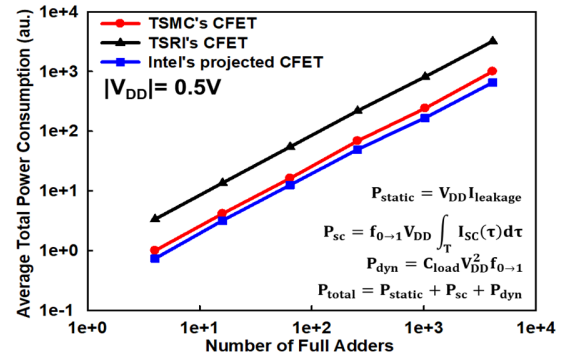


Fig. 8. The average total power consumption vs. the number of FAs under the same supply voltage and operational frequency among TSMC, TSRI, and Intel.

We now analyze power consumption and assess large-scale scalability. Static power consumption was evaluated using a set of representative logic gates, including AND, NAND, OR, and NOR structures. As shown in Fig. 5, the TSMC 48-nm GP CFET achieves lower leakage power than TSRI CFET, while Intel-projected CFET exhibits the lowest static power among the evaluated technologies. The results demonstrate the capability of the proposed model to quantify leakage characteristics across different CFET implementations. Dynamic power performance was further investigated using D flip-flops (DFFs) and full adders (FAs). The average power consumption results are shown in Figs. 7 and 8. Compared with TSRI CFET, the TSMC 48-nm GP CFET achieves approximately threefold lower power consumption. Intel-projected CFET further reduces power consumption by approximately 1.5 $\times$ relative to the TSMC implementation. These results confirm that the proposed ANN framework can accurately evaluate both static and dynamic power characteristics under realistic switching conditions.

The scalability of the proposed modeling framework was examined using SRAM arrays with increasing cell counts. Fig. 6 shows that the TSMC 48-nm GP CFET SRAM exhibits approximately 20 $\times$ lower static power consumption than TSRI CFET as the array size increases. The observed trend indicates favorable leakage scaling characteristics for large memory structures. More importantly, the proposed PINN model remains numerically stable when applied to extremely large circuit simulations. The framework supports circuit evaluation

TABLE II. RECENT ANN-BASED COMPACT MODELS FOR CFET CIRCUIT SIMULATION WITH VARIOUS TRANSISTOR NUMBERS.

Transistor Numbers	[4]	[5]	[6]	This Work
$<10^2$	✓	✓	✓	✓
$10^2\sim10^4$	–	✓	✓	✓
$10^4\sim10^6$	–	–	✓	✓
$\sim10^8$	–	–	–	✓

containing more than 10^8 transistors without requiring additional model simplification. Table II compares the proposed approach with previously reported ANN-based circuit simulation methods. While most prior works focused on individual devices or small-scale circuit demonstrations, the present work extends ANN-based CFET simulation to chip-level analysis. This capability enables efficient power-performance exploration for future CFET-based logic and memory systems. To the best of our knowledge, this is the first PINN-based CFET compact model demonstrated for circuit simulations exceeding 10^8 transistors.

IV. CONCLUSION

This work reported a PINN equivalent modeling framework for advanced CFET technologies. By integrating a physics-based current formulation with ANN-based residual learning, the proposed model accurately reproduces the electrical characteristics of CFET devices while preserving physical consistency beyond the training domain. Using measured silicon data from TSMC 48-nm GP CFET technology, the developed model achieved excellent agreement with experimental device characteristics and demonstrated reliable extrapolation capability under extended bias conditions. The extracted ANN compact model was further implemented in HSPICE for circuit-level evaluation of logic and memory structures, including inverters, ring oscillators, logic gates, SRAM arrays, D flip-flops, and full adders. Comparative benchmarking with TSRI and Intel-projected CFET technologies confirmed that the proposed framework accurately captures technology-dependent performance and power-consumption trends across different CFET implementations. More importantly, the proposed methodology extends ANN-based device modeling beyond conventional device-scale and small-circuit demonstrations by enabling stable simulation of CFET-based systems containing more than 10^8 transistors. To the best of our knowledge, this represents the first PINN-based CFET modeling framework shown at a chip-level simulation scale. The combination of measurement-calibrated accuracy, physical consistency, and large-scale simulation capability establishes the proposed framework as an efficient platform for CFET technology assessment, circuit design exploration, and power-performance optimization. These capabilities make the framework particularly attractive for future design-technology co-

optimization [13] and system-technology co-optimization studies targeting sub-2-nm semiconductor technologies. The reported scalability and predictive capability suggest that PINN modeling can serve as a practical bridge between silicon measurements and system-level evaluation for future CFET-based ICs.

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REFERENCES

- [1] S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices*, 4th ed., Wiley, 2021.
- [2] S. Liao et al., “Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling,” in: *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2023, pp. 1-4.
- [3] S. Lee et al., “Multi-Task Learning for Real-Time BSIM-CMG Parameter Extraction of NSFETs With Multiple Structural Variations,” *IEEE Access*, vol. 12, 2024, pp. 184619-184628.
- [4] A. Singhal and H. Agarwal, “ANN-Driven Modeling of Gate-All-Around Transistors Incorporating Complete Current Profiles,” *IEEE Transactions on Nanotechnology*, vol. 24, 2025, pp. 110-114.
- [5] Y.-S. Yang, Y. Li and S. R. Kola, “A Physical-Based Artificial Neural Networks Compact Modeling Framework for Emerging FETs,” *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 223-230, Jan. 2024.
- [6] Y. Tai, Y. Li and M.-H. Chuang, “A Device-Physics-Informed Artificial Neural Network Approach for Thermal-Aware I-V and C-V Modeling of GAA FETs,” *IEEE Access*, vol. 14, pp. 67674-67686.
- [7] Y. Dei, Y.-S. Yang and Y. Li, “Compact Modeling of N- and P-Type GAA NS FETs Using Physical-Based Artificial Neural Networks with Temperature Dependence,” *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Kobe, Japan, 2023, pp. 285-288.
- [8] Y. Li, Y. Tai and M.-H. Chuang, “Temperature-Dependent Current-Voltage Model for Emerging GAA NS FETs Using a Physics-Inspired Neural Network,” *2026 27th International Symposium on Quality Electronic Design (ISQED)*, San Francisco, CA, USA, 2026, pp. 1-8.
- [9] D. Frohman-Bentchkowsky and A. S. Grove, “Conductance of MOS transistors in saturation,” *IEEE Trans. Electron Devices*, vol. 16, no. 1, Jan. 1969, pp. 108-113.
- [10] S.-W. Chang et al., “First Demonstration of CMOS Inverter and 6T-SRAM Based on GAA CFETs Structure for 3D-IC Applications,” *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2019, pp. 11.7.1-11.7.4.
- [11] C.-Y. Huang et al., “3-D self-aligned stacked NMOS-on-PMOS nanoribbon transistors for continued Moore’s law scaling,” *IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 425-428.
- [12] S. R. Kola and Y. Li, “Electrical Characteristic and Power Fluctuations of GAA Si NS CFETs by Simultaneously Considering Six Process Variation Factors,” *IEEE Open Journal of Nanotechnology*, vol. 4, 2023, pp. 229-238.
- [13] Y.-W. Xu and Y. Li, “Pioneering the Use of Response Surface Modeling for Complementary Field-Effect Transistors Design and Optimization,” *2026 27th International Symposium on Quality Electronic Design (ISQED)*, San Francisco, CA, USA, 2026, pp. 1-9.