

SEMulator3D[®] Linking Deposition Process to Electrical Metrics-Accelerated WAT Learning

Xing Qin
Lam Research Corporation
Shanghai, China
xing.qin@lamresearch.com

Tristan Yang
Lam Research Corporation
Shanghai, China
tristan.yang@lamresearch.com

Deyong Kong
Lam Research Corporation
Shanghai, China
deyong.kong@lamresearch.com

Xiaoqiang Wan
Lam Research Corporation
Shanghai, China
xiaoqiang.wan@lamresearch.com

Abstract— In semiconductor manufacturing, Tungsten (W) is widely used in logic contact and metal gate fill for its low resistivity and excellent conformal fill capability. As a result, the W deposition process plays a critical role in determining overall device performance. Although both W deposition behavior and the electrical characteristics of High-K Metal Gate (HKMG) stacks are well studied individually, the direct linkage between deposition-process variation and HKMG electrical performance has rarely been reported. In this work, we leverage the virtual-fabrication capabilities of SEMulator3D[®] from Lam Research to quantitatively analyze how key process parameters in W deposition influence film properties, and how these film-level changes propagate to the final electrical performance of HKMG devices. Through high-fidelity 3D process modeling combined with electrical simulation, we systematically uncover the relationships between tungsten fill characteristics and HKMG behavior. The result shows trade-off between threshold voltage (V_t), saturation/off current and direct current matrices is solved, and over 10% gap of original performance to target has been eliminated. This reveals the value in utilizing virtual fabrication to predict deposition process induced device changes and optimize process for wafer acceptance test (WAT) ready for manufacturing. This approach demonstrates significant improvement in accelerating development cycles, reducing R&D costs, widening process window of semiconductor devices, and ultimately improving WAT and yield.

Keywords— metal gate, tungsten, deposition, wafer acceptance test, device simulation

I. INTRODUCTION

Continued device scaling strains traditional SiO_2 /polysilicon gate stacks because ultrathin oxide (<2 nm) suffers unacceptable tunneling leakage via quantum tunneling, raising static power and heat generation. High-K Metal Gate (HKMG) technology replaces SiO_2 with high k dielectrics and polysilicon with metal electrodes to suppress leakage and tune threshold voltages for (NMOS) and PMOS. In modern HKMG flows, tungsten is an essential fill material to regulate NMOS and PMOS to suitable threshold voltage (V_t), but its deposition conditions can introduce intrinsic stress and incorporate/transport fluorine, both of which modulate the effective work function (EWF) and thereby WAT performance including V_t and on/off currents.

SEMulator3D[®], a modeling platform within Lam Research's Semiverse[®] Solutions suite, enables virtual fabrication, virtual electrical testing, and fast design of experiments (DOE) through process modeling. It significantly accelerates the process development and improvement while

achieving cost savings [1]. Traditional method of optimizing wafer processing for electrical performance in wafer acceptance test (WAT) typically requires around 5 iterations in a 3 months span. Combined virtual fabrication and testing have the potential to shorten the time needed by improving the efficiency of tungsten deposition process development through early identification of optimal process conditions, prediction of electrical and mechanical outcomes, and quickly narrowing the experimental space.

In this work, SEMulator3D[®] was utilized to simulate W deposition process in Lam's ALTUS[®] Max tool to optimize its process parameters for WAT performance. It facilitates the capability to analyze the film properties to predict electrical outcomes of the device including threshold voltage (V_t), saturation current (I_{dsat}), and off-state current (I_{off}). Leveraging this platform, we investigated the impact of W films on device performance and the underlying mechanisms. Ultimately, a process recipe was successfully developed with optimal WAT performance within a period much less than traditional method.

II. MODELING

A. Layout and process build

A 2D layout created with KLayout was imported into SEMulator3D[®], and a full HKMG transistor process was constructed through a sequence of virtual steps mirroring the fab flow. Contact were defined for gate, source, and drain to enable electrical simulation. Figure 1 summarizes the workflow.



Fig. 1. Device and electrical simulation workflow

B. Materials calibration

The W film's intrinsic stress distribution uses material library of SEMulator3D[®], and parameters calibrated to blanket wafer measurements. Fluorine concentration profiles and diffusion behavior were set based on SIMS data from blanket films and then applied to in feature geometries to capture geometry dependent transport. Fluorine diffusion

behavior within multi-film stacked metal gates is studied by virtual W deposition.

C. Tungsten process space

We explored in feature W fill conditions representative of silane and diborane nucleation chemistries (SiH_4 vs. B_2H_6), as well as gas mixtures. These variations lead to distinct intrinsic stress states and microstructure in the W film, which couple into the channel and the p type work function metal (e.g., TiN/TiAl)

D. Electrical analysis

Different W films deposition in metal gate electrode were considered to evaluate the impact of stress transfer and fluorine diffusion on the effective work function (EFW) of metal gate. To better understand the underlying mechanism of EFW changes and predict the influence of W, SEMulator3D[®] analysis was used to simulate the transistor electrical performance under varying gate effective work functions. The V_t , I_{dsat} and I_{off} were extracted, and direct current (DC) performance defined as $\text{DC} = I_{\text{dsat}}/I_{\text{off}}$ based on diffusion-drift model was calculated.

III. RESULTS AND DISCUSSION

Virtual DOE shows that the tungsten nucleation chemistry strongly influences intrinsic film stress and, through stress transfer, the stress state of both the Si channel and the TiN work function layer. SiH_4 reduced W exhibits higher tensile intrinsic stress than B_2H_6 based nucleation, consistent with differences in crystallization and grain size, and causes the channel/TiN to shift toward more compressive stress under otherwise identical conditions (Fig. 2). The magnitude of stress transfer scales with W in feature volume and with device flavor: PMOS shows a larger stress change amplitude than NMOS, reflecting hole mobility benefits under compressive channel stress. However, the same compressive shift also tends to raise the EFW, creating a trade-off between mobility gain and V_t increase. Process recipes that target moderate compressive transfer can enhance PMOS mobility and DC performance without incurring excessive EFW induced V_t penalty. Compressive stress is helpful for hole carrier mobility thus increase DC performance, but it will make EFW of TiN metal and gate electrode higher[2].

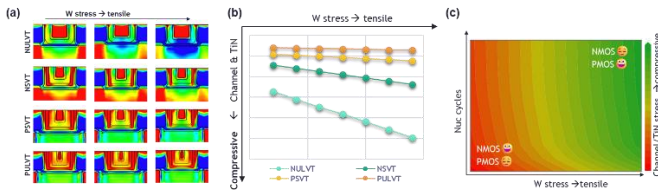


Fig.2. Swept Tungsten deposition simulation for in-feature fill DOE

Fluorine incorporated in the W film diffuses into underlying work function metals during subsequent processing. Simulations capture a clear W volume dependence: larger in feature W volumes drive stronger fluorine ingress into TiN/TiAl stacks (Fig. 3). Fluorine can trap Al that would otherwise diffuse into TiN to form a dipole, degrading dipole formation and increasing the effective work function, which elevates V_t and shifts WAT metrics. Consequently, controlling the fluorine content and its diffusion pathways is essential for stable threshold setting, particularly for TiAl based work function stacks[3]. More fluorine diffusion from W means a higher EFW of metal gate

electrode. W deposition conditions that minimize fluorine incorporation—or that kinetically hinder its transport—expand the acceptable process window for EFW and V_t control.

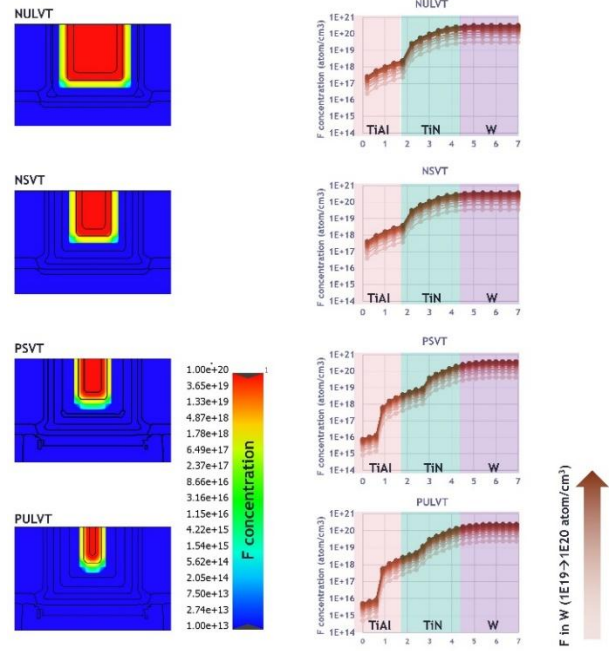


Fig.3. Fluorine diffusion simulation under different W film

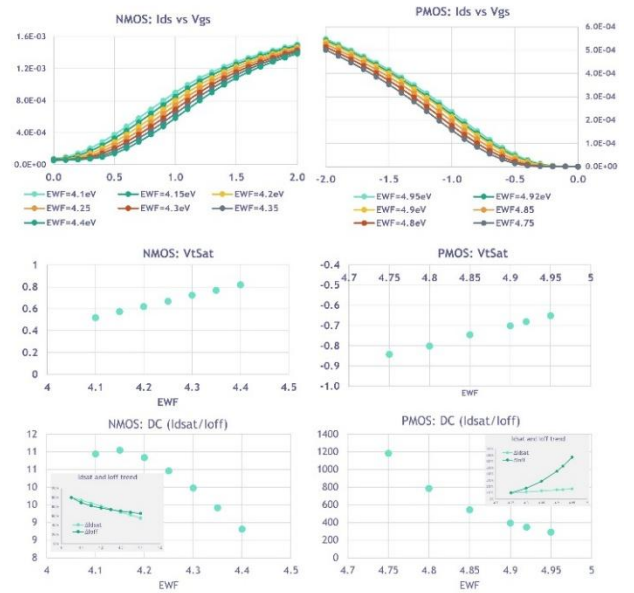


Fig.4. Electrical simulation of device under different gate EFW

To separate geometric/process effects from electrostatics, we swept EFW in the electrical model and analyzed the device response (Fig. 4). V_t increases approximately linearly with EFW for both NMOS and PMOS, as expected for HKMG stacks. The DC metric ($I_{\text{dsat}}/I_{\text{off}}$) is nonlinear versus EFW because I_{dsat} and I_{off} exhibit different sensitivities to barrier modulation and subthreshold transport. Because EFW tuning concurrently affects V_t , I_{dsat} , and I_{off} in different ways, optimal WAT performance is achieved by co-optimizing stress

transfer and fluorine diffusion—not by maximizing one lever alone.

By mapping W chemistry, in-feature fill, stress transfer, and fluorine transport to EWF and electrical metrics, SEMulator3D® narrows the experimental search space before running wafers. In our study, this workflow guided precursor selection (SiH_4 vs. B_2H_6 or mixtures) and fill conditions to meet target V_t and DC windows for ultra low V_t (ULVT) and standard V_t (SVT) NMOS and PMOS devices, leading to a recipe with improved WAT without multiple wafer iterations.

IV. CONCLUSION

SEMulator3D® based virtual fabrication reliably links tungsten deposition physics (intrinsic stress and fluorine diffusion) to metal gate EWF and device electrical behavior. The calibrated workflow predicts process induced shifts in V_t , I_{dsat} , and I_{off} , explains device type sensitivities, and exposes the trade space between mobility enhancement and EWF induced threshold changes. This enables efficient DOE exploration, fewer wafer runs, reduced development time and cost, and improved WAT and yield for HKMG technologies.

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