

Semi-Classical Monte Carlo Simulation of Contact Geometry Effect on Source/Drain Junction Resistance in N-Type Si Fin and Nanosheet FETs

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Abstract— Using three-dimensional semi-classical Monte Carlo (SCMC) simulation with quantum corrections, this work examines how contact geometry governs the source/drain (S/D) junction resistance and the overall behavior of n-type Si FinFETs and nanosheet FETs (NSFETs). Two configurations, End Contact (EC) and Wrap-Around Contact (WAC), are studied. EC directly injects carriers along a path matched to the source-to-drain (S-to-D) direction, whereas WAC forces a roughly 90° momentum redirection on carriers before they enter the channel. By avoiding this redirection, EC yields a higher on-current (I_{ON}) than WAC. Raising the S/D doping concentration reduces the EC-WAC difference in I_{ON} , since the added scattering helps carriers perform the redirection which WAC requires. For recessed contacts, enlarging the contact area which feeds carriers directly into the channel raises I_{ON} . These findings establish contact geometry as a strong determinant of the S/D junction resistance in both architectures, and they indicate that scaled devices should optimize the contact geometry to minimize the momentum change imposed on carriers before they enter the channel.

Keywords— carrier momentum, contact geometry, FinFETs, Monte Carlo simulation, NSFETs, phonon scattering, quantum confinement

I. INTRODUCTION

As CMOS technology is aggressively scaled, parasitic resistance has overtaken the intrinsic channel resistance as the principal limiter of device performance, with the resistance at the source/drain (S/D)-to-channel junction constituting its largest component. This challenge is intensified by the architectural shift from FinFETs to gate-all-around (GAA) nanosheet FETs (NSFETs), in which several vertically stacked channels are supplied by a single common S/D epitaxial pillar and its contact. The configuration of this contact around the pillar consequently exerts a strong influence on the drive current achievable at nodes below 2 nm.

Conventional strategies for reducing junction resistance have emphasized enlarging the effective S/D contact area and shortening the carrier path from the contact to the channel. Aggressive pitch scaling, however, leaves diminishing room for area expansion. The channel thickness is likewise scaled to retain electrostatic integrity, which shortens the transport path but simultaneously intensifies quantum confinement

(QC) and confines carriers within a progressively narrower channel. As these factors jointly impede injection, directing carriers into the channel along the source-to-drain (S-to-D) orientation becomes essential, and the contact geometry that governs this injection direction emerges as a key design parameter [1]. Process technology, however, places stringent limits on the realizable geometry. As the pitch is reduced, conformal metallization of deep and narrow S/D regions becomes impractical, rendering an idealized contact that spans the full S/D depth and uniformly addresses every nanosheet difficult to fabricate. Realistic structures therefore expose only a portion of the S/D surface or embed the metal within the pillar.

In this work, the influence of contact geometry on the S/D junction resistance and the overall characteristics of FinFETs and 1-, 2-, and 3-Stack NSFETs is assessed using ensemble semi-classical Monte Carlo (SCMC) simulation. End Contact (EC) and Wrap-Around Contact (WAC) are first evaluated at an identical contact area so that purely geometric effects are decoupled from contact-area effects. The S/D doping concentration is subsequently varied to elucidate how scattering mediates the momentum redirection imposed on carriers injected through the WAC from the S/D into the channel. Recessed contacts are finally analyzed for both device types as the metal penetration depth and width into the S/D pillar are varied.

II. SIMULATION METHODOLOGY AND DEVICE STRUCTURE

A. Simulation Methodology

Our analysis is carried out with an in-house three-dimensional (3D) SCMC simulator that couples the Boltzmann transport equation to Poisson's equation in a self-consistent loop [2], [3]. Solving the two together captures the non-equilibrium carrier distribution and degenerate statistics of the device, both of which are required to describe quasi-ballistic transport in heavily scaled FinFETs and NSFETs. The silicon conduction band is represented by an analytic non-parabolic effective-mass model, and intravalley and intervalley phonon scattering are treated alongside ionized impurity scattering. To account for QC, the two-dimensional effective-mass Schrödinger equation is solved on the cross-sectional plane normal to the source-to-drain (S-to-D) direction, and the resulting subband corrections are applied within the narrow channel, where confinement produces pronounced subband quantization.

The electrostatic potential is obtained on a uniform 0.5 nm finite-difference grid. The metal-semiconductor boundaries at the source and drain terminals are taken as ideal ohmic contacts that inject and absorb carriers perfectly. Because this

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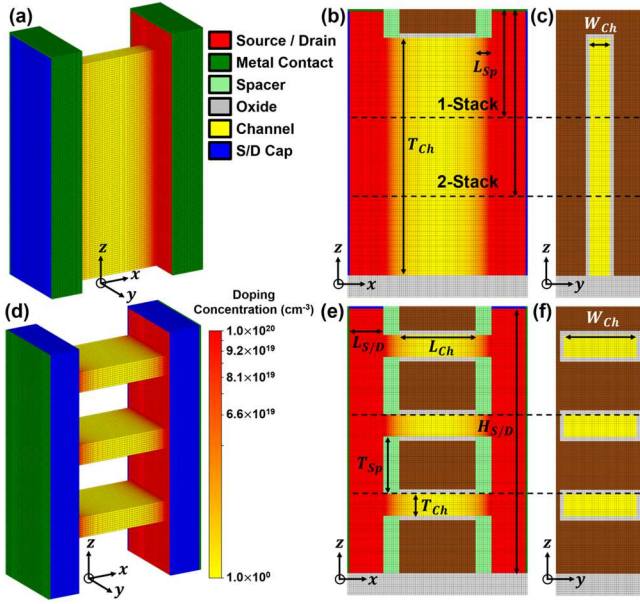


Fig. 1. 3D device structures and cross-sectional views. (a) 3D schematic of 3-Stack FinFETs with WAC. (b), (c) x-z and y-z cross-sections of FinFETs. (d) 3D schematic of 3-Stack NSFETs with EC. (e), (f) x-z and y-z cross-sections of NSFETs. Dashed lines at (b), (c), (d), (f) indicate the boundaries for the 1- and 2-Stack configurations.

TABLE I

PARAMETERS FOR SIMULATED DEVICES OF FINFETs AND NSFETs			
Parameter		FinFETs	NSFETs
S/D Doping Density	N_D (cm ⁻³)		1×10^{20}
Effective Oxide Thickness	EOT (nm)		1
S/D Height	$H_{S/D}$ (nm)		60
S/D Width	$W_{S/D}$ (nm)		20
S/D Length	$L_{S/D}$ (nm)		8.5
Sheet Spacing	T_{Sp} (nm)	-	13
Spacer Length	L_{Spa} (nm)		4
Channel Width	W_{Ch} (nm)	5	18
Channel Thickness	T_{Ch} (nm)	54	5
Channel Length	L_{Ch} (nm)		19
Channel Area of y-z Cross-Section	A_{Ch} (nm ²)		270

boundary removes the contact resistance, the geometric contribution of the contact can be examined in isolation.

A drain bias of $V_{DS} = 0.7$ V is applied. The threshold voltage V_T is defined by the constant-current condition $I_{DS} = 0.05$ mA/ μ m, with I_{DS} normalized to the S/D width $W_{S/D}$, and the on-current (I_{ON}) is read at an overdrive of $V_{OV} = 0.3$ V, that is, at $V_{ON} = V_T + V_{OV}$.

B. Device Structure

The simulated FinFETs and 3-Stack NSFETs devices are depicted in Fig. 1, and their geometric parameters are listed in Table I. Both architectures have the same contact poly pitch, gate length, and effective channel cross-sectional area. Therefore, they differ in only two respects, namely how the channel area is divided and the QC direction in the channel. The FinFETs keeps the whole channel area in one tall fin, while the NSFETs splits the same area among three stacked nanosheets. Every channel runs along the $\langle 110 \rangle$ S-to-D direction on a (100) wafer, and the S/D doping decreases exponentially into the channel at 2 nm/dec.

The EC and WAC configurations are used to study how the metal-interface location affects carrier injection. The two share identical S/D dimensions and doping, and differ only in where the metal meets the pillar. In EC, the metal is placed

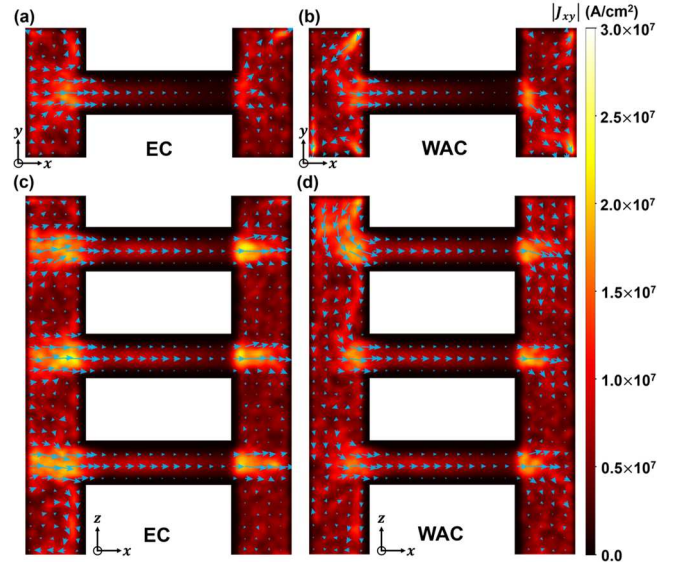


Fig. 2. Comparison of current density distributions for different contact geometries. (a) x-y cross-section of 3-Stack FinFETs with EC. (b) x-y cross-section of 3-Stack FinFETs with WAC. (c) x-z cross-section of 3-Stack NSFETs with EC. (d) x-z cross-section of 3-Stack NSFETs with WAC.

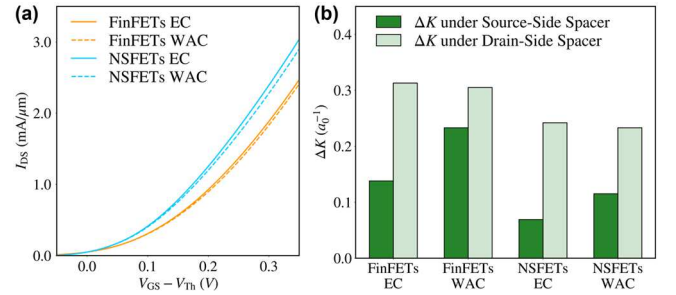


Fig. 3. (a) Transfer characteristics (I_{DS} - V_{GS}) of FinFETs and 3-Stack NSFETs. (b) Momentum Change (ΔK) in the channel regions under the source- and drain-side spacers at the On-state.

only on the outer source- and drain-side faces, along the S-to-D direction. This gives the injection path best aligned with transport, and therefore the least momentum redirection. WAC, by contrast, wraps the top and sidewalls of each S/D pillar. Carriers then enter from the side and bottom faces, and must rotate their momentum by roughly 90° before reaching the channel.

For a fair comparison, EC and WAC have the same contact area, whose value is given in Table I. As a result, any difference in their performance arises solely from how the metal interface is distributed in space and not from a difference in contact area.

III. SIMULATION RESULTS

Contact geometry has a direct impact on how efficiently carriers are injected into the channel. Fig. 2 maps the current density at $V_{GS} = V_{ON}$ for four cases, the FinFETs and NSFETs with EC or WAC. The overlaid arrows give the local current direction, so the route that carriers follow from the S/D into the channel can be read directly from each panel. Under EC, in Fig. 2(a) and (c), the arrows stay aligned with the S-to-D direction and carriers reach the channel along a direct path. Under WAC, in Fig. 2(b) and (d), the arrows bend by roughly 90°, because carriers injects from the side and bottom contact and must reorient before reaching the channel. The redirection scatters the flux near the S/D junction. This behavior is clear in Fig. 2(d), where carriers injected from the top surface are entering the top nanosheet with a comparable 90° redirection.

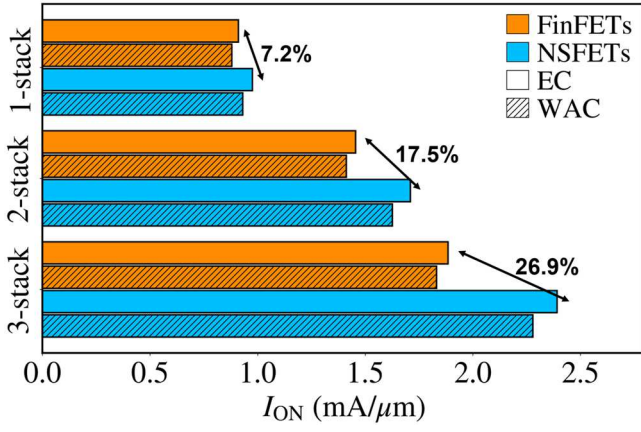


Fig. 4. I_{ON} for FinFETs and 1, 2, 3 Stack NSFETs with EC and WAC.

These geometric differences set the overall I_{ON} ordering $EC > WAC$, which the transfer curves in Fig. 3(a) confirm. For both schemes, NSFETs also delivers a higher I_{ON} than the FinFETs, a difference rooted in the QC orientation of each channel. All devices use a (100) Si wafer with a (110) S-to-D direction, but the channel is thinnest along a different direction in each device, and this thinnest direction sets the primary QC direction. The fin is thin laterally, perpendicular to S-to-D, so it is confined in-plane along (110). Each nanosheet is thin vertically, so it is confined out-of-plane along (100). Along these two directions the Si conduction-band valleys present different QC effective masses (m_{QC}^*), so carriers settle into different lowest valleys in the two devices. Because m_{QC}^* is smaller in the fin, its QC potential and hence its QC effect are stronger. The raised QC potential enhances phonon scattering and gives the fin a higher channel resistance than the nanosheet at equal channel thickness, which explains the consistently larger I_{ON} in NSFETs. This mechanism is further supported by Fig. 3(b) which shows the carrier momentum change (ΔK) as electrons traverse the channel regions underneath the source- and drain-side spacers. Overall, ΔK is larger in FinFETs than in NSFETs, which is consistent with the stronger QC-induced channel resistance of the fin. Beneath the drain-side spacer, ΔK is nearly identical for EC and WAC in each device, as the carrier momentum has already been aligned before entering this region. Beneath the source-side spacer, however, ΔK depends strongly on the contact scheme and is clearly larger for WAC than for EC, indicating the extra momentum redirection that WAC imposes during injection.

Fig. 4 shows the I_{ON} values of FinFETs and NSFETs for the 1-, 2-, and 3-Stack cases under EC and WAC, respectively. The NSFETs-to-FinFETs gap widens monotonically as stacks are added. Under EC, it grows from 7.2% for the 1-Stack device to 17.5% for the 2-Stack and 26.9% for the 3-Stack. The same trend appears under WAC, where the gap increases from 6.8% to 15.4% and 20.5% across the 1-, 2-, and 3-Stack devices. Because the matched S/D dimensions give both architectures similar parasitic resistance, this widening gap stems mainly from the larger channel resistance of FinFETs due to the stronger QC.

Fig. 5 presents how S/D doping modifies the contact-geometry effect [4]. In both FinFETs and NSFETs, the EC-WAC difference in I_{ON} shrinks as the S/D doping rises. Because WAC injects electrons from the side and top of the pillar, those carriers start out misaligned with the S-to-D direction and need a roughly 90° turn to enter the channel. Heavier doping increases the scattering rate, mostly through

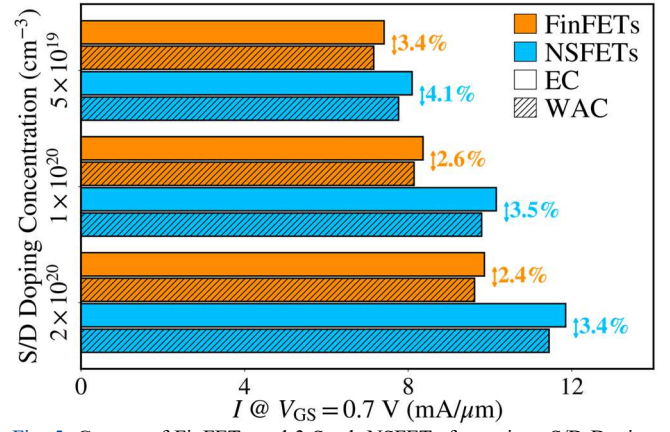


Fig. 5. Current of FinFETs and 3-Stack NSFETs for various S/D Doping Concentration at $V_{GS}=0.7 V$.

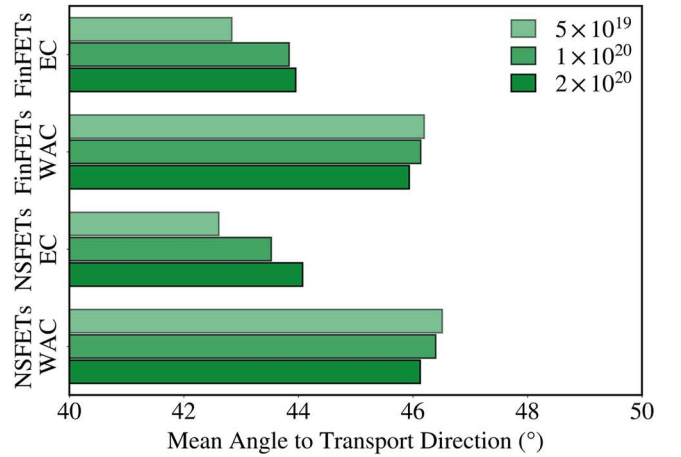


Fig. 6. Mean injection angle of carriers with respect to the S-to-D direction, evaluated at the source/channel boundary, for FinFETs and NSFETs under EC and WAC at S/D doping concentrations of 5×10^{19} , 1×10^{20} , and 2×10^{20} cm⁻³. A smaller angle indicates better alignment with the S-to-D direction.

ionized impurity scattering, and this extra scattering helps supply the redirection that WAC needs. In EC, the carriers are already aligned, so the same added scattering instead degrades their alignment. Heavier doping therefore aids WAC injection but hinders EC injection, which lifts the WAC current toward EC and closes the gap.

Fig. 6 supports this interpretation by reporting the mean injection angle of carriers in FinFETs and NSFETs for EC and WAC, respectively. It represents the average angle between the carrier direction and the S-to-D axis at the source-channel boundary. A smaller value therefore corresponds to better alignment with the S-to-D direction. Raising the S/D doping concentration lowers the angle for WAC yet raises it for EC. These opposite movements mean that alignment improves under WAC and degrades under EC. This behavior agrees directly with the narrowing I_{ON} difference seen in Fig. 5.

EC gives the best injection throughout the analysis so far, yet a perfectly vertical metal-S/D interface is hard to be implemented in practice. Real processes cannot cleanly expose the S/D end face and attach metal to it. Contact plugs are instead formed by etching into the S/D region and refilling the cavity with metal. Such a recessed contact is process-feasible, and the deeper the metal reaches into the S/D, the more its injection path approaches that of the ideal EC. As illustrated in Fig. 7, we describe the recessed contact by three geometric parameters. The recess depth T_M is how far the metal extends vertically into the S/D from the top, the

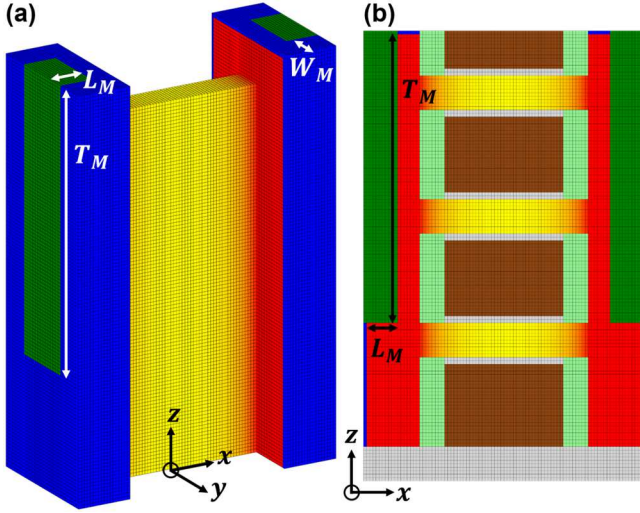


Fig. 7. Recessed contact structure of (a) FinFETs and (b) NSFETs, showing the recess depth T_M , the uncovered sidewall width W_M , and the recessed contact length L_M .

TABLE II

PARAMETERS FOR RECESSED CONTACT FOR FINFETs AND NSFETs

Parameter		FinFETs	NSFETs
Recessed Contact Length	L_M (nm)		5
Recessed Contact Thickness	T_M (nm)	11, 24, 29, 42, 47, 60	
Uncovered Sidewall Width	W_M (nm)		0, 5, 7.5

uncovered sidewall width W_M is the lateral gap left between the metal and the channel sidewall. Lastly, the recessed contact length L_M is the length of the metal plug on S-to-D direction. L_M is fixed at 5 nm here, so the study focuses on the two swept parameters T_M and W_M , which are listed in Table II.

We begin with the recess-depth dependence at $W_M = 0$ nm. The chosen T_M values line up with the vertical edges of the three stacked nanosheets. $T_M = 11$ nm reaches the bottom edge of the top sheet, $T_M = 24$ and 29 nm the top and bottom edges of the middle sheet, and $T_M = 42$ and 47 nm the top and bottom edges of the bottom sheet, while $T_M = 60$ nm runs the metal to the bottom of the S/D pillar. Fig. 8 shows that the T_M differently affect two architectures. In FinFETs, I_{ON} rises smoothly with T_M , since the fin is a vertically continuous channel and a deeper recess steadily improves the injection path. In NSFETs, I_{ON} instead rises in discrete steps. It responds strongly while the metal overlaps a nanosheet vertically, but weakly in the gaps between sheets, where the metal faces no channel.

We next turn to the uncovered sidewall width W_M . The $W_M = 0$ and 5 nm cases have essentially equal contact area, so the current difference between them in Fig. 8 isolates the geometric change. Averaged over all T_M , adding $W_M = 5$ nm costs only about 0.5% of I_{ON} in FinFETs but near 5% in NSFETs. A wider W_M of 5 or 7.5 nm opens the gap between the metal and the channel sidewall and sends a larger share of carriers along the $\pm y$ directions. These carriers need a large momentum change to reach the channel. In NSFETs, the

wider gap removes the direct metal-to-sheet overlap and eliminates the efficient injection path. In FinFETs, the fin sits centered along y and keeps some alignment with the metal even at large W_M . NSFETs therefore loses much more I_{ON} than FinFETs as W_M increases.

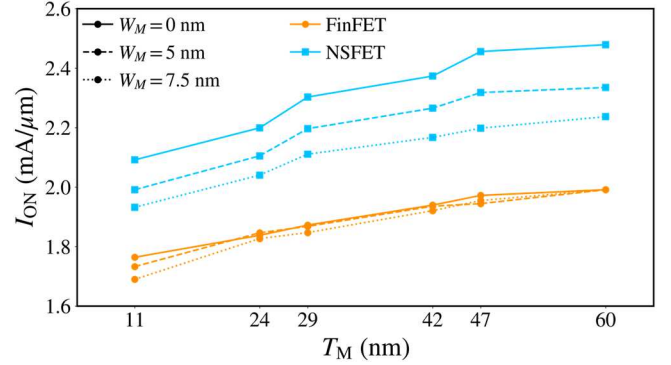


Fig. 8. I_{ON} of FinFETs and NSFETs with recessed contact as a function of T_M and W_M . The simulated T_M values correspond to the vertical boundaries of the channel stacks.

IV. CONCLUSION

This study shows, through SCMC simulation, that contact geometry plays a decisive role in the performance of FinFETs and NSFETs. In WAC, carriers must go through momentum change by roughly 90° turn around to reach the channel, while in EC they arrive already aligned with the S-to-D direction. Heavier S/D doping closes the EC-WAC I_{ON} gap, because the stronger scattering affects WAC more favorably than EC, providing the redirection that WAC needs while degrading the alignment that EC already has. The recessed-contact sweeps over T_M and W_M further show that greater overlap between the metal and the channel cross-section is preferable, as carriers then enter the channel more directly. Taken together, these results identify contact geometry as a major factor in setting the S/D junction resistance. With continued vertical scaling through nanosheet stacking, contact geometry importance will grow as a key design parameter.

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