

Hot Carriers and Self-Heating Effects in FD-SOI Devices at Cryogenic Temperatures

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Abstract—The goal of this work is to understand the role of self-heating on the high-energy tail of the carrier energy distribution function in the drain end of the channel in FD-SOI devices. We find that self-heating enhances phonon absorption processes, which in turn lead to some carriers having an energy that is higher when compared to the isothermal case. These carriers may cause reliability concerns in nanoscale device structures.

Index Terms—Cryogenic FD-SOI, Self-heating, Monte Carlo device simulation, Device reliability, Phonon transport.

I. INTRODUCTION

The rapid advancement of quantum computing has accelerated interest in cryogenic electronics to enable efficient control and readout of qubits at extremely low temperatures. Nanoscale fully depleted Silicon-on-insulator (FD-SOI) devices are particularly promising for readout circuits in quantum computing applications due to their excellent electrostatic control, which reduces leakage currents. However, the impact of self-heating effects is amplified at cryogenic temperatures due to the poor thermal conductivity of the underlying buried oxide (BOX) layer. Localized heating reduces the on-current (I_{on}) and also leads to population of higher energy states of the position-dependent non-equilibrium distribution function. The latter can give rise to reliability concerns.

Modeling hot carriers and their impact on device degradation (HCD) involves three key steps: (1) simulation of carrier transport coupled with phonon transport, (2) calculation of defect generation rates, and (3) modeling of device degradation [1]. In this work, we focus on the first step, employing a hybrid approach [2] in which electron dynamics are calculated via Monte Carlo (MC) solution of the Boltzmann Transport Equation (BTE). The phonon dynamics are captured through the energy balance model for both acoustic and optical phonon populations.

The paper is organized as follows. Section II contains the description of the theoretical device model implemented in the in-house 2D self-consistent electro-thermal Monte Carlo device simulator. The simulation results are presented in

Section III. Conclusions derived from this work are presented in Section IV.

II. ELECTRO-THERMAL SOLVER

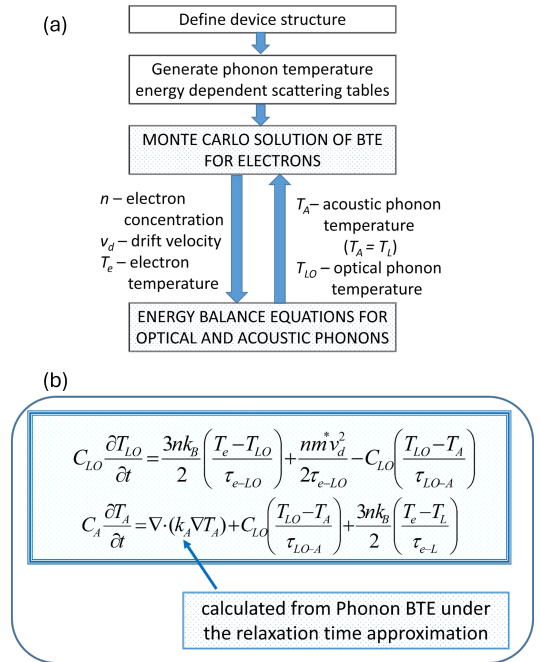


Fig. 1. Electro-thermal device simulator: (a) Exchange of variables between the two kernels. Note that the phonon temperature-energy-dependent scattering tables are generated as a preprocessing scheme before device simulation starts. (b) Energy balance equation for optical and acoustic phonons—the lattice temperature, T_L , is estimated as equivalent to T_A . C_{LO} and C_A represent the heat capacity of optical and acoustic phonons, respectively, and k_A is the thermal conductivity.

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populations (Fig. 1). Because SOI devices consist of two distinct regions — the silicon device layer and the buried oxide layer, the energy balance equations for optical and acoustic phonons are solved in the silicon layer to accurately model the heat transport, but the simple heat diffusion equation is used in the amorphous BOX. The two distinct computational regions are coupled through interface conditions that account for differences in material properties.

The simulations are initialized from the ambient temperature, with the acoustic and optical phonon temperatures initially set to the lattice temperature. At the contacts, carrier injection is treated using equilibrium carrier statistics corresponding to the applied terminal biases, while the electrostatic potential is fixed by the source, drain, and gate voltages. For the thermal problem, the external boundaries are maintained at the ambient temperature, and the silicon/BOX interface is coupled through heat-flux continuity using the corresponding material properties. The electron and phonon solvers are then updated iteratively until the carrier quantities, local phonon temperatures, and terminal current reach a stable self-consistent solution [2]–[4].

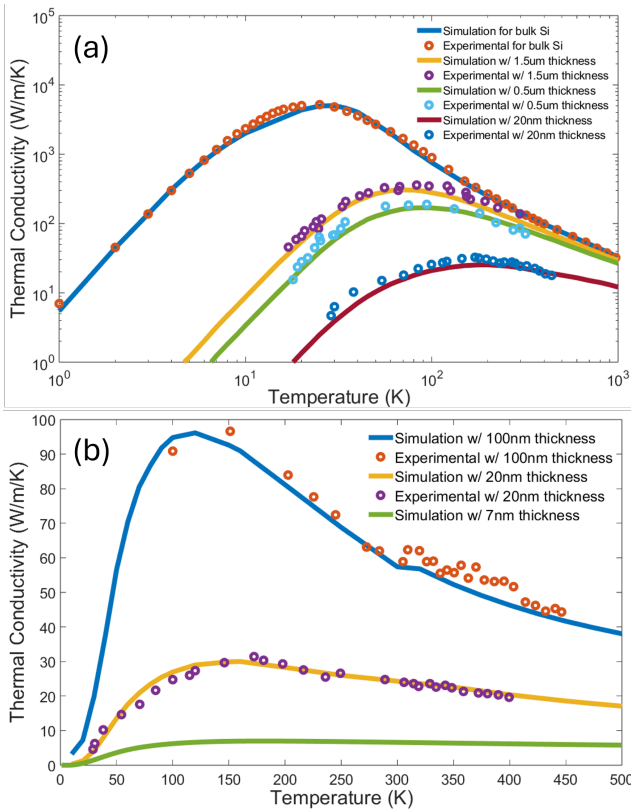


Fig. 2. (a) Temperature-dependent thermal conductivity of several different SOI-based silicon structures: bulk material and thin silicon films. (b) Comparison of the calculated thermal conductivity data for thin silicon films of 7 nm with available experimental data and corresponding theoretical calculations for silicon films with thicknesses of 20 nm and 100 nm.

The primary path of energy transport is represented first by scattering between electrons and optical phonons (T_{LO})

and then optical phonons to the lattice (T_A). The BTE for both kinds of phonons is used to provide the energy balance of the process. The temperature dependence of the thermal conductivity of the silicon thin film is obtained by solving the phonon BTE under the relaxation-time approximation. This incorporates full phonon dispersion relations and momentum-dependent boundary scattering, as well as three-phonon and isotope scattering mechanisms [3]. For 7 nm thick silicon films, phonon boundary scattering and interface roughness ultimately limit the thermal conductivity to values below 10 W/m-K (see simulation results from Fig. 2). At cryogenic temperatures, we also account for the reduction of the specific heat capacity and the partial ionization of dopants [4]. The simulator's predictive capability is validated against available experimental data from Ref. [5].

III. RESULTS AND DISCUSSIONS

The device structure being investigated in this study is a 28 nm technology node, an FD-SOI device with an effective gate length of 30 nm [5]. The gate stack is modeled as a single layer of SiO_2 with an effective oxide thickness of 1.2 nm. The silicon film thickness is 7 nm, and the buried oxide layer is 25 nm. A schematic of this device structure is shown in Fig. 3. The doping of the source and the drain regions is taken to be 5×10^{19} , which is a factor of two lower than the actual doping. In this way, we reduce the total number of particles being simulated to speed up the calculations at the expense of the introduction of a small series resistance effect.

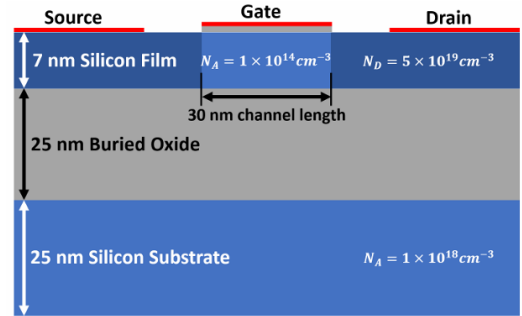


Fig. 3. Schematic description of the FDSOI device structure being investigated in this study [5]. It is a 28 nm technology node with a physical gate length of 30 nm. The effective gate oxide thickness is 1.2 nm.

The device transfer characteristics at $T = 4.2 \text{ K}$, 77 K , and 300 K are shown in Fig. 4. We observe two important effects: (1) an increase in the threshold voltage with a decrease in temperature due to partial ionization of the dopants, and (2) degradation of the current due to self-heating that leads to increased phonon scattering. This is clearly seen from the results as shown in Fig. 5.

The role of self-heating and non-equilibrium phonons is illustrated in Fig. 6, where it is seen that energy transfer from the electron gas to the phonon gas is larger in the thermal simulation.

At high temperatures, it is defined by the balance between phonon absorption and emission. In the equilibrium case, the

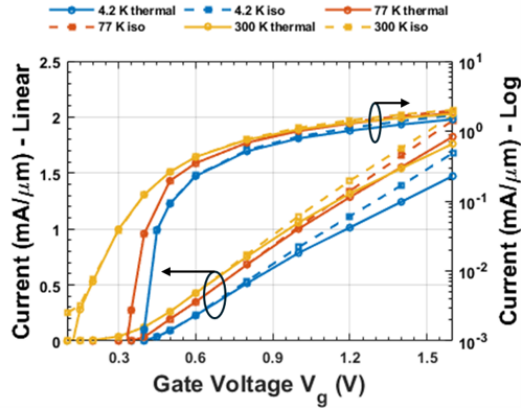


Fig. 4. Transfer Characteristics for $V_{DS} = 1.2V$ and $T = 4.2K, 77K$, and $300K$ on the linear and logarithmic scale. Solid lines are the thermal calculations, and dashed lines represent isothermal simulation results.

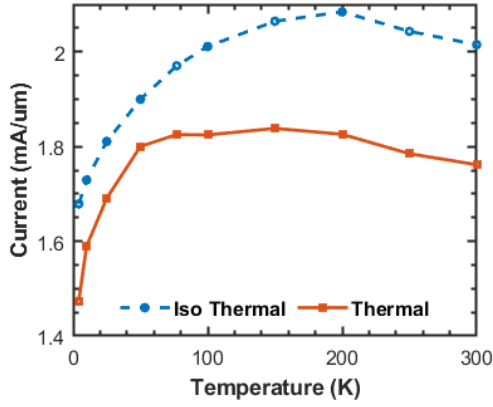


Fig. 5. On-Current degradation due to self-heating effects as a function of the ambient temperature. Notice the significant degradation at cryogenic temperatures due to self-heating and partial ionization of the dopants. The increase in the degradation at higher temperatures is due to the increase in phonon scattering, which is further enhanced due to lattice heating. The applied biases are $V_{GS} = V_{DS} = 1.2V$.

processes balance each other, so the energy flux is zero. In the non-equilibrium case, the phonon emission dominates. Fig. 6 also depicts that in the low temperature regime, the energy loss is based on the number of phonons.

The same is confirmed in Fig. 7 as well, where the electron distribution function deviates from the equilibrium Fermi-Dirac statistics more in the thermal than in the isothermal simulation, thus leading to larger energy loss. The high temperature difference (Fig. 4) is most pronounced at the drain because the deviation of electron distribution is the largest in this region. The low temperature difference is caused by the non-equilibrium phonon distribution. Therefore, at cryogenic temperatures, self-heating and non-equilibrium phonons must be accounted for to accurately describe FD-SOI device operation.

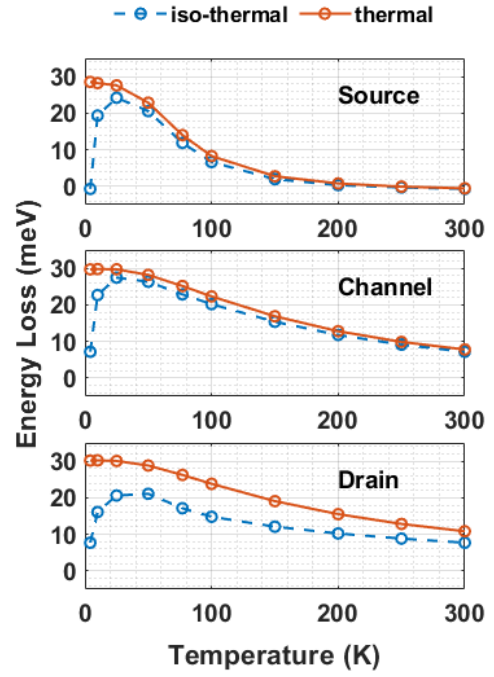


Fig. 6. Net energy loss of the carriers to the lattice as a function of ambient temperature for the source, channel, and drain sections of the device.

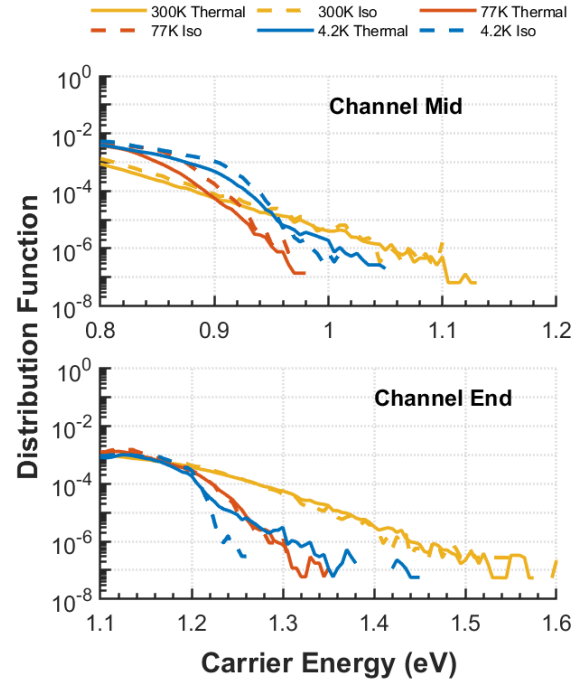


Fig. 7. Non-equilibrium electron distribution function tails at the middle and end of the channel at $V_{GS} = V_{DS} = 1.2V$. The application of high drain voltage gives rise to very energetic carriers at the drain end of the channel. As expected, at $300K$ we have more energetic carriers than at $77K$ and $4.2K$. Notice also that the tail of the distribution function is more populated at $4.2K$ than at $77K$. The increase in the high-energy tail of the distribution function due to self-heating is caused by the increased phonon absorption.

CONCLUSIONS

In summary, this work examines self-heating in FD-SOI devices at cryogenic temperatures using a Monte-Carlo device simulator self-consistently coupled to an energy-balanced approach for the phonon bath. The buried oxide layer limits heat removal from the thin silicon film, so the local phonon system can deviate from the ambient temperature. This changes the energy exchange between electrons and phonons and alters the non-equilibrium electron distribution function. The results show that cryogenic operation cannot be described using only an isothermal transport model, especially when non-equilibrium phonons and partial dopant ionization are important. Overall, this work shows that reliability modeling requires attention to the full electron energy distribution function rather than only average transport quantities.

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