

Double-Gate LDMOS Transistors with Exceptional Figure-of-Merit Exceeding 700 kW/mm²

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ABSTRACT— This paper reports a Bayesian-optimization (BO) driven TCAD study of a double-gate LDMOS transistor structured to emulate a nanosheet gate-all-around geometry, aimed at replacing hand-tuned device design with an automated six-parameter search. The resulting device reaches a specific on-resistance of 0.17 mΩ·mm² at 11.32 V breakdown voltage, a Baliga figure of merit of 738 kW/mm², more than five times a conventional planar LDMOS baseline. Benchmarked directly against a manually optimized planar LDMOS device, the dual-gate structure is shown to ease the usual BV- $R_{sp,on}$ trade-off through better lateral current spreading, supporting nanosheet-style double-gate transistors as a viable steppingstone toward full 3D Gate-All-Around LDMOS.

INDEX TERMS— Bayesian optimization, Double-Gate LDMOS, figure-of-merit, specific on-resistance.

I. INTRODUCTION

Power-management ICs built in BCD (Bipolar-CMOS-DMOS) processes rely heavily on the LDMOS transistor for its low conduction loss, fast switching, and native compatibility with CMOS flows. Because current flows laterally rather than vertically, LDMOS geometry gives designers direct control over the drift and channel regions, which is what allows one device family to cover such a broad voltage range [1-2]. That same lateral geometry, however, becomes a liability as dimensions shrink short-channel effects intensify and off-state leakage (I_{leak}) climbs [3].

This gain in electrostatic control matters because power-device performance ultimately reduces to a trade-off between two numbers: breakdown voltage (BV) and on-resistance ($R_{ds,on}$) [4]. Raising BV means giving the drift region more length and a doping profile graded to satisfy the RESURF condition [5]; lowering $R_{ds,on}$ means doing the opposite, shrinking length and, secondarily, narrowing width. Since both dimensions scale with area, the two pull in different directions on the specific on-resistance $R_{sp,on} = R_{ds,on} \times \text{Area}$, and reconciling them, while staying within leakage and reliability limits, is what makes DG electrostatic design difficult [6-7].

Recently, machine learning (ML) algorithms have become increasingly proficient at detecting complex patterns and relationships within large datasets that are often beyond human capabilities and understanding. Given enough TCAD or measured data, such a model can associate doping, geometry, and material choices with the resulting device behavior well enough to search multi-objective trade-offs without brute-force simulation of every candidate, turning device design from trial-and-error into a guided search [8].

This study pushes a 2D DG-LDMOS through six-parameter Bayesian optimization (BO) to a FOM of 738 kW/mm², more than five times a typical planar result, promising future direction of Gate-All-Around (GAA) LDMOS devices.

The optimized device simultaneously maintains high BV and ultra-low $R_{sp,on}$, setting a new performance point in the BV-FOM landscape and demonstrating the clear advantage of integrating Bayesian optimization with DG-LDMOS design.

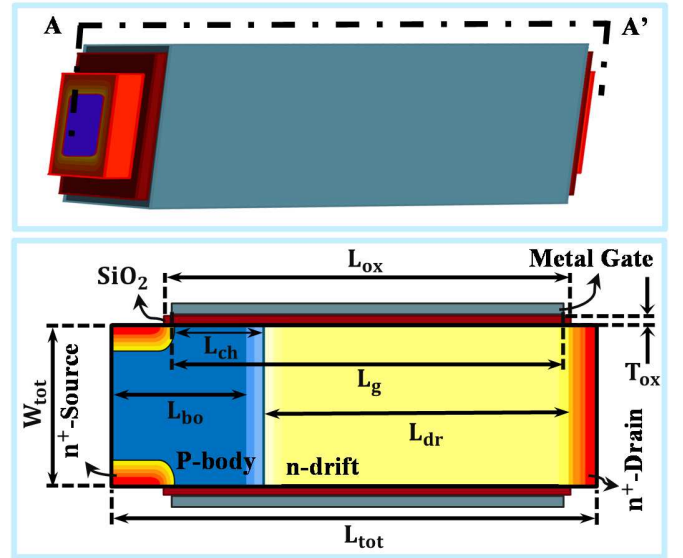


FIGURE 1. (a) The proposed 3D GAA-LDMOS showing A-A' cross-section representing our studied DG-LDMOS. (b) A-A' Cross-sectional view of the optimized DG-LDMOS structure corresponding to the highest FOM reported in this work, showing top and bottom 12 nm SiO₂ gate dielectrics and metal gates symmetrically controlling the channel within a 2D TCAD framework. Gaussian doping profiles are applied in the source, drain, drift, and body regions.

II. SIMULATION AND OPTIMIZATION

The target geometry is the 3D GAA-LDMOS sketched in Figure 1a. This paper works with its A-A' cross-section, shown in Figure 1b, modeled as a 2D DG-LDMOS. Mirrored top and bottom gates stand in for the wraparound gate of the full GAA structure, giving a tractable 2D proxy for its electrostatics while isolating the channel and drift regions on each side. Gate metal is aluminum with a 4.1 eV work function, consistent with an n-type device.

Channel length in this structure is not an independent parameter; it emerges from geometry. A 12 nm SiO₂ dielectric separates each gate from a p-body doped to N_p , and the lateral extent of the channel is fixed by two overlapping extensions: L_{bo} on the p-body side, L_{dr} on the drift side. Both depend on N_p and N_d , but only L_{dr} actually varies in this study, since L_{bo} is fixed in place to preserve a consistent body-drift overlap. Practically, then, channel length

and the depletion geometry around it track L_{dr} , N_p , and N_d directly.

TCAD simulations use a validated commercial 2D drift-diffusion solver [9]. Recombination is handled via doping-dependent SRH lifetimes together with Auger recombination; avalanche behavior follows the Van Overstraeten impact-ionization model [10]; and carrier transport accounts for field- and doping-dependent mobility degradation, bandgap narrowing, and Fermi-Dirac carrier statistics.

Doping in the p-body, n-drift, source, and drain regions follows Gaussian profiles, the standard TCAD approximation for implanted-and-annealed junctions [11]. A high-graded concentration in the p-body keeps the channel under tight electrostatic control, while a light-graded n-drift profile spreads the electric field and helps push BV higher without creating localized peaks. Together these choices give a physically realistic leakage baseline against which the BV- $R_{sp,on}$ trade-off can be optimized.

All four bias points follow a fixed convention: BV is read at avalanche under $V_{GS} = V_{BS} = V_{SS} = 0$ V, I_{leak} at $V_{GS} = 0$ V, $V_{DS} = 5$ V, and $R_{ds,on}$ from V_{DS}/I_{DS} at $V_{GS} = 5$ V, $V_{DS} = 0.1$ V. From there, $R_{sp,on} = R_{ds,on} \times L_{tot}$, L_{tot} being the source-to-drain half pitch, and $FOM = BV^2/R_{sp,on}$ (kW/mm²) follow directly.

Sign	Descriptions	Bounds	Sign	Descriptions	Bounds
L_{tot}	Device length	400 – 800 nm	L_g	Gate length	300 – 700 nm
W_{tot}	Device width	200 – 400 nm	N_p	Body doping concentration	$(0.7-3) \times 10^{18} \text{ cm}^{-3}$
L_{dr}	Drift region extension length	300 – 680 nm	N_d	Drift doping concentration	$(0.8-8) \times 10^{17} \text{ cm}^{-3}$

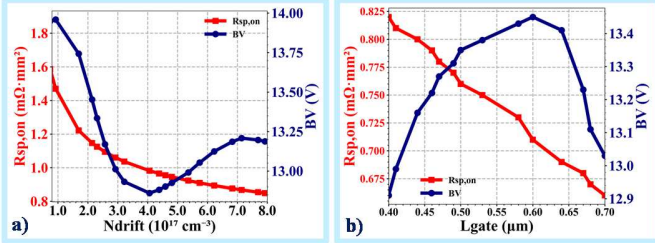


FIGURE 2. (a) Independent effect of N_d on the BV- $R_{sp,on}$ trade-off. (b) Independent effect of L_g on the BV- $R_{sp,on}$ trade-off. **TABLE 1:** Symbols, descriptions, and bounds of the six input parameters used in this work.

Before turning to full BO, N_d and L_g are swept one at a time in TCAD to build intuition for their individual effect on BV and $R_{sp,on}$ (Figure 2a,b). L_{tot} , W_{tot} , L_{dr} , and N_p are held at 800 nm, 200 nm, 550 nm, and $2 \times 10^{18} \text{ cm}^{-3}$, respectively, throughout. During the N_d sweep L_g is fixed at 680 nm, during the L_g sweep N_d is fixed at $3 \times 10^{17} \text{ cm}^{-3}$.

The BO objective function is Baliga's figure of merit (FOM) [12], written as:

$$f(x) = FOM = BV^2/RSP \quad (1)$$

This six-element vector $x = [L_{tot}, W_{tot}, L_{dr}, L_g, N_p, N_d]$ is what BO searches over. Rather than evaluating FOM directly at every candidate, which would mean a full TCAD run each time, a Gaussian Process (GP) model is trained to approximate it cheaply, and an Expected Improvement (EI) acquisition function decides which point to try next, balancing exploration against

exploitation so that strong designs turn up in far fewer TCAD calls than an exhaustive search would need x . These six parameters, listed with their bounds in the table accompanying Figure 2, fully specify the DG-LDMOS geometry and electrostatics that BO is allowed to vary x .

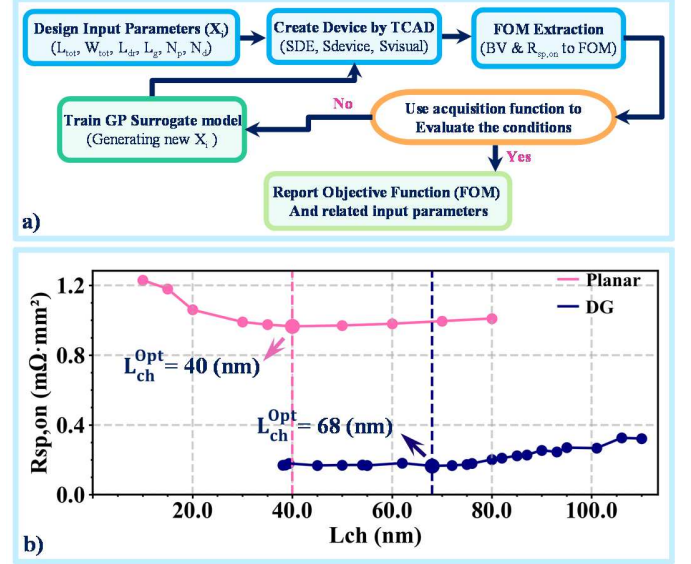


FIGURE 3. (a) BO-TCAD Optimization Flowchart. (b) Specific on-resistance $R_{sp,on}$ versus length of the channel (L_{ch}) for 5V optimized DG-LDMOS (blue) and planar LDMOS (pink), showing a notable $R_{sp,on}$ reduction to 0.17 mΩ·mm² at $L_{ch} = 68$ nm.

The optimization framework combines Bayesian optimization (BO) with TCAD simulations to identify optimal DG-LDMOS design parameters, as shown in Figure 3. Each run begins from 20 uniformly sampled, space-filling seed points spanning all six structural parameters (L_{tot} , W_{tot} , L_{dr} , L_g , N_p , and N_d), each evaluated in TCAD to fit an initial GP surrogate of FOM. EI then proposes new candidates that balance exploring uncertain regions against exploiting known good ones, with each proposal simulated and folded back into the surrogate [13-14].

III. RESULTS AND DISCUSSION

Figure 4 presents the 250 BO iterations for the full six-parameter optimization space (L_{tot} , W_{tot} , L_{dr} , L_g , N_p , and N_d). The BV-FOM distribution in Figure 4a shows that jointly tuning all six structural parameters drives the performance frontier upward, with FOM values exceeding 700 kW/mm² and reaching a peak of 738 kW/mm² while maintaining acceptable BV. The dashed convex hull in Figure 4a highlights the performance boundary achieved through this high-dimensional optimization, illustrating how the broadened design space enables the BO algorithm to push the attainable BV-FOM frontier to higher values.

$R_{sp,on}$ tells the same story from the other side (Figure 4b): the highest-FOM points cluster at the lowest $R_{sp,on}$, confirming that BV and $R_{sp,on}$ are improving together rather than trading off. The zoomed inset in the lower-left corner emphasizes $R_{sp,on}$ values below 1.0 mΩ·mm², increasingly achieved with higher-dimensional optimization.

Taken together, these results show BO efficiently navigating a genuinely multi-parameter design space, converging on high-

performance configurations far faster than exhaustive TCAD sweeps could.

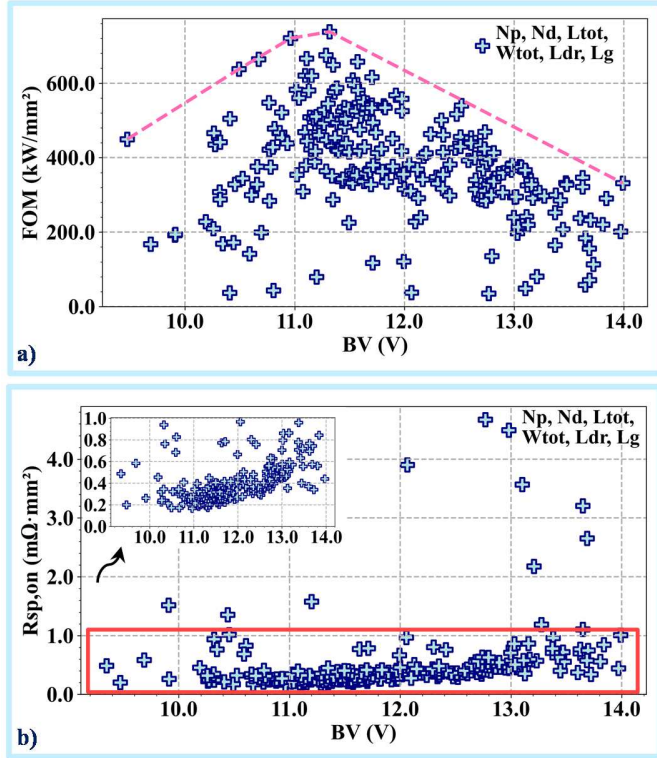


FIGURE 4. (a). FOM versus BV for the six-parameter group, with the convex hull showing the expanded optimization envelope. (b) $R_{sp,on}$ versus BV for the same six-parameter group, highlighting the reduced resistance achieved through multi-parameter optimization.

A second comparison, shown in Figure 3b, plots $R_{sp,on}$ against channel length L_{ch} for the strongest BO-identified DG-LDMOS devices and compares them with the planar LDMOS baseline. $R_{sp,on}$ reaches a minimum for the DG device $L_{ch} = 68$ nm, roughly a fivefold reduction from the planar optimum, without sacrificing BV [15]. This minimum does not occur at the shortest available L_{ch} : classical MOSFET scaling would predict resistance to increase with channel length [16]. Indeed, all DG-LDMOS designs remain below 0.4 mΩ·mm² regardless of L_{ch} , whereas the planar device never comes within a factor of two of that minimum, even at much shorter L_{ch} . This gap reflects the greater electrostatic headroom provided by the dual-gate structure and how effectively BO exploits it to push beyond the conventional BV- $R_{sp,on}$ trade-off.

Figure 5 breaks down the origin of this headroom by comparing the electrostatics and current transport at the 738 kW/mm² operating point. In the full DG-LDMOS (Figure 5a-5c), the electric field remains smooth along the drift region, with only mild peaking near the drain, a sign that the dual gates share the field-shaping role rather than allowing the field to concentrate at a single junction.

That same field shaping carries over to the half DG-LDMOS (Figure 5a'-5c'), which keeps the suppressed drain crowding and spread-out impact ionization but loses roughly half the

conduction cross-section; its $R_{sp,on}$ rises to about 0.35 mΩ·mm², close to double the full device's, exactly as expected if the benefit scales with the number of active conduction channels rather than with any geometric side-effect.

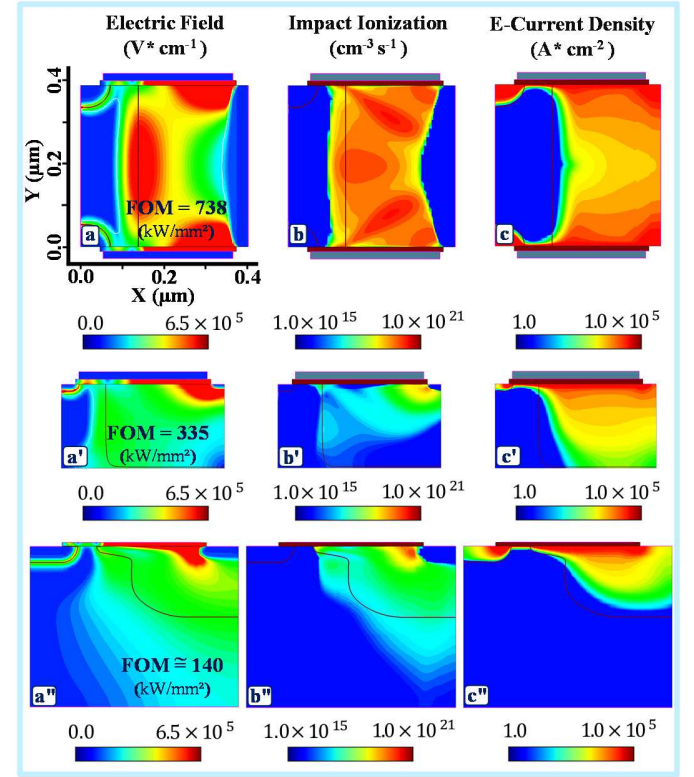


FIGURE 5. Electric-field distribution (a-a''), impact ionization profile (b-b''), and electron current density (c-c'') of the full DG-LDMOS (top row), half DG-LDMOS (middle row), and conventional planar LDMOS (bottom row) at the breakdown condition ($V_{GS} = 0$ V). The DG-LDMOS structures exhibit reduced drain-side field crowding, distributed impact ionization, and vertically distributed current transport at on-state ($V_{GS} = 5$ V and $V_{DS} = 0.1$ V), resulting in progressively enhanced FOM compared with the conventional LDMOS.

The conventional planar LDMOS (Figure 5a''-5c'') behaves quite differently: field crowding concentrates at the drain, impact ionization localizes there too, and current is confined to a thin surface channel, all of which drive up drift resistance. FOM tracks this progression directly, 140 kW/mm² for the planar device, 335 kW/mm² for the half DG-LDMOS, and 738 kW/mm² for the full DG-LDMOS, tying the improvement squarely to the added conduction paths and field relief that the dual-gate structure provides.

IV. CONCLUSION

We obtained $R_{sp,on}$ of 0.17 mΩ·mm² at a channel length of 68 nm for an 11.32 V breakdown voltage device, while keeping leakage current below 1×10^{-13} A/μm for 5 V power DG-LDMOS applications, yielding a Baliga FOM of 738 kW/mm². This high FOM reflects an excellent balance between breakdown voltage and specific on-resistance, highlighting the effective use of advanced machine learning techniques, specifically Bayesian optimization, device's efficiency and power application potential.

REFERENCES

- [1] A. Flandre, C. Detcherrey, P. G. A. Jespers, and J.-P. Colinge, "BCD (bipolar–CMOS–DMOS) technology trends for power management integrated circuits," *Microelectronics Journal*, vol. 34, no. 4, pp. 313–319, Apr. 2003.
- [2] STMicroelectronics, Understanding LDMOS Device Fundamentals, Application Note AN1629, 2006. [Online]. Available: https://www.st.com/resource/en/application_note/cd00004124-understanding-lmos-device-fundamentals-stmicroelectronics.pdf
- [3] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, and Y. Taur, "Device scaling limits of silicon MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001, doi: 10.1109/5.915374.
- [4] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455–457, Oct. 1989, doi: 10.1109/55.43098.
- [5] J. A. Appels and H. M. J. Vaes, "High-voltage thin-layer devices (RESURF devices)," in *Tech. Dig. Int. Electron Devices Meeting (IEDM)*, Washington, DC, USA, 1979, pp. 238–241, doi: 10.1109/IEDM.1979.189468.
- [6] P.-J. Chuang, A. Saadat, S. Ghazvini, H. Edwards, and W. G. Vandenberghe, "Determining the performance limits of lateral double-diffused MOSFETs with three common types of field oxides," *IEEE Transactions on Electron Devices*, vol. 71, no. 4, pp. 2315–2321, Apr. 2024, doi: 10.1109/TED.2024.3370133.
- [7] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*. New York, NY, USA: Springer, 2008, doi: 10.1007/978-0-387-71752-4.
- [8] S. Ghazvini, G. Schuppener, W. Fan, S. Ramaswamy, and W. G. Vandenberghe, "Design and optimization of silicon avalanche photodiodes with desired breakdown voltage using Bayesian optimization," *IEEE Transactions on Electron Devices*, vol. 72, no. 5, pp. 2424–2430, May 2025, doi: 10.1109/TED.2025.3552537.
- [9] Synopsys, *Sentaurus Device User Guide*. Mountain View, CA, USA: Synopsys Inc., 2023.
- [10] R. van Overstraeten and H. de Man, "Measurement of the ionization rates in diffused silicon p–n junctions," *Solid-State Electronics*, vol. 13, no. 5, pp. 583–608, May 1970, doi: 10.1016/0038-1101(70)90139-5.
- [11] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice, and Modeling*. Upper Saddle River, NJ, USA: Prentice Hall, 1999.
- [12] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455–457, Oct. 1989, doi: 10.1109/55.43098.
- [13] P.-J. Chuang, A. Saadat, S. Ghazvini, H. Edwards, and W. G. Vandenberghe, "Constrained Bayesian Optimization Using a Lagrange Multiplier Applied to Power Transistor Design," *arXiv:2308.09612*, Aug. 2023.
- [14] A. Saadat, M. L. van de Put, H. Edwards, and W. G. Vandenberghe, "Channel length optimization for planar LDMOS field-effect transistors for low-voltage power applications," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 711–715, Jul. 2020, doi: 10.1109/JEDS.2020.3008388.
- [15] A. Saadat, M. L. van de Put, H. Edwards, and W. G. Vandenberghe, "Channel length optimization for planar lateral double-diffused MOSFETs for low-voltage power applications," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 711–715, Jul. 2020, doi: 10.1109/JEDS.2020.3008388.
- [16] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.