

SOI PeDMOS R_{ON} -BV- I_{OFF} tradeoff optimization through TCAD simulations

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Abstract—In this work, we investigate thin Silicon-On-Insulator P-type extended drain MOSFET (PeDMOS) performances, through TCAD simulations. Layout and technological parameter impact on ON-resistance, Breakdown Voltage and leakage current tradeoff (R_{ON} -BV- I_{OFF}) is evaluated thanks to TCAD simulations calibrated on experimental data. From this sensitivity analysis, optimization tracks for PeDMOS are defined and we demonstrate that the experimentally evidenced P-type Extended Drain MOSFET can be scaled and its resistance can be reduced by a factor 2.5 with a moderate leakage current increase while the electric field lateral distribution at high drain voltage V_{DS} indicates that the breakdown voltage should be unaffected.

Keywords— Extended Drain MOS, TCAD, SOI, Resistance, leakage, breakdown

I. INTRODUCTION

The extended drain MOSFET (eDMOS) is an asymmetric device generally used in the applications where a high voltage needs to be sustained on the drain. P-type eDMOS on thin SOI (23 nm Si – 25 nm BOX, highly doped N-type Ground Plane (GP) with a SiO₂ polysilicon gate stack (EOT=5.6 nm)) functionality was demonstrated in **Error! Reference source not found.** with a channel length L_{ch} =230 nm, a channel doping fixed to achieve threshold voltage around -0.5V and various extension doping ($N_{ext,i}$) to modulate the performance. The breakdown voltage (BV) is higher than 17 V, while the ON-Resistance R_{ON} (extracted at V_{GS} =-2.5 V and V_{DS} =-0.1 V) multiplied by the surface R_{ONS} is lowered down to 7.5 m Ω .mm² with a leakage current I_{OFF} =2 pA/ μ m (V_{GS} =0V, V_{DS} =-7 V). As the Si film is relatively thick, the device operation in not fully depleted but dynamically depleted operation: at V_{DS} Floating Body effects occur [2]**Error! Reference source not found.** It was shown in **Error! Reference source not found.** that the experimental characterization of the processed PeDMOS devices reveals a competitive performance compared to body-contacted partially-depleted PeDMOS [3] (same breakdown voltage with a reduced resistance (-50%)). However, despite the higher breakdown voltage compared to N-type fully depleted eDMOS [4], the resistance of the analyzed P-eDMOS is still higher. This is mainly caused by the lower mobility of holes compared to electrons. The objective of this paper is to investigate the optimization paths through TCAD simulations in order to improve the PeDMOS performance, thanks to the analyze of the layout and technological parameters impact on the three figures of merit: resistance, leakage and breakdown voltage.

II. DEVICE PRESENTATION AND TCAD CALIBRATION

P-type Extended Drain MOSFET “PeDMOS” on thin SOI (23nm Si – 25nm BOX, highly doped N-type Ground Plane “GP”) with a SiO₂ polysilicon gate stack (EOT=5.6nm)

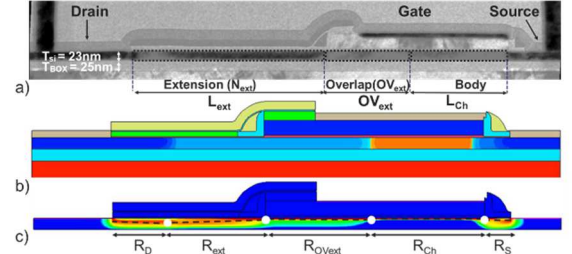


Fig. 1. a. p-EDMOS TEM cross-section, b. TCAD simulated structure. c. Current trajectory at V_{GS} =-2.5V and V_{DS} =-0.1V with resistance components

functionality was shown in [1]. Optimal performance is demonstrated for the shorter available device: gate length L_G =430nm (overlap OV_{ext} =200nm and channel length L_{ch} =230nm) extension length L_{ext} =200nm with Breakdown Voltage $BV > 17V$, ON-resistance R_{ONS} =7.5m Ω .mm² (extracted at V_{GS} =-2.5V and V_{DS} =-0.1V and multiplied by device surface S) I_{OFF} =2pA/ μ m (V_{GS} =0V, V_{DS} =-7V). Using this device as the reference (REF), we use TCAD [5] to optimize PeDMOS performance with more aggressive design rules. We start from SOI pMOS TCAD described in [6] which demonstrated process and device calibration based on electrical and physical characterization. Then we add specific eDMOS process steps (extension doping and SIPROT formation to avoid extension silicidation). The morphology is checked against TEM cross-section (Fig. 1, from [1]). 2D TCAD device simulations are first performed with Drift-Diffusion model, Poisson equation, and IALMob mobility to account for mobility dependence with doping [7]. From comparison with PeDMOS I_{DS} - V_{GS} measurement in linear regime (V_{DS} =-0.1V), we demonstrate that the threshold voltage V_{th} is well predicted by TCAD, but mobility need to be reduced by 20% to match the drain current on the complete characteristic (black curve, Fig. 2) and to reproduce R_{ON} variation with extension doping N_{ext} and length L_{ext} (Fig. 3,

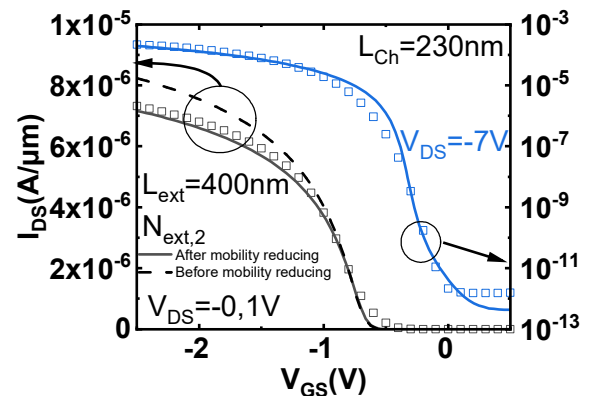


Fig. 2. I_{DS} - V_{GS} in linear and saturation regime before and after transport calibration

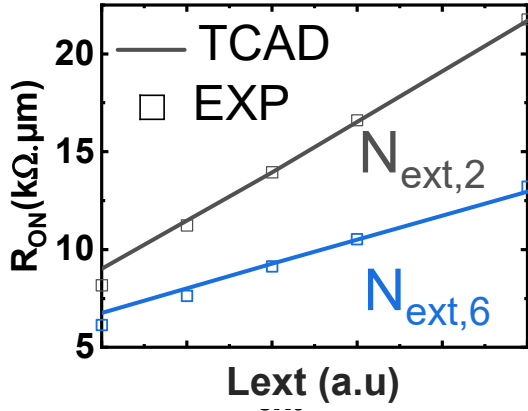


Fig. 5. $R_{ON}(L_{ext})$ from calibrated TCAD and measurement

$N_{ext,i} > N_{ext,j}$ for $i > j$). Mobility parameter adjustment is required to compensate TCAD misaccuracy in extension doping vertical distribution and/or the presence of charges in SIPROT stack which increase resistivity. For saturation regime ($V_{DS} = -7V$), we use the same setting and model parameters as pMOS [6]: Schenk Band-to-Band tunneling (B2B) [8] and Shockley–Read–Hall Recombination (SRH) with electric field enhancement [9]. Indeed, as shown in [1] PeDMOS Gate Induced Drain Leakage (GIDL) is a combination of B2B and SRH, both proportional to electrical field E . For floating body effects, we activate van Overstraeten – de Man impact ionization model in reducing impact ionization rate by a factor of 100 (as for pMOS [6]). PeDMOS saturation regime is validated by comparison with $I_{DS}-V_{GS}$ measurement at $V_{DS} = -7V$ (blue curve, Fig. 2).

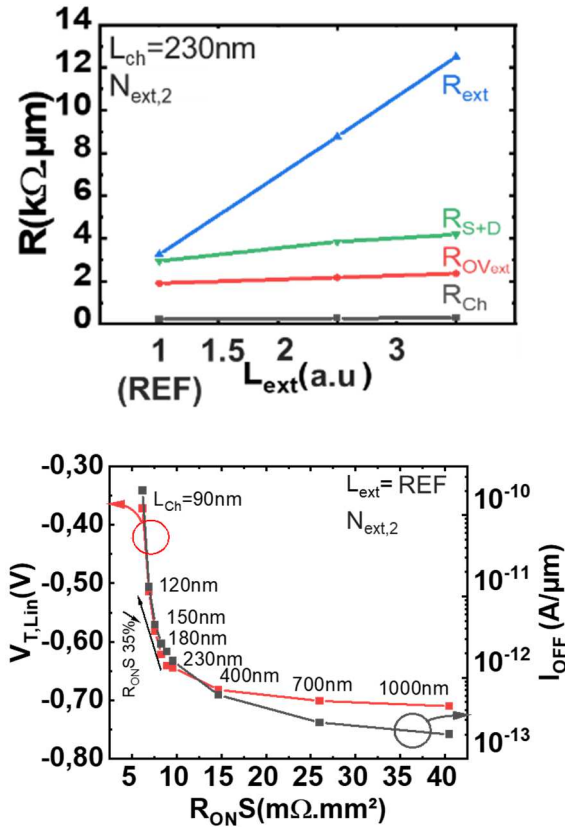


Fig. 3. $V_{T,lin}$ and I_{OFF} $R_{ON}S$ for several channel lengths L_{ch}

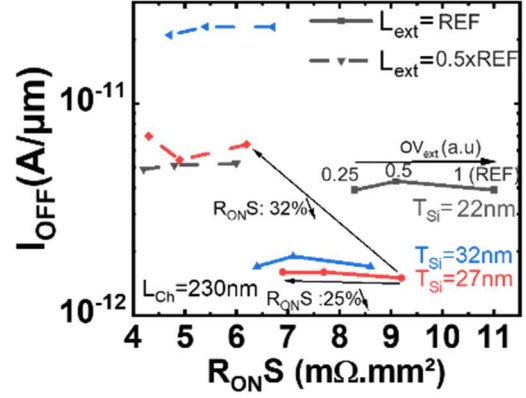


Fig. 6. L_{ext} , OV_{ext} and T_{Si} impact on $I_{OFF} / R_{ON}S$ for $L_{ch} = 230nm$

III. RESISTANCE OPTIMIZATION AND IMPACT ON LEAKAGE

Resistance breakdown is performed thanks to QuasiFermiLevel (QFL) extraction along current path as in [10] for FDSOI transistor. QFL are extracted at $V_{DS} = -0.1V$ and $V_{GS} = -2.5V$ on white dots of Fig. 1-c to evaluate the different resistance components. Each component is plotted for L_{ext} variation (for $N_{ext,2}$, Fig. 4). The most resistive contributions are the extension overlap with the gate (R_{Ovext} , weak variation with L_{ext}) and the extension (R_{ext} , linear variation with L_{ext}), which both decrease for stronger extension doping.

To determine eDMOS optimization performance path, we perform then simulations varying parameters one by one. First, channel length L_{ch} can be reduced to decrease R_{ON} but it activates short channel effects leading to leakage degradation for $L_{ch} < 300nm$. Indeed, if L_{ch} is reduced from 230 to 90nm, 35% R_{ONS} lowering is obtained, but it is associated to 2 decades leakage I_{OFF} degradation due to V_T lowering (Fig. 5). Then, OV_{ext} , L_{ext} and T_{Si} impact on R_{ONS}/I_{OFF} tradeoff is shown on Fig. 6. For $T_{Si} = 23nm$ (red curves), R_{ONS} is reduced by 25% with OV_{ext} reduced by a factor 4 compare to REF without impact on I_{OFF} . However, reducing L_{ext} by a factor 2 yields a 32% R_{ONS} reduction but at the cost of ~1-decade increase in I_{OFF} . To understand I_{OFF} behavior, the lateral electric field $|E|$ distribution from the source to the drain at $T_{Si}/2$ is extracted from TCAD at $V_{GS} = 0V$ and $V_{DS} = -7V$ for OV_{ext} (Fig. 7) and L_{ext} (Fig. 8) variations. Three $|E|$ maximums (E_{MAX}) locations are identified and indicated by symbols: channel/Extension junction (Triangle), Gate corner (circle) and extension/drain junction (star). Starting from REF device, OV_{EXT} reduction up to a factor 4, the space between E_{MAX} decreased, but E_{MAX} value remains the same on the three locations, explaining why the leakage is constant. Lowering L_{ext} by a factor 2 produces an increase of E_{MAX} at gate corner and drain/extension junction: that's why I_{OFF} increases for shorter extension (Fig. 8). With thicker silicon film T_{Si} than REF device, R_{ONS} and I_{OFF} are reduced, but I_{OFF} increases and R_{ONS} remains the same for L_{EXT} reduction by a factor 2. It highlights that the tradeoff between gate electrostatic control on Si film and the silicon resistivity is modulated by any eDMOS structure variation. I_{OFF} variation with extension doping is evaluated for several L_{ext} and OV_{ext} values (Fig. 9): the optimum N_{EXT} for I_{OFF} is not impacted by OV_{ext} and increases for shorter

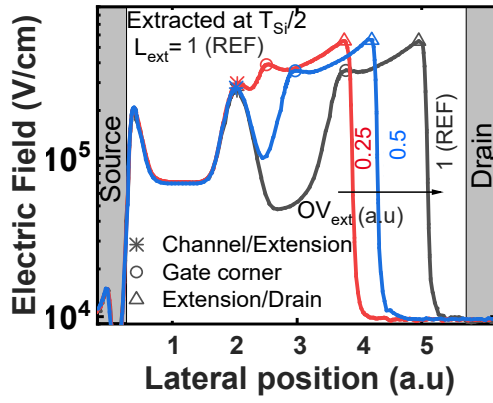


Fig. 7. TCAD lateral electric field for OV_{ext} variation extracted at $T_{Si}/2$ at I_{OFF} .

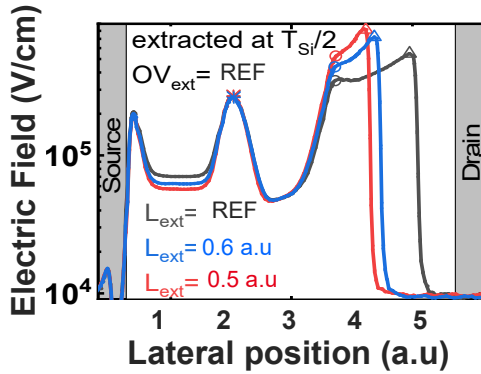


Fig. 8. TCAD lateral electric field for L_{ext} variation extracted at $T_{Si}/2$ at I_{OFF} .

extension. This behavior is fully explained by E_{MAX} variation extracted by TCAD (Fig. 10): N_{EXT} variation allows to minimize E_{MAX} thanks to an equal distribution of the electric field between the three critical locations. Indeed, at low extension doping (for resistive extension), the electric field peak is only located at the drain/extension junction while at high extension doping it is only at the gate corner. In both cases, E_{MAX} is higher: carriers generation mechanisms responsible of GIDL increase and leakage is degraded.

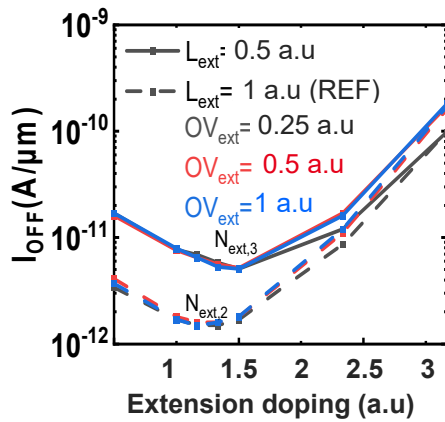


Fig. 10. L_{ext} and OV_{ext} impact on $IOFF$ dependency on extension doping

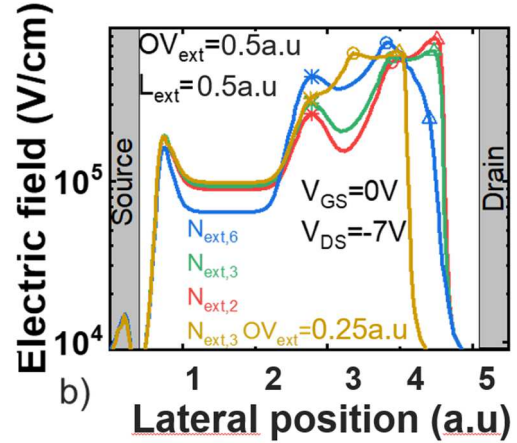
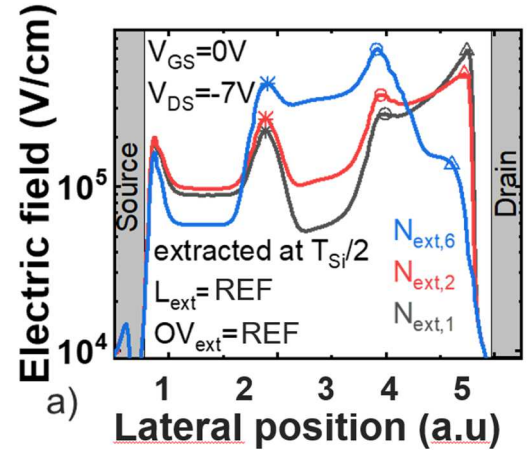


Fig. 9. Electric field versus extension doping for several N_{ext} variation (a) and OV_{ext} variation (b) extracted at $T_{Si}/2$ in I_{OFF} condition.

IV. RESISTANCE AND LEAKAGE OPTIMIZATION IMPACT ON BV

Fig. 11 shows the step by step PeDMOS performance optimization starting from the experimental point [1]. The best tradeoff between leakage and resistance is obtained for a significantly scaled eDMOS. Main device dimensions are reduced: (40% L_{Ch} , 50% OV_{ext} and 25% L_{ext}), leading to R_{ONS} lowering by a factor 2.5 with a limited I_{OFF} increase. No

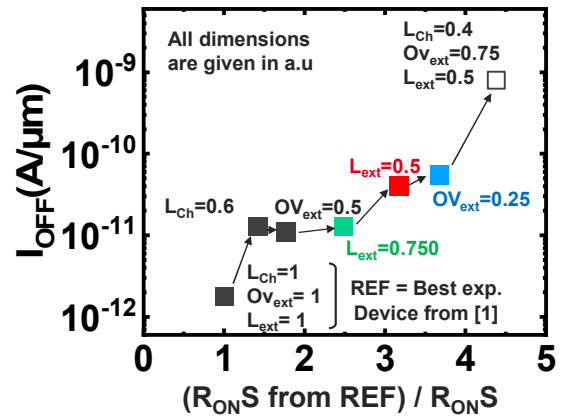


Fig. 11. R_{ONS} - $IOFF$ Step by step PeDMOS optimization through L_{Ch} , L_{ext} and OV_{ext} variation

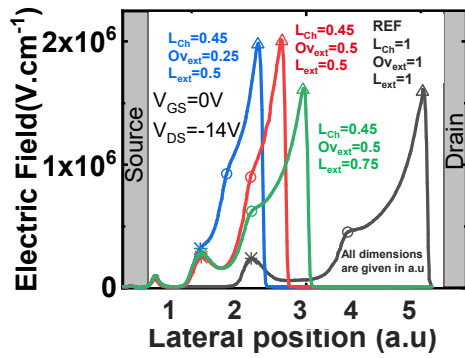


Fig. 12. Electric field distribution in OFF-state ($V_{DS}=-14V$) for optimized PeDMOS

	L_{ch} (a.u.)	$O_{v_{ext}}$ (a.u.)	L_{ext} (a.u.)	R_{ON-S} (a.u.)	I_{OFF} (pA/ μm)	BV
REF	1	1	1	1	2	Similar
#1	0.6	0.5	0.75	2.5	15	
#2	0.6	0.5	0.5	3.2	40	Degradation $E_{MAX} \nearrow$
#3	0.6	0.25	0.5	3.7	60	

Table 1 PeDMOS optimization summary.

impact on device robustness of this optimization is expected. Indeed, the E-field distributions is extracted by TCAD at $V_{DS}=-14V$ and $V_{GS}=0V$ and show that the optimized device exhibits the same E_{MAX} as the experimental reference reported in [1] (green compare to black curves on Fig.12). In contrast, further scaling severely degrades leakage (Fig. 11) and BV as indicated by E_{MAX} increase (Fig. 12), and should probably reduce BV. Optimized PeDMOS dimensions and performances are indicated in table 1.

V. CONCLUSION

This paper demonstrates that a further optimization is possible for the already processed PeDMOS transistors. This was achieved thoroughly by TCAD simulations starting from the resistance contributions decomposition. Three layout optimization paths were identified. Firstly, the channel resistance can be reduced with a slight channel shortening while maintaining the gate electrostatic control of the channel effects. Secondly, shorter extension length allows to reduce R_{ON-S} but increases the leakage, due to the short distance between two locations of electric field maximum: the gate corner and the extension/drain junction. Thirdly, the extension overlap shortening allow to reduce resistance without impact on I_{OFF} (Fig 12 and Table 1). It was also proved that thinning the silicon film increases significantly the leakage. This is linked to a higher SRH and Band-to-Band generation. A thicker Si film allows the current to flow in larger volume, which reduces the resistance. However, floating body effects are less controlled when the film is thicker. Finally, the step-by-step optimization demonstrates that P-type Extended Drain MOSFET can be significantly scaled (factor 0.6 on channel length, 0.5 on overlap length and 0.75 on extension length compare to [1]) and its resistance can be reduced by a factor 2.5 with a moderate leakage current increase while the electric field lateral

distribution at high V_{DS} indicates that the breakdown voltage should be unaffected.

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