

# Circuit-to-Micromagnetics Analysis of Read Disturbance in Two-Terminal SOT-MRAM

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**Abstract**—Two-terminal (2T) spin-orbit torque MRAM (SOT-MRAM) presents a promising approach for high-density, energy-efficient on-chip memory by integrating spin-orbit torque (SOT) and byproduct spin-transfer torque (STT) within a compact cell architecture. However, its shared read and write path introduces a potential read disturbance concern that needs to be assessed. To this end, in this work, we present a circuit-to-micromagnetics framework, which includes layout-extracted SPICE simulations of a 2T SOT-MRAM to evaluate the read current and read delay, and subsequently quantify the read disturbance error (RDE) using rare-event-enhancement-based micromagnetic analysis for 2T full-fixed layer (FFL) and 2T half-fixed layer (HFL) configurations. The suggested 2T-ZSOT design reduces bit-cell area by 43.8% compared to 3T SOT-MRAM while preserving enough read margin (120–170 mV) and quick read access (1.66 ns). It also demonstrates RDE below  $10^{-14}$  for FFL and  $10^{-12}$  for HFL configurations for an out-of-plane spin torque efficiency of  $\xi_{DL,z}=0.052$ . Our findings establish a clear tradeoff between write energy and read disturbance and provide quantitative design guidelines for reliable operation in high-density 2T SOT-MRAMs.

**Keywords**—Magnetic tunnel junction (MTJ), spin-orbit torque (SOT), SOT-MRAM, Read disturbance error (RDE).

## I. INTRODUCTION (HEADING 1)

With the continued scaling of semiconductor technology toward advanced nodes, emerging nonvolatile memory technologies are being actively investigated to address the growing demand for on-chip memory [1]. Among these options, SOT-MRAM is considered a promising candidate due to its superior performance and scalability. SOT-MRAM employs spin-orbit coupling to switch the magnetization of the free layer in a magnetic tunnel junction (MTJ) through the spin Hall effect [2]. In contrast to STT-MRAM, which induces switching by passing a current through the MTJ [3], SOT-MRAM generates a transverse spin current by applying an in-plane current through a non-magnetic heavy metal layer, thereby exerting torque on the free layer magnetization [4]. The spin-transfer torque efficiency per unit charge in STT-MRAM is limited to less than one (in units of  $\hbar/2$ ), whereas SOT-MRAM can achieve values exceeding one, depending on material properties and device geometry, which enables enhanced energy efficiency [5]. Furthermore, SOT-MRAM provides faster switching, greater endurance, and improved read performance, making it well-suited for applications such as in-memory computing, probabilistic computing, and reservoir computing [6].

To improve memory density and scalability, two-terminal (2T) SOT-MRAM has been introduced as a compact alternative to conventional three-terminal (3T) designs by eliminating the separate write access path and reducing device footprint [7]. This approach enables higher integration density and improved layout efficiency, making 2T SOT-MRAM suitable for large-scale memory arrays. Beyond its density advantage, 2T SOT-MRAM leverages both spin-orbit torque (SOT) and byproduct spin-transfer torque (STT) to enhance switching efficiency and reduce write energy. Both 2T full fixed-layer (FFL) and half fixed-layer (HFL) configurations have been investigated to optimize spin current injection and switching efficiency [8]. It is reported in [8] that an out-of-plane spin torque component ( $\xi_{DL,z}$ ) is necessary for 2T SOT-MRAM to obtain competitive write performance, while a moderate out-of-plane spin-torque suffices to obtain SRAM-level write energy. Also, the HFL design can achieve enhanced average spin current density and reduced write energy due to its enhanced effective electron path through the SOT layer [8]. Consequently, 2T SOT-MRAM demonstrates improved write performance compared to conventional STT-MRAM and 3T SOT-MRAM designs. However, this increased switching efficiency introduces a critical reliability concern: a small read current during read operation may perturb the free layer magnetization, resulting in Read Disturbance Error (RDE). In recent literature, read disturbance has been extensively studied in STT-MRAM [9], demonstrating read disturbance errors in the range of 1ppb. In addition, read disturbance in 3T SOT-MRAM from a device reliability perspective has been analyzed in [10–12]. Notably, since the read and write paths are decoupled in 3T SOT-MRAM, the MTJ oxide barrier can be made thicker to effectively eradicate read disturbance. However, since 2T SOT-MRAM shares the same path for read and write operations, similar to STT-MRAM, the corresponding analysis of read disturbance for 2T SOT-MRAM remains largely unexplored. Specifically, prior studies do not address the interplay between array-level read operation, device-level current distribution, and magnetization dynamics, leaving a significant gap in understanding the read disturbance behavior in practical 2T SOT-MRAM systems.

In this study, we analyze read disturbance in two-terminal SOT-MRAM using a comprehensive circuit-to-magnetization framework, as shown in Fig. 1. The suggested method first uses SPICE simulations of a 128x128 subarray using layout-extracted parasitics to obtain realistic read conditions. Afterwards, the calculated read currents are incorporated into

finite-element analysis to obtain the current distribution and subsequently to evaluate the spin current using the spin drift-diffusion framework. Finally, rare-event-enhanced micromagnetic analysis is utilized to estimate read disturbance. This comprehensive framework allows us to assess the RDE for both HFL and HFL and to determine the impact of out-of-plane spin torque efficiency on RDE.

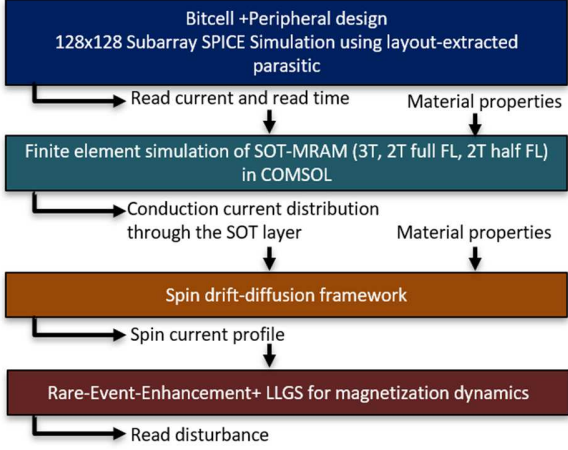


Fig. 1. Circuit-to-micromagnetics framework to assess RDE

## II. BIT-CELL AND PERIPHERAL DESIGN FOR 2T SOT-MRAM

### A. Bit-cell Design

This study examines two-terminal SOT-MRAM bit-cells with FFL and HFL configurations, adopted from [8], which are illustrated in Fig. 2(a). The layout of a perpendicular magnetic anisotropy (PMA) 2T SOT-MRAM, where a  $2 \times 2$  bit-cell unit shares bit-line (BL) and word-line (WL) contacts, is illustrated in Fig. 2(b). The SOT layer and magnetic tunnel junction (MTJ) are vertically integrated between the M1 and M2 metal levels and connected through vias. A simplified representation of the layout is presented in Fig. 2(c).

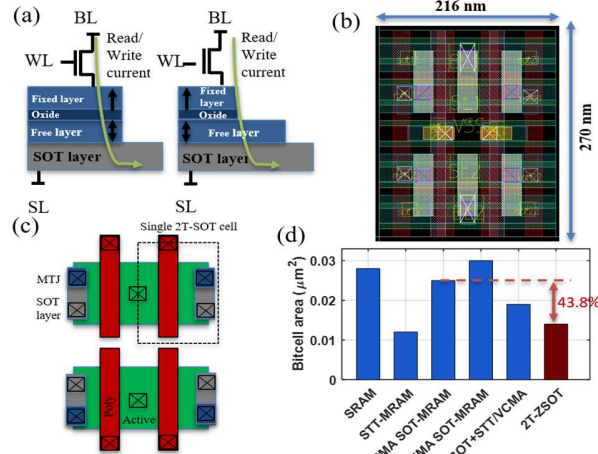


Fig. 2. (a) 2T SOT-MRAM bit cells (b) 2T SOT-MRAM layout (c) Simplified representation of the layout (d) Bitcell area comparison for various memory options

The bit-cell layout uses M1 through M3 metal layers, with BL and source-line (SL) routed on M2, and WL on M3. Here, M2 is oriented horizontally, while M3 is oriented vertically. This work was supported by SUPREME, one of seven centers in JUMP 2.0, an SRC program sponsored by DARPA.

area of a  $2 \times 2$  unit is found to be  $0.216 \mu\text{m} \times 0.270 \mu\text{m}$ , which corresponds to a bit-cell area of  $0.0146 \mu\text{m}^2$ . Thus, due to the compact two-terminal structure, the proposed 2T-ZSOT design achieves a 43.8% reduction in bit-cell area compared to conventional 3T SOT-MRAM.

### B. Peripheral Design and Read Performance

The peripheral circuits are co-designed with the bit-cells to facilitate compact array integration while ensuring robust read and write operations. The WL, BL, and SL drivers shown in Fig. 3 are integrated with level shifters to support a higher write voltage ( $V_{DDH} = 0.8\text{--}1.3 \text{ V}$ ) than the core supply voltage ( $V_{DD} = 0.7 \text{ V}$ ). The write current is supplied through SL and BL drivers during write operation, while column multiplexers are incorporated in the BL path for read operation. The integrated bitline driver used in this study employs a tri-state buffer-based design that is triggered by the write enable signal, ensuring proper isolation between the read and write paths. WLs are driven by inverter-based drivers with three fins, as the WL primarily drives capacitive gate loads and therefore does not require large drive strength.

For the read operation, a differential voltage scheme is employed using a reference column as shown in Fig. 4. The reference column consists of two bit-cells biased in parallel (P) and antiparallel (AP) states, generating a reference current of  $(I_P + I_{AP})/2$ , where  $I_P$  and  $I_{AP}$  correspond to the currents of the selected bit-cell in the P and AP states, respectively [13].

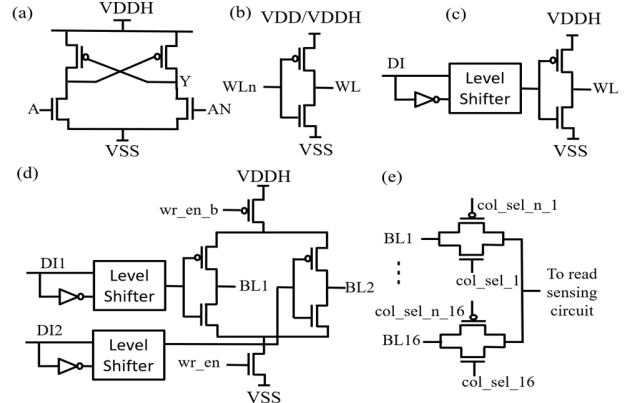


Fig. 3. Schematic for (a) low-to-high level shifter, (b) WL driver, and (c) SL driver. (d) Modified integrated bitline driver (e) Schematic for column multiplexers.

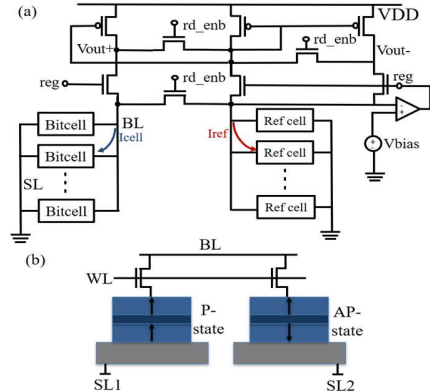


Fig. 4. Schematics for (a) read circuit and (b) read reference for a 2T SOT-MRAM

### C. Read Performance of 2T SOT-MRAM

Through circuit simulations for a 128x128 subarray using layout-extracted R and C parasitics, the bit-cell current ( $I_{\text{cell}}$ ) is compared against the reference current ( $I_{\text{ref}}$ ) to produce a differential voltage, which is defined as the read margin. The transistors are modeled using BSIM-CMG compact models corresponding to a 7 nm FinFET technology. We find that the read margin stays inside the range of 120–170 mV, with the maximum margin achieved at  $V_{\text{bias}} = 125$  mV, corresponding to read currents of 6  $\mu\text{A}$  (P) and 4.8  $\mu\text{A}$  (AP) as shown in Fig. 5.

Next, the read performance of a 128x128 2T SOT-MRAM with  $V_{\text{bias}} = 125$  mV is presented in Fig. 6. Depending on the MTJ state, the bitline current starts to develop as the read enable signal is asserted, producing a corresponding differential voltage at the sensing nodes. The charging and discharging of parasitic capacitances cause the read margin to first fluctuate briefly before settling to a steady value. The sense amplifier resolves this differential signal to produce a full-swing digital output afterwards. The read delay, defined as the time from the read enable assertion to the valid output, is found to be 1.66 ns from Fig. 6.

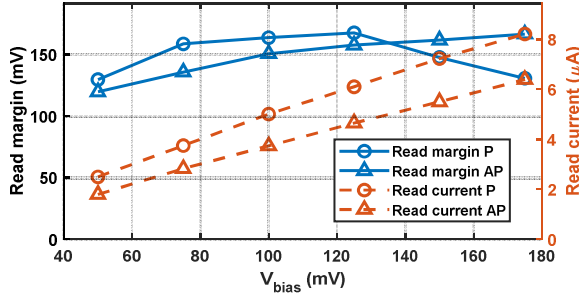


Fig. 5. Read margin and read current for various  $V_{\text{bias}}$

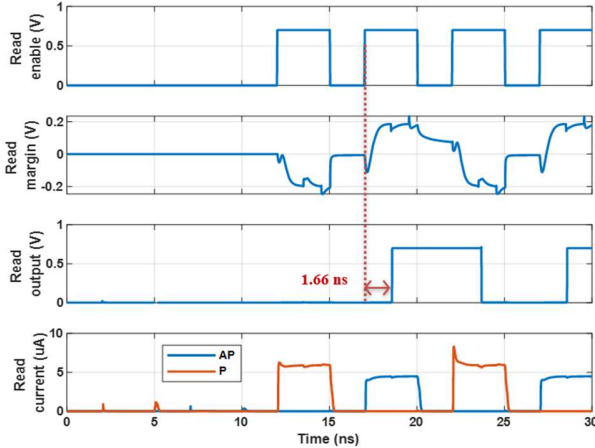


Fig. 6. Read performance of a 128x128 2T SOT-MRAM

### III. READ DISTURBANCE MODELING USING REE-BASED MICROMAGNETIC FRAMEWORK

To assess read disturbance, first, the conduction current density distribution within the SOT layer is determined through finite-element simulations, using the read current derived from layout-aware SPICE simulations. Next, the resulting non-uniform current density profiles are applied in the spin drift-diffusion framework [14] to calculate the respective spin current components for both the 2T FFL and HFL configurations, as

illustrated in Fig. 7. As evident from Fig. 7, the SOT-induced spin current for the FFL configuration shows a roughly linear increase over the device length. This leads to a higher peak spin current density close to one edge but a comparatively lower average spin current. Due to the high resistance of the oxide layer, the STT-induced spin current is almost constant throughout the device. Notably, the average spin current for the HFL design is higher than for the FFL scenario because the spin current quickly achieves a constant value close to the end of the shortened fixed-layer region and thereafter stays almost constant. The overall spin torque operating on the free layer is further increased by the substantial enhancement of the STT contribution within the shortened fixed-layer area. Thus, the HFL configuration possesses greater vulnerability to read disturbance due to its enhanced spin current generation.

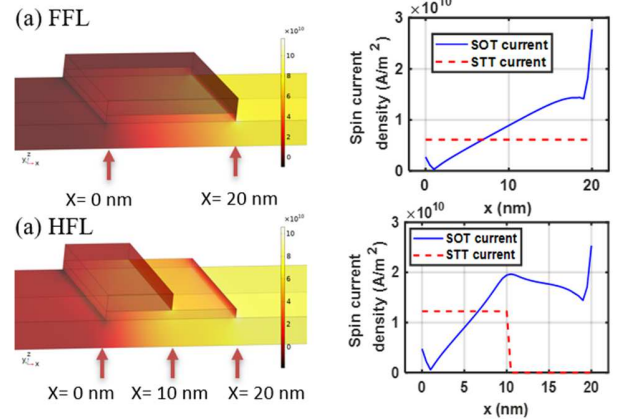


Fig. 7. Conduction current distributions and generated spin currents for FFL and HFL structures

TABLE I

| Parameter                                             | Values for PMA            |
|-------------------------------------------------------|---------------------------|
| Saturation magnetization $M_s$ (A/m)                  | $1.257 \times 10^6$       |
| Damping constant $\alpha$                             | 0.01                      |
| MTJ dimension (nm)                                    | $20 \times 20 \times 1.3$ |
| Resistance-area product ( $\Omega \mu\text{m}^2$ )    | 4.0                       |
| Magnetic anisotropy energy $K_u$ (MJ/m <sup>3</sup> ) | 1.33                      |
| Temperature (K)                                       | 300                       |
| Thermal stability factor ( $\Delta$ )                 | 57                        |
| Exchange constant $A_x$ (pJ/m)                        | 20                        |
| External magnetic field $B_x$ (mT)                    | 0                         |

The generated spin current profiles are then integrated into micromagnetic simulations conducted with OOMMF, with the parameters outlined in Table I [3]. We employ a rare-event enhancement (REE)-based write error rate framework that has been validated against the experimental data reported in [15], as demonstrated in Fig. 8. Estimating the probability of a rare event,  $P(R)$ , in traditional Monte Carlo (MC) simulations needs on the order of  $1/P(R)$  trials, making it computationally impractical for MRAM read disturbance analysis, where incredibly low error rates are needed. However, read disturbance probability below  $10^{-12}$  can be accurately estimated using the importance-splitting-based rare-event enhancement (REE) technique. By starting with a reasonable number of trials and gradually biasing the sampling toward paths that are more likely to achieve the rare event, the REE approach overcomes the computational constraint. In particular, low-probability

switching events can be effectively investigated by selectively duplicating trials nearer the target event while maintaining total statistical weight. In the case of PMA magnets, the rare event corresponds to accidental switching of the free layer magnetization ( $m_z$ ). Until a switching event ( $m_z < 0$ ) is noted, trials with lower  $m_z$  values are preferentially duplicated. With this method, read disturbance error (RDE) may be efficiently estimated at very low probability levels (around  $10^{-25}$ ) without sacrificing computational practicability.

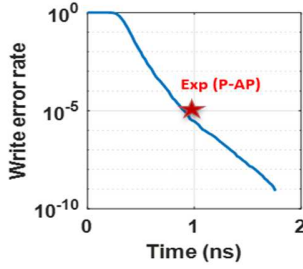


Fig. 8. REE-based write error rate for a conventional SOT-MRAM

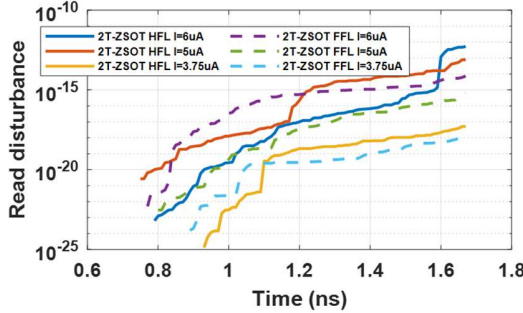


Fig. 9. Read disturbance errors for different read currents

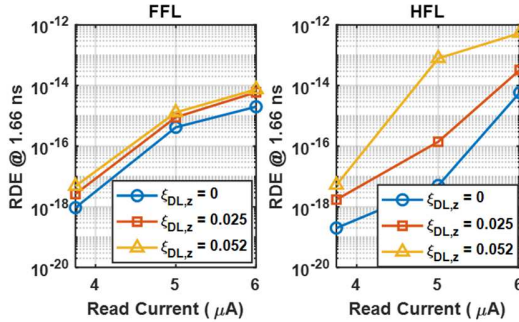


Fig. 10. Read disturbance error dependencies on out-of-plane spin torque efficiency

With this framework, we assess the read disturbance error (RDE) based on the read current and time obtained from SPICE simulations. Fig. 9 demonstrates that for an out-of-plane spin torque efficiency of  $\xi_{DL,z}=0.052$ , which is the necessary  $\xi_{DL,z}$  for the HFL configuration to achieve SRAM-level write energy [8], all scenarios maintain RDE below  $10^{-12}$  at a read duration of 1.66 ns. Fig. 10 depicts the relationship between RDE and  $\xi_{DL,z}$  by illustrating RDE at 1.66 ns against the read current for various  $\xi_{DL,z}$  levels, where the FFL configuration shows an RDE lower than  $10^{-14}$ , while the HFL configuration displays greater sensitivity with an RDE of around  $10^{-12}$ . This increased sensitivity in the HFL case is attributed to its higher effective

spin current and stronger dependence on the out-of-plane torque component  $\xi_{DL,z}$ . Thus, although HFL designs enhance write efficiency by increasing spin current injection, they are more vulnerable to read disturbance.

#### IV. CONCLUSIONS

In conclusion, the suggested 2T-ZSOT design maintains a read margin of 120–170 mV and a read delay of 1.66 ns with read currents of 6  $\mu$ A (P) and 4.8  $\mu$ A (AP), while achieving a bit-cell area of 0.0146  $\mu\text{m}^2$  (43.8% reduction vs. 3T). The read disturbance error is found to be below  $10^{-14}$  for the FFL configuration and below  $10^{-12}$  for the HFL configuration at  $\xi_{DL,z}=0.052$  using REE-based micromagnetic analysis, which suggests a greater dependence on the out-of-plane spin torque component for HFL.

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