

Revealing New Leakage Paths in GAAFETs using Predictive First-Principles Simulations

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Abstract—Gate-All-Around Field-Effect Transistors (GAAFETs) are emerging as successors to Fin Field-Effect Transistors (FinFETs) and are central to continued scaling at advanced semiconductor nodes. Despite their improved electrostatic control, recent measurements show that the drain current in GAAFETs deviates strongly from thermionic behavior at negative gate voltages, increasing as the gate voltage becomes more negative. This leakage has been attributed to direct gate-drain tunneling through the high- k dielectric, enhanced by drain-induced dielectric barrier lowering (DIDBL). Here, we use predictive, charge-self-consistent Non-Equilibrium Green Function (NEGF) simulations based on the Contact Block Reduction (CBR) method to spatially resolve this leakage pathway in GAAFETs. Unlike approaches based primarily on phenomenological leakage models, our first-principles, multi-terminal quantum-transport framework treats the source, drain, and gate as current-carrying quantum-mechanical contacts and resolves the local current density throughout the device. The spatially resolved current density shows that gate-injected carriers tunnel through the high- k dielectric preferentially near the drain side of the gate—where the dielectric barrier is most strongly lowered by the drain bias—and are collected by the drain, providing a direct real-space picture of the DIDBL-driven gate-drain leakage mechanism.

Index Terms—Gate-All-Around Field-Effect Transistor (GAAFET); gate leakage; Non-Equilibrium Green Function (NEGF); Contact Block Reduction (CBR) method; quantum transport simulations

I. INTRODUCTION

Gate-All-Around Field-Effect Transistors (GAAFETs) are emerging as the leading device architecture for continued

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This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

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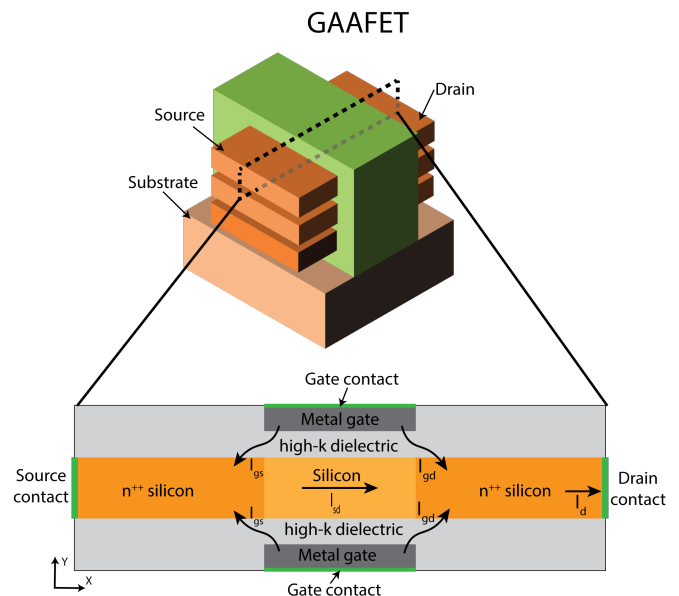


Fig. 1. GAAFET architecture and cross-sectional schematic of the single-sheet GAAFET device used in this work.

CMOS scaling beyond Fin Field-Effect Transistor (FinFET) technology. By fully surrounding the nanosheet or nanowire channel with the gate (Fig. 1), GAAFETs provide improved electrostatic control, reduced short-channel effects, and a pathway toward stacked-channel designs with higher drive current and increased integration density. These advantages make GAAFETs central to advanced semiconductor nodes and future high-performance computing technologies.

Despite these advantages, recent measurements in [1] have revealed non-ideal behavior outside the nominal operating regime. In particular, at negative gate voltages, the measured drain current deviates strongly from the expected thermionic trend (see Fig. 2): instead of continuing to decrease expo-

nentially as the channel barrier increases, the current departs from the thermionic trend and rises as the gate voltage becomes more negative. Understanding the physical origin of this behavior is important for determining the scaling limits of GAAFETs, reducing off-state leakage, and assessing device reliability in applications where radiation-induced defects predominantly affect the deep-subthreshold regime [2].

In conventional MOSFETs and FinFETs, negative-gate-bias leakage is commonly attributed to gate-induced drain leakage (GIDL), driven by band-to-band tunneling near the gate-drain overlap region. However, this mechanism is less applicable to GAAFETs because the active channel is isolated from the substrate by the surrounding high- k dielectric, and the relevant drain-bias range is not expected to produce conventional GIDL conditions. These differences motivate a quantum-transport analysis that treats the source, drain, and gate contacts quantum mechanically and explicitly accounts for all possible current paths.

For computational efficiency, many conventional Non-Equilibrium Green Function (NEGF) implementations are formulated as two-terminal source-drain problems in which the gate enters only electrostatically, through the potential obtained from Poisson's equation, and is not treated as an open quantum-mechanical contact with its own carrier injection. Such methods capture channel transport and electrostatic short-channel effects but cannot directly resolve gate-related leakage paths, such as gate-source or gate-drain. In contrast, the multi-terminal NEGF based on the Contact Block Reduction (CBR) method used here treats the source, drain, and gate as current-carrying quantum contacts, which is essential both for decomposing the total current into its physical components and, as we show here, for resolving where these currents flow inside the device.

In our previous work [3], we identified the physical origin of the negative-gate-voltage leakage in GAAFETs. We showed that the dominant contribution arises from direct gate-drain tunneling through the high- k dielectric. This gate-drain leakage is further enhanced when the applied drain bias lowers the effective dielectric tunnel barrier between the gate and drain, a mechanism we identified as drain-induced dielectric barrier lowering (DIDBL). This gate-drain leakage mechanism has since been independently corroborated by experiment [4]. However, while the terminal-current decomposition revealed the dominant leakage component, the spatial pathway of this leakage across the device remained unresolved. In this work, we focus on the gate-drain leakage channel and employ a charge-self-consistent, multi-terminal NEGF/CBR framework to spatially resolve it, directly visualizing how gate-injected carriers tunnel through the dielectric and reach the drain.

II. METHODS

Simulations use the open-system, charge-self-consistent Non-Equilibrium Green's Function (NEGF) formalism [5], [6] implemented via the Contact Block Reduction (CBR) method [7]–[15]. This framework has previously reproduced

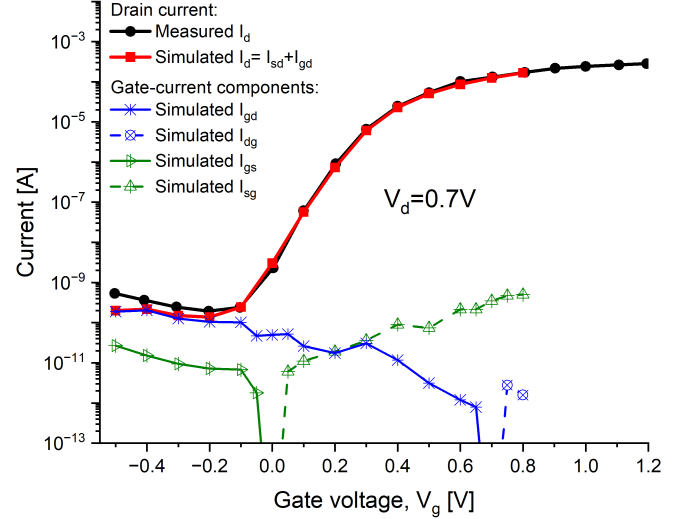


Fig. 2. $I - V_g$ characteristics and the corresponding gate leakage current contributions for $V_d = 0.7$ V. Adapted from [3] under the Creative Commons Attribution License (CC BY). Measured currents reprinted with permission from [1]. Copyright 2017 IEEE.

experimental results in several nanoscale device systems, supporting its robustness and predictive capability [3], [16]–[18]. The CBR method enables efficient calculation of the density matrix, transmission function, and related quantities for arbitrarily shaped multi-terminal two- and three-dimensional open devices within the NEGF formalism, with linear scaling, $O(N)$, with the system size (N). Importantly, its applicability to multi-terminal systems allows the source, drain, and gate to be treated as current-carrying quantum-mechanical contacts within the same self-consistent solution. This capability is essential for accurately calculating gate leakage and separating source-drain, gate-source, and gate-drain current components.

Within this framework, the open-system Schrödinger equation and the nonlinear Poisson equation are solved self-consistently [7], [10], [13]. The kinetic energy operator is described using a multiband effective-mass tensor approximation with three non-equivalent, double-degenerate silicon valleys defined by the longitudinal and transverse effective masses. From the same self-consistent solution, the spatially resolved current density $\mathbf{J}(\mathbf{r})$ is obtained from the energy-resolved non-equilibrium (lesser) Green function, yielding the local current between neighboring grid sites and thereby the internal current pathways visualized below.

III. RESULTS AND DISCUSSION

The simulated device shown in Fig. 1 consists of a 2D single-sheet GAAFET structure, where the silicon nanosheet channel is surrounded by a high- k gate dielectric and metal gate. Following Ref. [1], the physical gate length is $L_g = 12$ nm, the silicon nanosheet thickness is $T_{Si} = 5$ nm, and the effective nanosheet width is $W_{Si} = 30$ nm. The source and drain regions are highly doped with a concentration of $3.0 \times 10^{20} \text{ cm}^{-3}$, while the channel doping is $5.0 \times 10^{17} \text{ cm}^{-3}$.

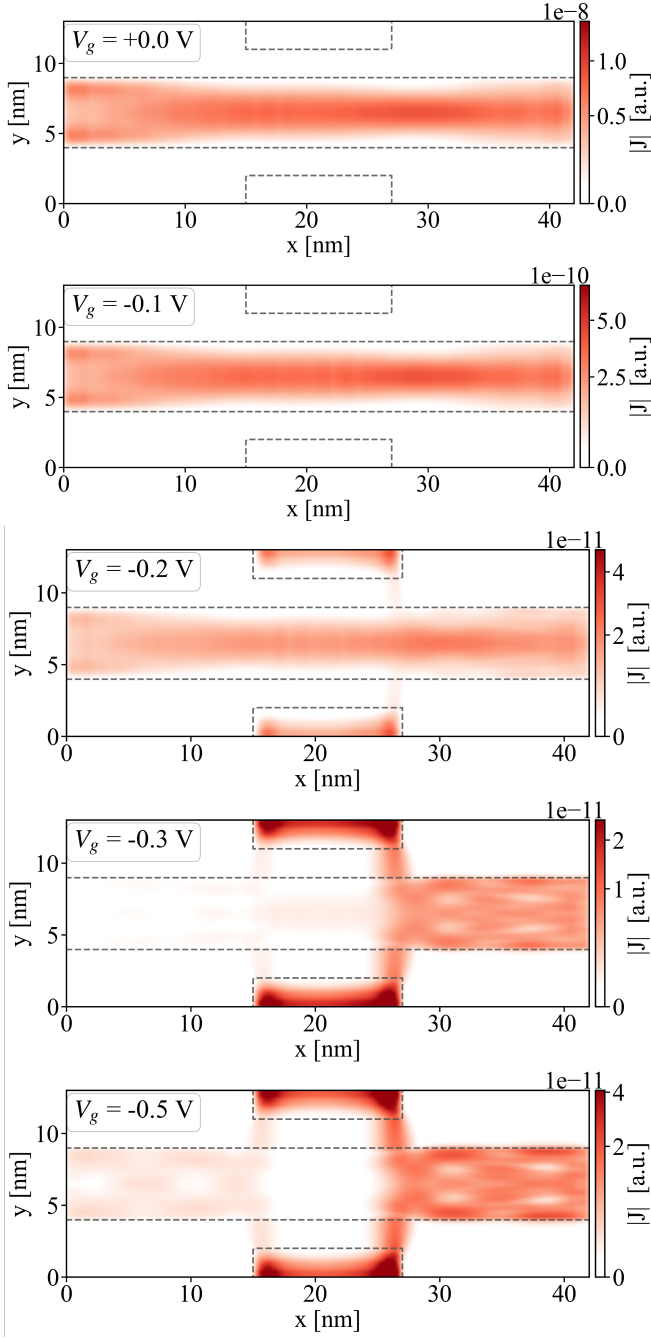


Fig. 3. Spatial current density across the device at zero and several negative gate voltages. Note that each panel uses its own color scale to highlight the spatial distribution at each bias.

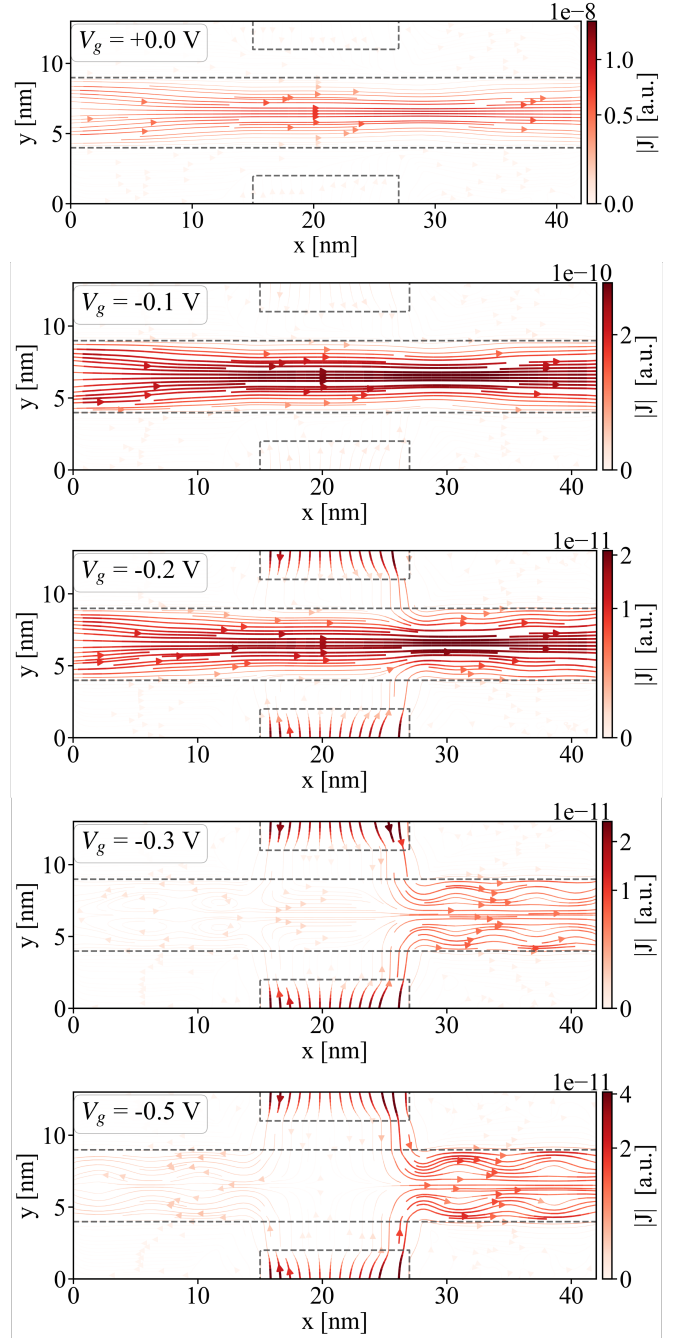


Fig. 4. Streamlines of the current density across the device at zero and several negative gate voltages. The current direction is defined by the direction of electron flow. Note that each panel uses its own color scale to highlight the spatial distribution at each bias.

The gate stack uses a 2 nm HfO_2 high- k dielectric with a dielectric constant of $\epsilon = 20$ and an electron barrier height of 1.6 eV, together with a metal gate work function of 4.5 eV.

Fig. 2 shows the measured and simulated current–gate-voltage characteristics at $V_d = 0.7$ V, together with the decomposed gate-current components. The simulated total drain current ($I_d = I_{sd} + I_{gd}$) is in very good agreement with the

measurement over the full gate-voltage range. For positive gate voltages, the total drain current is the intended source–drain channel current, while the gate-current components (I_{gd} and I_{gs}) remain several orders of magnitude smaller. At negative gate voltages, the behavior changes qualitatively: the gate-drain current (I_{gd}) rises to become the dominant contribution to the total drain current and accounts for its increase as V_g

becomes more negative. The pronounced enhancement of I_{gd} with applied drain bias, established in Ref. [3], identifies drain-induced dielectric barrier lowering (DIDBL) between the gate and drain as the mechanism underlying this leakage.

Figs. 3 and 4 present the spatially resolved current density and its flow direction, the central result of this work. Fig. 3 shows the magnitude $|\mathbf{J}(\mathbf{r})|$ and Fig. 4 the corresponding streamlines, oriented along the electron flow, at $V_g=0$ V and several negative gate voltages (each panel uses its own color scale). At $V_g=0$ V and small negative biases, the current is confined to the silicon channel and flows directly from source to drain, as expected for normal operation. As the gate voltage becomes more negative, the channel current is progressively suppressed and a qualitatively different pattern develops: carriers are injected from the metal gates, tunnel across the high- k dielectric, and are collected by the drain.

This gate-drain leakage path is strongly asymmetric: it forms preferentially at the drain-side edge of the gate, whereas the gate-source side carries comparatively little current. This drain-side localization is the real-space signature of DIDBL, as the drain bias lowers the dielectric barrier most effectively where the gate and the highly doped drain are in close proximity, opening the leakage path precisely there. The streamlines make the mechanism explicit, showing carriers entering from both the top and bottom gates near the drain edge, turning, and converging into the drain. By $V_g=-0.5$ V, the source-to-drain channel path is essentially extinguished and the device current is carried almost entirely by this gate-drain leakage path. These maps thus localize, in real space, the leakage that the terminal-current decomposition could attribute only to the gate-drain terminal pair.

IV. CONCLUSION

In this work, we demonstrated a predictive, charge-self-consistent NEGF/CBR framework that treats the source, drain, and gate as current-carrying quantum-mechanical contacts within a single self-consistent solution, enabling both a decomposition of the terminal currents and a spatially resolved map of the internal current density.

Applying this framework to a scaled GAAFET, we showed that the non-thermionic increase of the drain current at negative gate voltages originates from direct gate-drain tunneling through the high- k dielectric, enhanced by drain-induced dielectric barrier lowering. The spatially resolved current density localizes this leakage at the drain-side edge of the gate and visualizes, in real space, how gate-injected carriers cross the dielectric and are collected by the drain, providing direct confirmation of the DIDBL-driven gate-drain leakage mechanism.

These results highlight the value of multi-terminal, spatially resolved quantum-transport simulations for advanced transistor design. Beyond identifying the dominant leakage path, the real-space picture points to concrete co-design mitigation strategies, such as locally thickening the high- k dielectric or replacing it with a higher-barrier material (e.g., SiO_2) on the drain side of the gate, without degrading gate control over

the channel. The NEGF/CBR framework thus provides a predictive basis for identifying scaling limitations and evaluating such designs in future ultra-scaled technologies.

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