

Performance Analysis of Silicon GAA-NS-FETs

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Abstract— Gate-all-around Silicon Nanosheet (GAA-NS) FETs with an aggressive gate length L_g of 6 nm are simulated at the atomic scale thanks to a non-equilibrium Green's function (NEGF) formalism. Accurate band structures combined with a generalized low-rank approximation enable a systematic exploration of short-channel effects (SCE) and downscaling trends for channel thicknesses T_{Si} ranging from 4 nm to 2 nm. Key performance metrics - subthreshold slope (SS), drain-induced barrier lowering (DIBL), effective mobility, and injection velocity (V_{inj}) - are extracted for multiple substrate orientations of technological interest. The results are in good agreement with recently published experimental data and reveal a clear improvement in electrostatic control and carrier transport as silicon thickness is reduced, with no observable performance degradation.

Keywords— Simulation, Atomistic, NEGF, GAA, Nanosheet, MOSFET, SCE, DIBL, SS, Mobility, Injection Velocity.

I. INTRODUCTION

The CMOS manufacturing industry is moving toward the so-called one-Ångström era [1], with increasingly precise surface engineering aimed at approaching the ultimate scaling limit through atomically smooth materials and defect-free interfaces. Gate-all-around nanosheet FETs (GAA-NS-FETs) are replacing Fin-FET technology by providing superior electrostatic control and enabling higher integration densities. Nevertheless, scaling the gate length L_g below 10 nm remains challenging [2], not only from a fabrication standpoint but also because of the increasing impact of short-channel effects and quantum confinement. At these dimensions, conventional TCAD approaches based on semiclassical transport become increasingly inaccurate, as they cannot fully capture atomistic effects, quantum confinement, and coherent transport. To address these limitations, we investigate Si GAA-NS-FETs using atomistic quantum transport simulations based on the non-equilibrium Green's function (NEGF) formalism, which naturally incorporates quantum effects with atomic-scale resolution [3].

II. METHODOLOGY

A. NEGF Code

The simulations are performed using the *Victory Atomistic* tool [4], an atomistic NEGF solver derived from Nemo5 [3]. The electronic structure is described within the $sp^3d^5s^*$ tight-binding basis, which accurately reproduces the silicon band structure and offers excellent transferability to nanosheet FET geometries with nanometer-scale cross sections. Silicon dangling bonds are passivated by hydrogen through an ad hoc passivation self-energy, ensuring a realistic

description of the nanostructure. The resulting atomistic Hamiltonian provides the accuracy required to describe the electronic states of thin silicon nanosheets. When combined with a state-of-the-art low-rank approximation (LRA) projection technique [5], the NEGF solver enables computationally efficient atomistic simulations of ultra-scaled transistors while accounting for the essential carrier-scattering mechanisms.

B. Physical Dimensions and Parameters

The geometry of the GAA-NS-FET is shown in Fig. 1. It consists of a silicon nanosheet channel connected to heavily doped source and drain regions, surrounded by an ultra-thin gate-all-around oxide, and completed by inner dielectric spacers on both sides of the gate. Following current technology, the channel is oriented along the $\langle 110 \rangle$ transport direction, with (001) and (110) confinement surfaces, as illustrated in Fig. 2.

TABLE I. PHYSICAL DIMENSIONS OF THE Si $\langle 110 \rangle$ GAA-NS-FETs, DIELECTRIC PROPERTIES, AND DOPING.

Parameter	Value/range
Width (W)	12 nm
T_{Si} (H)	2, 3, 4 nm
L_s, L_d	9 nm
L_{ch}	15 nm
L_{s1}, L_{s2}	4.5 nm
L_g	6 nm
t_{ox}	1 nm
$\epsilon_{Si, S2}$	2.7 (ϵ_0)
ϵ_g	3.9 (ϵ_0)
Doping (Ch)	10^{15} (e.cm $^{-3}$)
Doping (S, D)	10^{20} (e.cm $^{-3}$)

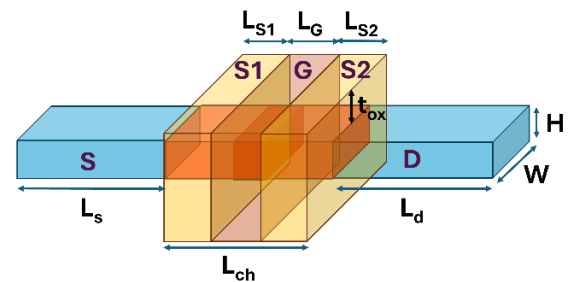


Fig. 1. GAA-NS-FET showing the inner dielectric spacers and the characteristic device dimensions. The corresponding geometrical and physical parameters are listed in Table I.

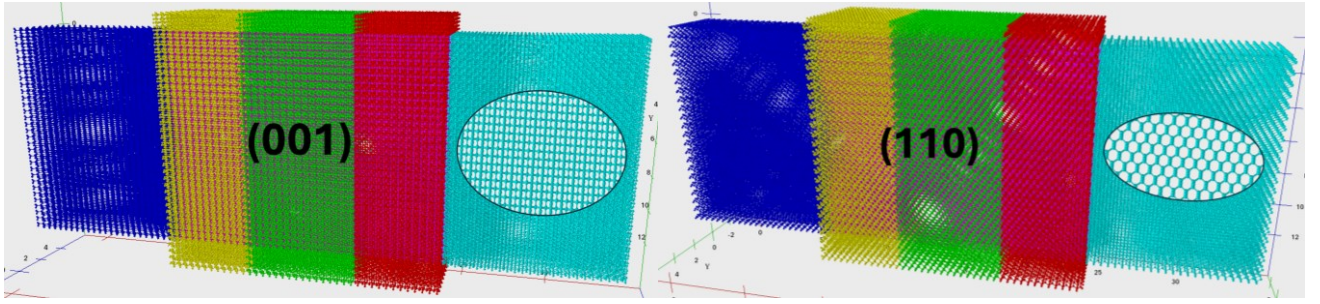


Fig. 2. Atomistic structure of a $4 \times 12 \text{ nm}^2$ Si channel oriented $\langle 110 \rangle$ with two different substrate orientations (001) (left) and (110) (right) seen from above. S/D in blue and turquoise, spacers in yellow and red, gate in green. A zoom on the crystal structure is performed in the drain region.

The device parameters are summarized in Table I. An ensemble of six GAA-NS-FETs is investigated, each with a nanosheet width of 12 nm, channel thicknesses of 2, 3, or 4 nm, a gate length of 6 nm, and two 4.5 nm low-K inner spacers. For each channel thickness, the two substrate orientations, (001) and (110), are considered. Each atomistic structure contains approximately 10^5 atoms.

C. NEGF Self-Consistency and Electron-Phonon Scattering

Under steady-state conditions, the NEGF and Poisson equations are solved self-consistently for different bias conditions to compute the device current characteristics.

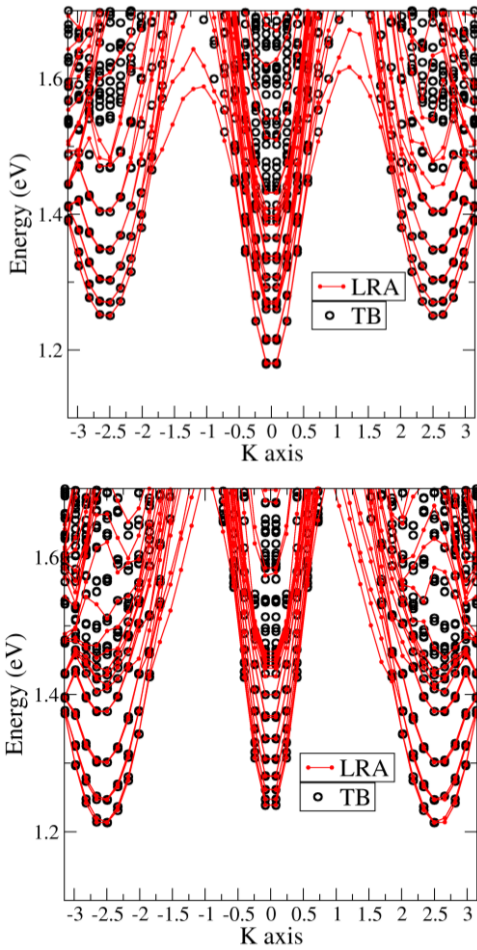


Fig. 3. Si band structure for a $4 \times 12 \text{ nm}^2$ NS cross-section oriented (001) (top), (110) (bottom). The original tight-binding (TB $\text{sp}^3\text{d}^5\text{s}^*$) bands are in black, the LRA approximation in red, reproducing a dozen bands within an energy window of 0.3 eV above the conduction band minima

Electron-phonon interactions are incorporated within the self-consistent Born approximation. The acoustic and optical phonon branches are described using bulk silicon parameters, which capture the dominant scattering mechanisms governing charge transport in the silicon channel surrounded by silicon oxide.

D. Low-Rank Approximation

The computational cost of atomistic NEGF simulations is primarily determined by the matrix order N , which scales with the product of the number of atoms and the size of the tight-binding basis. Since the required matrix operations scale as $O(N^3)$, scattering mechanisms and detailed band structures are often simplified to reduce the computational burden, limiting simulations to parabolic-band models. To retain an accurate description of the nanosheet electronic structure, the Hamiltonian is projected onto a reduced basis using the generalized LRA [5], which filters out degrees of freedom with negligible impact on transport. This approach reduces the matrix rank by more than one order of magnitude while preserving the relevant physics. As shown in Fig. 3, the LRA accurately reproduces the $\text{sp}^3\text{d}^5\text{s}^*$ band structure over the transport energy window using a greatly reduced number of bands. For the $4 \times 12 \text{ nm}^2$ cross-section, the full silicon slice contains more than 8000 bands, whereas for the simulation of an n-type channel, only 153 and 177 are retained for the (001) and (110) substrate orientations, respectively. Without the LRA, such a systematic study would be computationally prohibitive, not to say impossible.

III. RESULTS

A. DIBL, SS

The transfer characteristics are computed at low $V_d = \pm 50 \text{ mV}$ and moderate $V_d = \pm 200 \text{ mV}$ drain biases for both n- and p-type GAA-NS-FETs. For the $4 \times 12 \text{ nm}^2$ nanosheet cross-section, the resulting $I_d(V_g)$ characteristics are presented in Figs. 4 and 5 for the n- and p-channel devices, respectively, considering both the (001) and (110) substrate orientations. The threshold voltages, DIBL, and SS slope are extracted with conventional methods. The corresponding DIBL and SS values for all twelve device configurations are summarized in Tables II and III, respectively.

Despite differences in geometry and doping profile, the simulated DIBL values for the $L_g = 6 \text{ nm}$ devices are in very good agreement with the experimental results reported in [2].

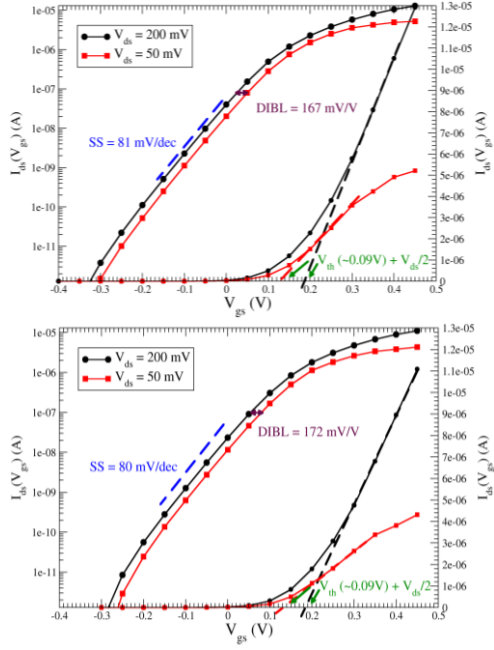


Fig. 4. $I_d(V_g)$ characteristic curves at low (50 mV) and moderate (200 mV) V_d for an n-Si GAA-NS-FET of $4 \times 12 \text{ nm}^2$ cross-section oriented (001) (top), (110) (bottom). The DIBL in mV/V is indicated in purple, the subthreshold slope in mV/dec is in blue, and the threshold voltage in V is in green.

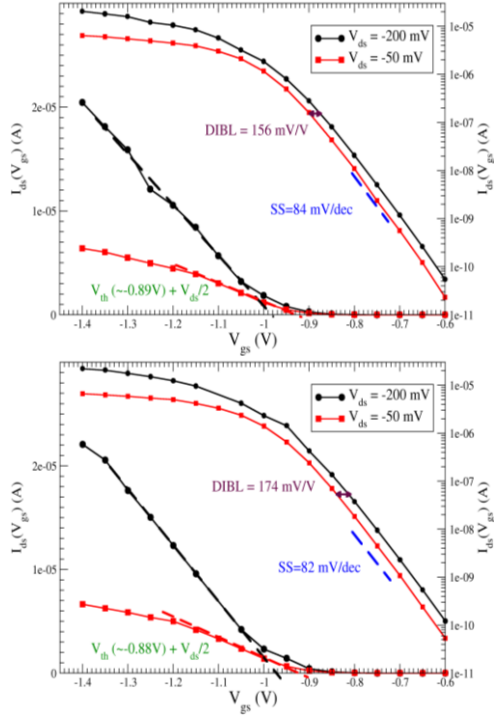


Fig. 5. $I_d(V_g)$ characteristic curves at low (-50 mV) and moderate (-200 mV) V_d for a p-Si GAA-NS-FET of $4 \times 12 \text{ nm}^2$ cross-section oriented (001) (top), (110) (bottom). The DIBL in mV/V is indicated in purple, the subthreshold slope in mV/dec is in blue, and the threshold voltage in V is in green.

Moreover, a significant reduction in DIBL is observed as the silicon channel thickness decreases, highlighting the improved electrostatic control provided by thinner nanosheets. This improvement is accompanied by a slight reduction in the subthreshold slope (SS), in agreement with the experimental observations reported in [2].

TABLE II. DRAIN-INDUCED BARRIER LOWERING (DIBL, mV/V) AS A FUNCTION OF SILICON CHANNEL THICKNESS T_{Si} AND SUBSTRATE ORIENTATION. THE FIRST TWO ROWS CORRESPOND TO THE PRESENT SIMULATIONS, WHILE THE THIRD ROW REPORTS THE EXPERIMENTAL VALUES EXTRACTED FROM FIG. 11 OF [2].

T_{Si}	4 nm	3 nm	2 nm
(001) N-/P-	167	156	124
(110) N-/P-	172	174	120
Intel[2] N-/P-	125	175	110

TABLE III. SUBTHRESHOLD SLOPE (SS, mV/DEC) AS A FUNCTION OF SILICON CHANNEL THICKNESS T_{Si} AND SUBSTRATE ORIENTATION. THE FIRST TWO ROWS CORRESPOND TO THE PRESENT SIMULATIONS, WHILE THE THIRD ROW REPORTS THE EXPERIMENTAL VALUES EXTRACTED FROM TABLE I OF [2].

T_{Si}	4 nm	3 nm	2 nm
(001) N-/P-	81	84	74
(110) N-/P-	80	82	73
Intel[2] N-/P-			66

B. Mobility, Injection Velocity

The effective mobility, μ_{eff} is extracted from the channel charge Q_{ch} , obtained from the atomistic NEGF carrier density by integrating the charge over the channel region. At low drain bias, μ_{eff} is evaluated for a range of gate voltages using

$$\mu_{eff} = I_{ds} \times L_{ch} / W \times Q_{ch} \times V_{ds} \quad (1)$$

where I_{ds} is the drain current, L_{ch} is the channel length, W is the nanosheet width, and V_{ds} is the drain bias. The resulting effective mobility is plotted as a function of the channel inversion charge N_{inv} in Figs. 6 and 7 for the n- and p-channel GAA-NS-FETs, respectively.

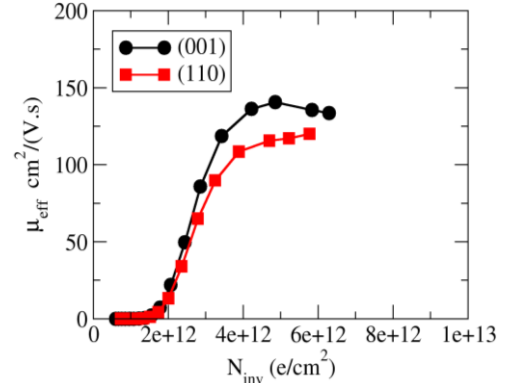


Fig. 6. Effective mobility of n-Si GAA-NS-FET of $4 \times 12 \text{ nm}^2$ cross-section, as a function of channel inversion charge for two substrate orientations (001) and (110).

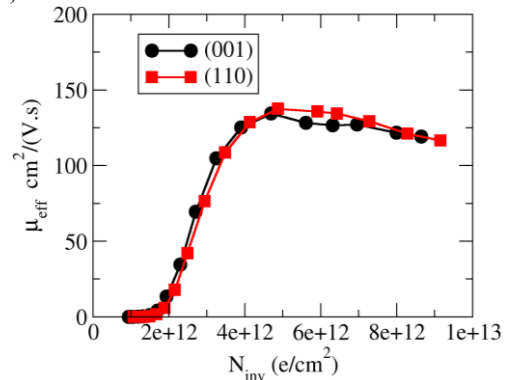


Fig. 7. Effective mobility of p-Si GAA-NS-FET of $4 \times 12 \text{ nm}^2$ cross-section, as a function of channel inversion charge for two substrate orientations (001) and (110).

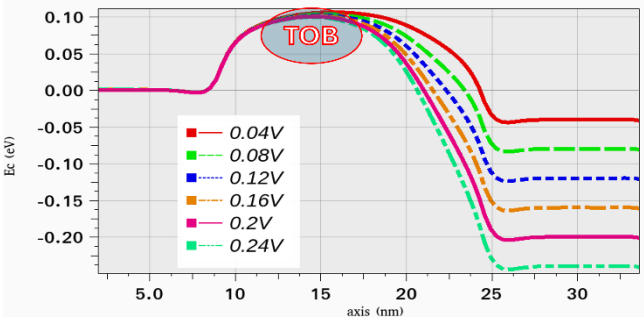


Fig. 8. Top of the barrier (TOB) of an n-Si GAA-NS-FET of $2 \times 12 \text{ nm}^2$ cross-section. The 1D electrostatic band profile is visualized along the NS longitudinal direction for several V_{ds} voltages with a constant gate voltage V_g slightly above threshold.

Figures 6 and 7 show a peak effective mobility of approximately $150 \text{ cm}^2/(\text{V}\cdot\text{s})$. The n-channel GAA-NS-FET exhibits higher mobility for the (001) substrate orientation than for the (110) orientation, while the p-channel device shows no significant orientation dependence.

Because transport in a GAA-NS-FET with a 6 nm gate length is quasi-ballistic, the concept of carrier mobility becomes less meaningful. We therefore focus on the extraction of the injection velocity, V_{inj} , using the top-of-the-barrier (TOB) model [6]. For each $I_{ds}(V_{ds}, V_{gs})$ bias condition, the TOB is identified from the electrostatic potential profile Fig. 8, and the atomistic charge, Q_{TOB} , is obtained by integrating the quantum-mechanical carrier density over a small volume centered on the TOB. The injection velocity, V_{inj} is then evaluated at sufficiently high V_{ds} using

$$V_{inj} = I_{ds} / W \times Q_{TOB} \quad (2)$$

The results presented in Figs. 9 and 10 are consistent with the asymptotic experimental trends reported in [2]. Interestingly, the n-channel GAA-NS-FET exhibits a higher injection velocity on the (001)-oriented substrate, whereas the p-channel device performs better on the (110)-oriented substrate. This orientation dependence is consistent with the mobility trends reported in [7] for longer-channel devices. This suggests that the detailed band structure and underlying quantum transport mechanisms remain influential in the quasi-ballistic transport regime.

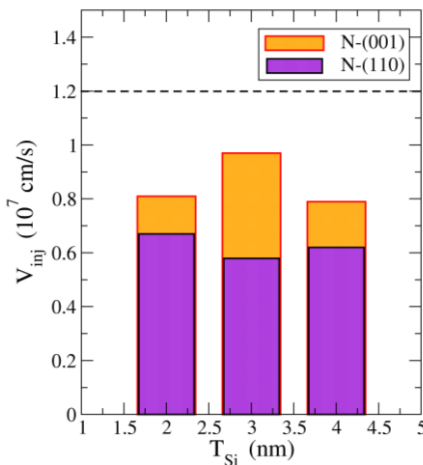


Fig. 9. Injection velocity V_{inj} of n-Si GAA-NS-FETs for several thicknesses $T_{Si} = 2, 3, 4 \text{ nm}$, width $W = 12 \text{ nm}$, and two substrate orientations. The V_{inj} is higher for the (001) orientation.

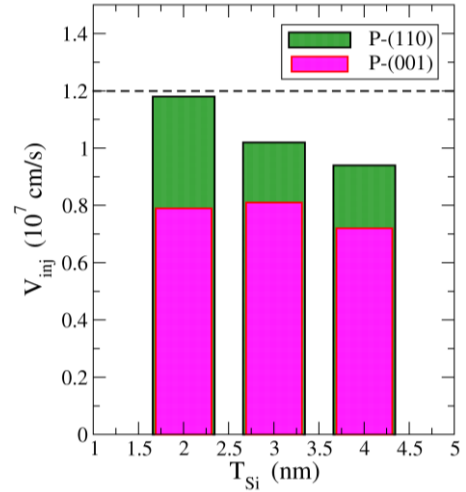


Fig. 10. Injection velocity V_{inj} of p-Si GAA-NS-FETs for several thicknesses $T_{Si} = 2, 3, 4 \text{ nm}$, width $W = 12 \text{ nm}$, and two substrate orientations. The V_{inj} is higher for the (110) orientation.

IV. CONCLUSION

A thorough study of a GAA-NS-FET with a 6 nm gate length has been performed using atomistic NEGF. The simulated electrostatic and transport characteristics, including DIBL, subthreshold slope, effective mobility, and injection velocity, are in good agreement with recent experimental observations. The results demonstrate that reducing the silicon thickness below 3 nm systematically improves the device electrostatics and transport performance without introducing detrimental effects. The analysis further highlights the importance of atomistic band-structure modeling, showing that crystallographic orientation influences carrier transport even in the quasi-ballistic regime. These findings confirm the predictive capability of atomistic NEGF simulations for the optimization and design of next-generation GAA-NS-FETs in the Ångström era.

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REFERENCES

- [1] International Roadmap for Devices and Systems (IRDS) 2024 Edition
- [2] A. Agrawal *et al.*, "Silicon RibbonFET CMOS at 6nm Gate Length," *Proc. IEEE IEDM*, San Francisco, CA, USA, 2024, pp. 1-4
- [3] S. Steiger, M. Povolotskyi, H.-H. Park, T. Kubis, and G. Klimeck, "Nemo5: A Parallel Multiscale Nanoelectronics Modeling Tool," *IEEE Trans Nano*, vol. 10, p. 1464, 2011
- [4] P. Blaise *et al.*, "Nanoscale FET: How To Make Atomistic Simulation Versatile, Predictive, and Fast at 5nm Node and Below," *Proc. SISPAD*, Kobe, Japan, 2020, pp. 249-252
- [5] Lemus, D.A., Charles, J., Kubis, T., "Mode-Space-Compatible Inelastic Scattering in Atomistic Nonequilibrium Green's Function Implementations," *J Comput Electron* 19, 1389–1398 (2020)
- [6] Lundstrom, Mark, "Fundamentals of Nanotransistors," *Lessons from Nanoscience: A Lecture Notes Series*, World Scientific, 2017
- [7] S. Mochizuki *et al.*, "Evaluation of (110) versus (001) Channel Orientation for Improved nFET/pFET Device Performance Trade-Off in Gate-All-Around Nanosheet Technology," *Proc. IEEE IEDM*, San Francisco, CA, USA, 2023, pp. 1-4