

Multi-subband Monte Carlo Simulation of Scaled Forksheet FETs

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Abstract—We simulate forksheet-based transistors at sub-2nm dimensions with a multi-subband Monte Carlo simulator taking into account quantum confinement effects and source-to-drain tunneling. We compute their performance and subthreshold behavior to determine their scaling limit.

Index Terms—Monte Carlo, multi-subband, forksheets, nanosheets

I. INTRODUCTION

The Forksheet (FS) Field-Effect Transistor (FET) has emerged as the main architecture for sub-2nm CMOS scaling [1], specifically addressing the physical limitations of the n-top separation inherent in Nanosheet (NS) FET designs. Despite the lack of the gate at one of the lateral sides (Figure 1), the electrostatic integrity of FS FETs has been shown to be similar to NS FETs [2]. However, if the channel length is scaled aggressively, the short channel behavior is deteriorated, due to the lack of a complete surrounding gate. In this work, we study the scaling properties of the n-side of FS FETs employing a multi-subband Monte Carlo simulator, which fully takes into account the 2D lateral quantum confinement and accurately models the 3D charge distribution inside the channel of the device.

II. SIMULATION TOOL AND DEVICE STRUCTURE

For this study, we employ MULHACEN [3], an advanced multi-subband simulator for n-channel devices based on the mode-space approach: it self-consistently combines the solution of the 2D Schrödinger equation in several device cross sections with 1D Monte Carlo transport and 3D Poisson equation. The transport treatment is based on the classical Boltzmann equation, paired with the quantum mechanical description of the scattering mechanisms. Moreover, we included Source to Drain Tunneling (SDT) by allowing the simulation particles to overcome the barrier according to the tunnel probability computed with the Wentzel–Kramers–Brillouin (WKB) approximation.

The first simulated structure is a single channel of an n-type FS FET, representative of a 2nm technological node, as shown in Figure 1a). The height and width of the silicon channel are 5 nm and 20 nm, respectively. The interfacial

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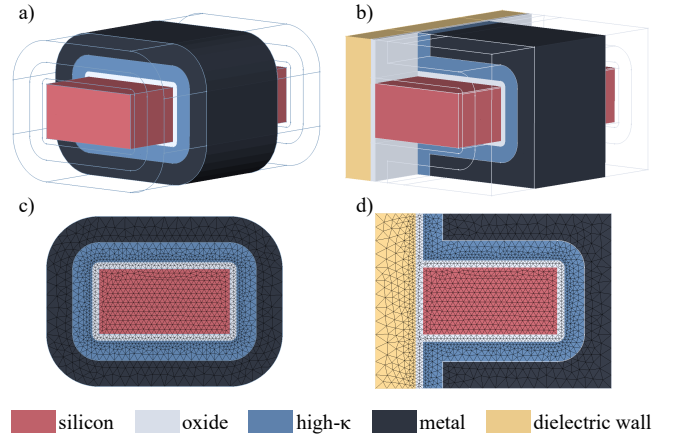


Fig. 1. Simulated structures: a),c) nanosheet, b),d) forksheet. Panels a) and b) show the 3D structures, with the spacers hidden in order to show the channel and the gate stack. Panels c) and d) show a cross section of the devices, showing how the meshing adapts to the geometry.

SiO_2 layer thickness is 0.5 nm, surrounded by a 1.4 nm thick HfO_2 layer; nitride dielectric wall and spacers ($L_{sp} = 5$ nm) are included in the structure description. Source and drain doping is $N_D = 1 \times 10^{21} \text{ cm}^{-3}$ with Gaussian decay, the vertical pitch between channels is 10 nm, and the metal work function is set at 4.41 eV. To inspect the electrostatic integrity, the gate length, L_G , is scaled down to 8 nm and the results are compared to NS based devices, as shown in Figure 1b), with the same dimensions. For comparison, we also simulate structures without an high- κ dielectric, substituted by a SiO_2 layer with the Equivalent Oxide Thickness (EOT), that is $t_{EOT} = 0.77$ nm.

III. RESULTS

Figures 2a) and b) show the transfer and output curves, respectively, of a single n-channel forksheet with $L_G = 14$ nm, comparing the results (solid curves) to those obtained without SDT (dashed curves). It is well known that SDT negatively affects the OFF current and the subthreshold behavior of transistors with channel length below 10 nm [4]. In this case, at $L_G = 14$ nm, the subthreshold behavior is barely affected by tunneling but we observe an important difference, especially at large values of V_G and V_D . This behavior can be understood by inspecting Figure 3: at low gate and drain bias, the barrier is too wide and high to allow a significant tunneling current.

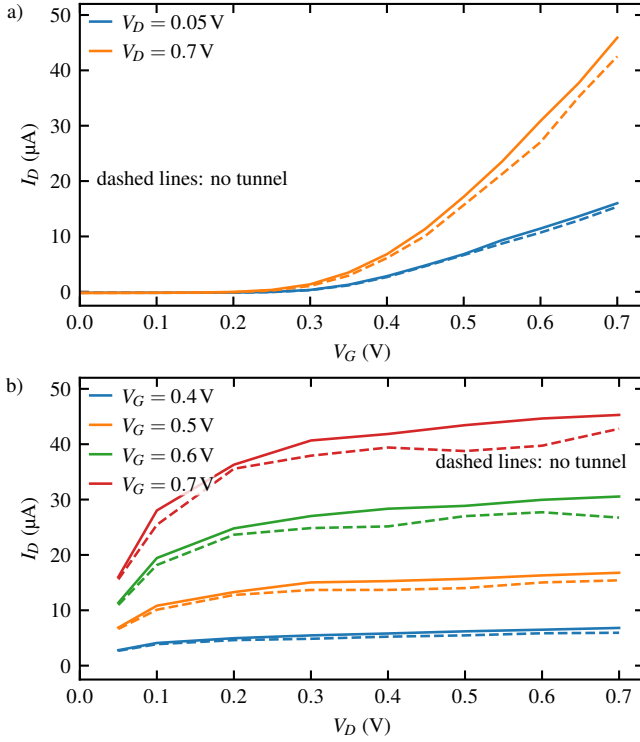


Fig. 2. a) Transfer curves for $V_D = 0.05$ V and $V_D = 0.7$ V. b) Output curves for different values of V_G . In both panels, the dashed curves represent the results obtained neglecting SDT.

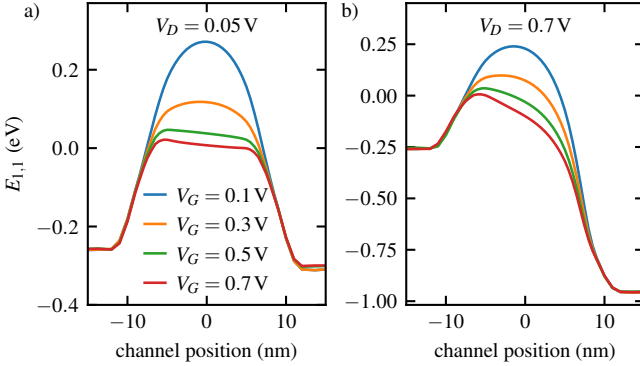


Fig. 3. Fundamental subband energy as a function of position along the channel for a) $V_D = 0.05$ V and b) $V_D = 0.7$ V and different values of V_G , showing that, near the top of the barrier, the barrier length decreases for large values of V_D and V_G .

However, at large values of V_G and V_D the barrier, near its top, becomes narrower and allows tunneling probability to increase.

To assess the scaling behavior, we compute the threshold voltage, V_{th} , for devices with different L_G down to 8 nm. Since the numerical Monte Carlo results are inherently noisy, we employ the constant current method [5] with $I_{Dcc} = 5 \times 10^{-7} \text{ A} \times W_{eff}/L_G$, where W_{eff} is the effective perimeter of the cross section. Now, the study of the subthreshold behavior of these transistors needs a deeper analysis. Despite the statistical

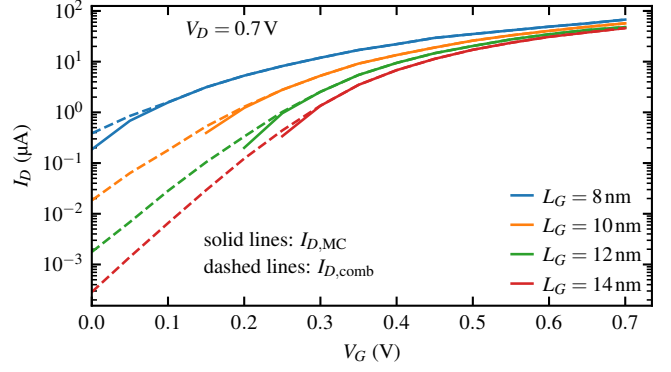


Fig. 4. Transfer curves in logarithmic scale for FS devices with different gate lengths from 8 nm to 14 nm. The solid curves represent the Monte Carlo result, $I_{D,MC}$, truncated at V_G values where the corresponding standard deviation becomes larger than the current itself. The dashed curves represent the combined curves, computed according to Eq. (1).

enhancements implemented in the MULHACEN simulator [6], in these simulations, the subthreshold behavior presents large statistical fluctuations where, for several values of the gate voltage V_G , the computed estimation of the drain current $I_{D,MC}$ is smaller than the estimation of its standard deviation. Therefore, to obtain the Subthreshold Swing (SS), we employ the current $I_{D,bal}$ computed by the Landauer formula [7] for each of the subbands, taking into account their self-consistent profile. The Landauer approach assumes ballistic transport, so that the absolute current levels do not take into account the full physics of the simulation. However, since SS is mainly determined by the electrostatic behavior, we assume that the obtained SS values are reliable. Thus, we can obtain a “combined” current $I_{D,comb}$ without large oscillations and noise in the subthreshold region by multiplying the ballistic current by a constant factor given by the ratio of the Monte Carlo and ballistic currents at $V_G = V_{th}$:

$$I_{D,comb}(V) = \begin{cases} I_{D,MC}(V) & \text{for } V \geq V_{th} \\ I_{D,bal}(V) \frac{I_{D,MC}(V_{th})}{I_{D,bal}(V_{th})} & \text{for } V < V_{th} \end{cases} \quad (1)$$

The resulting current curves are shown in Figure 4 for $V_D = 0.7$ V and different values of L_G .

The results obtained for V_{th} , SS and the Drain Induced Barrier Lowering (DIBL) for the FS devices down to $L_G = 8$ nm are shown as blue lines in Figure 5. As expected, we observe a relevant threshold voltage roll-off: V_{th} strongly decreases with the gate length. Since we employ the constant current method to compute V_{th} , the results without tunneling imply a smaller value: a smaller V_G is needed to obtain the same I_D . On the contrary, tunneling does not affect in a significant way the SS for $L_G = 14$ nm but its relevance increases as the gate length is scaled down, in line with expectations. The DIBL also steadily increases for decreasing L_G , coupled with an increase of the effect of tunneling. In general, we can observe that the electrostatic integrity is severely compromised below $L_G = 12$ nm. In Figure 5, we also show the results obtained for NS devices. Even if the electrostatic integrity is severely

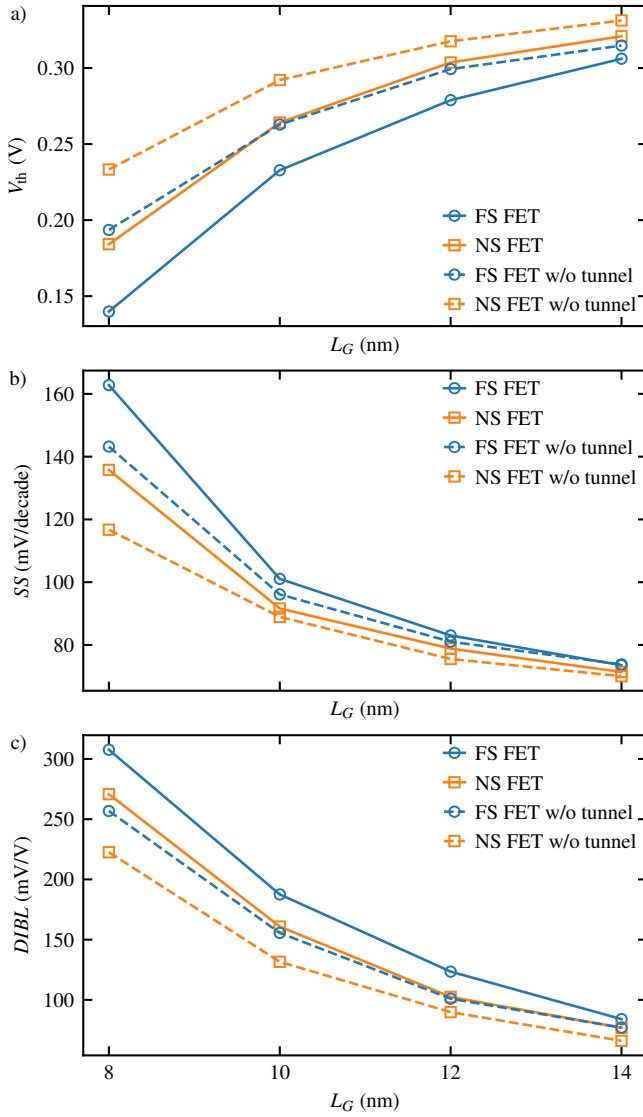


Fig. 5. a) Threshold voltage (V_{th}), b) Subthreshold swing (SS) and c) drain induced barrier lowering (DIBL) as a function of L_G for FS devices and NS devices, taking into account SDT or neglecting it.

compromised below $L_G = 12$ nm, the NS devices present a generally better scaling behavior. This means that the absence of the gate on a lateral side of the original FS indeed worsens its electrostatic behavior, as expected.

To get more details and insights into the loss of electrostatic integrity, we also compute the SS and the DIBL for devices where the high- κ insulator is replaced with an equivalent oxide (FS EOT), and show them in Figure 6. We can observe that, especially for FS devices, the use of an equivalent oxide thickness improves the electrostatic behavior. In general, for non-planar devices, the concept of equivalent oxide thickness is not as straightforward as in planar devices because of the effect of the corners [8]. However, the effect is quite stronger in the case of FS FETs with respect to NS FETs,

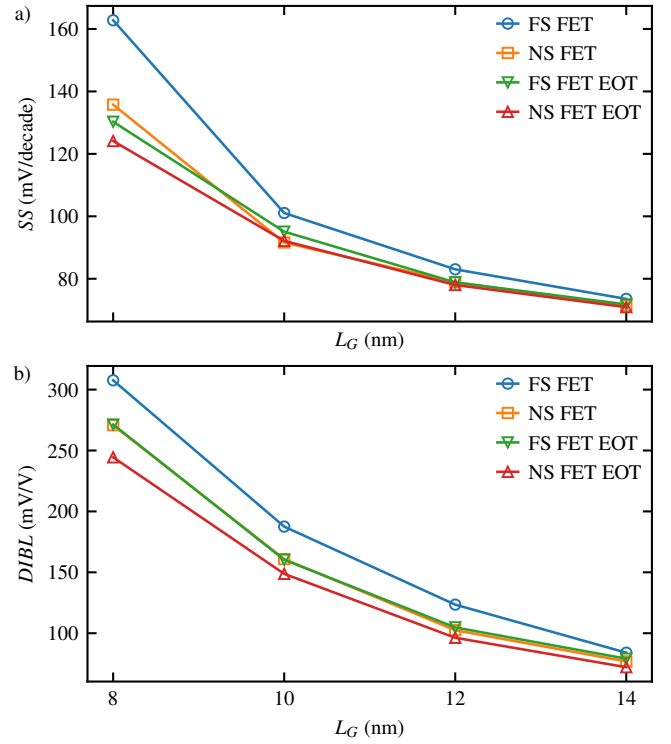


Fig. 6. a) Subthreshold swing (SS) and b) drain induced barrier lowering (DIBL) as a function of L_G for FS devices (FS FET), FS devices with high- κ insulator substituted with an equivalent oxide (FS FET EOT), NS devices (NS FET) and FS with high- κ insulator substituted with an equivalent oxide (NS FET EOT). All curves are computed including SDT.

especially regarding the SS. The reason for this behavior can be understood by inspecting the cross section of the device, as shown in Figure 1d). We can observe that the presence of a thick insulator moves the gate away not only from the surface of the channel, but also from the dielectric gate. Therefore, near the dielectric wall there is a section of the semiconductor sheet which is not covered by the gate, and this region is smaller when a thinner oxide is used, such as when the supposedly “equivalent” oxide thickness is employed. We can conclude that the absence of a thick insulator mitigates the drawback of a non-complete gate and allows the side of the channel to be better controlled by it.

Figure 7 validates this interpretation showing that in the original device the gate loses control over the side of the channel near the dielectric wall at $V_G = 0$ V, clearly with respect to the NS device, Figure 7c), but also with respect to the FS EOT device, Figure 7b). However, at large V_G , when the device is ON, the difference is not so large as shown in Figures 7e) and f), and the drain current is similar in both cases. In this instance, the difference is also smaller with respect to the NS case.

Finally, the comparison between Figure 7c) and Figure 7d) at $V_G = 0$ V and Figure 7g) and Figure 7h) at $V_G = 0.7$ V shows that for NS devices the thinner oxide with EOT is almost equivalent to the one with the high- κ insulator.

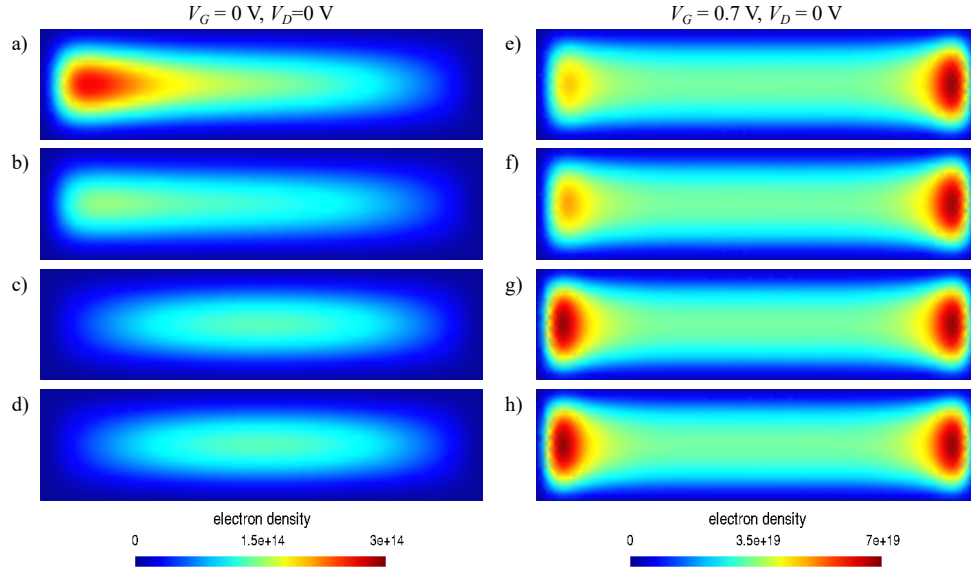


Fig. 7. Electron density in a cross section at the center of a device with $L_G = 14$ nm for a), e) FS devices, b), f) FS devices with high- κ insulator replaced by an equivalent oxide, c), g) NS devices and d), h) NS devices with high- κ insulator replaced by an equivalent oxide. The figures correspond to $V_D = 0$ V and a), b), c), d) $V_G = 0.0$ V and e), f), g), h) $V_G = 0.7$ V. The dielectric wall is located on the left side of the FS devices as in Figure 1.

IV. CONCLUSIONS

We simulated the electrical behavior of n-channel FS FETs for sub-2nm scaling. We showed that source to drain tunneling impacts the ON current and only marginally affects the sub-threshold behavior for $L_G = 14$ nm. For shorter channels, the electrostatic behavior worsens because the gate is kept far from the side of the channel by the thick high- κ insulator wrapping the dielectric wall. The comparison with NS shows that, for devices with dimensions considered in this study, the main part of the loss in the electrostatic behavior can be recovered in a structure with a thinner oxide.

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