

Low-Temperature Behavior in Silicon Nanowire n-FETs Studied by Atomistic NEGF

Sanam Moslemi-Tabrizi
Ciena Inc.
Ottawa, Canada
smoslemi@ciena.com

Peter Schvan
Ciena Inc.
Ottawa, Canada

Philippe Blaise
Silvaco Inc.
Grenoble, 38000 France
philippe.blaise@silvaco.com

Udita Kapoor
Silvaco Inc.
Santa Clara, CA 95054, USA

Daniel Lemus
School of Electrical and Computer
Engineering
Purdue University
West Lafayette, IN 47907, USA

Tillmann Kubis
School of Electrical and Computer
Engineering
Purdue University
West Lafayette, IN 47907, USA

Abstract— The low-temperature operation of silicon gate-all-around nanowire n-FETs (GAA-NW-FETs) is investigated using atomistic quantum transport simulations based on the non-equilibrium Green's function (NEGF) formalism, including electron-phonon scattering down to 2 K. The simulated temperature dependence of the subthreshold slope is in good agreement with published experimental data for silicon FETs, validating the modeling approach. The simulations further reveal that inner dielectric spacers produce strong electrostatic confinement, leading to localized quantum states near the conduction-band edge. While these states have a negligible impact on the current at intermediate temperatures, they become energetically and spatially resolved at cryogenic temperatures, where they can accommodate only a few electrons. The associated gate-coupling capacitance and lever-arm factor are extracted, demonstrating the atomistic NEGF approach's capability to describe the quantum properties of GAA-NWFETs at cryogenic temperatures.

Keywords—Simulation, Atomistic, NEGF, GAA-FET, Nanowire, Quantum confinement, Cryogenic, Localized states.

I. INTRODUCTION

CMOS scaling has facilitated the adoption of nanosheet and nanowire FETs, with characteristic dimensions of only a few nanometers [1]. In parallel, there is a renewed interest in operating devices at cryogenic temperatures, particularly for high-performance computing, advanced memories, and quantum and cryo-CMOS applications [2]. In this regime, carrier transport is affected by quantum confinement and energy level discretization. Conventional TCAD approaches, based on the effective mass approximation and semiclassical transport, are unable to model these quantum effects with the required accuracy and often exhibit convergence issues below a few tens of kelvins [3]. To overcome these limitations, we use atomistic NEGF simulations to systematically analyze confinement, energy-level separation, and state occupancy in Si GAA-NW-FET from 300 K to 2 K.

II. METHODOLOGY

Simulations are performed using Victory Atomistic [4], an atomistic NEGF solver derived from NEMO5 [5]. The electronic structure is described using an $sp^3d^5s^*$ tight-binding basis, ensuring accurate modeling of confined states near the silicon band edges. In steady state, self-consistency between the NEGF and Poisson equations is achieved at a low drain bias, $V_{ds} = 10$ mV. The electron-phonon interactions are included thanks to the self-consistent Born approximation.

TABLE I. PHYSICAL DIMENSIONS OF THE Si <100> GAA-NW-FETs, DIELECTRIC PROPERTIES, AND DOPING.

Parameter	Value/range
Cross-section	2x2, 2x3 nm ²
L_S, L_D	20 to 40 nm
L_{CH}	19 to 33 nm
L_{S1}, L_{S2}	7 to 14 nm
L_G	5 nm
t_{OX}	1 nm
$\epsilon_{S1,S2}$	4 to 20 (ϵ_0)
ϵ_G (SiO ₂)	3.9 (ϵ_0)
Doping (CH)	10^{15} (e.cm ⁻³)
Doping (S, D)	10^{20} (e.cm ⁻³)

The acoustic and optical phonon branches are described using bulk silicon parameters, which capture the dominant effects of electron-phonon scattering on the current characteristics and energy-level broadening. Numerical efficiency is achieved through a low-rank approximation matrix [6] and adaptive energy grids with a resolution better than 0.1 meV at 2 K.

The baseline device is illustrated in Figs. 1 and 2: a silicon <100>-oriented GAA-NW-FET with an intrinsic channel, an equivalent-oxide-thickness of 1 nm, heavily doped source and drains, and dielectric spacers. The device parameters employed in our simulations are summarized in Table I.

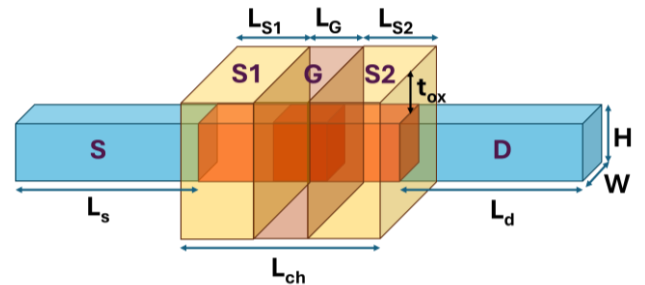


Fig. 1. Schematic of the GAA-NW-FET with a square cross-section including dielectric spacers with the various characteristic lengths. The device parameters are listed in Table I.

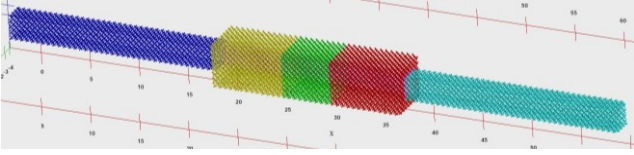


Fig. 2. Atomistic structure of a $2 \times 2 \text{ nm}^2$ $\langle 100 \rangle$ Si nanowire with the source (blue) and drain (turquoise) of 20 nm length each, gate of 5 nm (green), and dielectric spacers (yellow and red) of 7 nm each.

III. RESULTS

A. Validation Against Published Subthreshold Slope Data

Before analyzing the cryogenic confinement regime, we focus on the simulated temperature dependence of the subthreshold slope (SS) against published experimental data for Si MOSFETs.

Fig. 3 shows the simulated drain current I_{ds} as a function of gate voltage V_g at four temperatures ranging from 300 K to 2 K, under low drain bias $V_{ds} = 10 \text{ mV}$.

Table II compares our simulations with the measurements of Beckers et al. [7]. Although their study considers bulk planar MOSFETs while our work focuses on a $2 \times 2 \text{ nm}^2$ GAA-NW-FET with a 5 nm gate length, the simulated SS reproduces the expected temperature scaling and agrees well with the experimental values at 300 K and 20 K. At lower temperatures, however, the simulated SS deviates more strongly from the ideal thermal limit, increasing from an 8% excess at 300 K (64 vs. 59.5 mV/dec) to 77% at 20 K (7 vs. 3.96 mV/dec).

This enhanced deviation indicates the onset of non-thermionic transport. As thermionic emission is suppressed at cryogenic temperatures, localized states induced by the dielectric spacers become energetically resolved and provide an additional subthreshold conduction path. Their contribution, discussed in Section III.B, explains both the SS degradation at 20 K and the larger deviation observed at low temperature in the GAA-NW-FET, Section III.D.

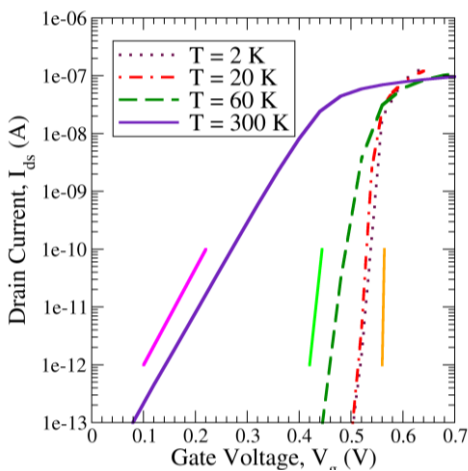


Fig. 3. $I_d(V_g)$ current transfer characteristic at $T = 2 \text{ K}$, 20 K , 60 K and 300 K , $V_{ds} = 10 \text{ mV}$, along with the ideal slopes of 4 mV/dec (orange), 12 mV/dec (green) and 60 mV/dec (magenta).

TABLE II. COMPARISON OF SIMULATED SUBTHRESHOLD SLOPE (THIS WORK, GAA NW-FET, $2 \times 2 \text{ nm}^2$) AGAINST EXPERIMENTAL DATA FROM BECKERS ET AL. [7] (BULK PLANAR Si MOSFET).

Temperature (K)	SS This work (mV/dec)	SS Beckers et al. [7] (mV/dec)	Ideal kT/q (mV/dec)
300	~64	~65-70	59.5
20	~7	~7-10	3.96

B. Confinement and Localized States

At low drain bias, the GAA geometry provides excellent electrostatic control. At temperatures down to 60 K, several localized states form below the top of the barrier due to quantum confinement. At 20 K, confined states clearly detach from the conduction band once the gate voltage V_g exceeds approximately 0.5 V; see Fig. 4.

In Fig. 5, increasing spacer length has a limited impact on confinement, whereas reducing the spacer dielectric constant significantly deepens the quantum well and enhances energy confinement.

Increasing V_g allows the two lowest-energy states to be progressively filled with electrons, while higher-energy states exhibit different spatial symmetries along the transport direction (Figs. 4 and 6). Lowering the temperature to 2 K reveals an additional splitting of $\sim 1 \text{ meV}$ in the lowest-energy levels without increasing the total trapped charge (Fig. 6).

While the localized states become well defined at low temperature, their observability is ultimately limited by scattering-induced broadening. In particular, electron-phonon coupling determines the energy resolution of these states, and thus whether closely spaced levels can be experimentally distinguished. This effect is analyzed quantitatively in the following section.

C. Phonon-Induced Level Broadening

The electron-phonon coupling that limits individual state resolution at 2 K (Fig. 7) can be characterized quantitatively through the full width at half maximum (FWHM) of the DOS peaks corresponding to the two lowest confined levels. Table III summarizes the FWHM values extracted directly from Fig. 7 at $T = 2 \text{ K}$, alongside the observed level splitting from Fig. 6 at $T = 20 \text{ K}$ and $T = 2 \text{ K}$.

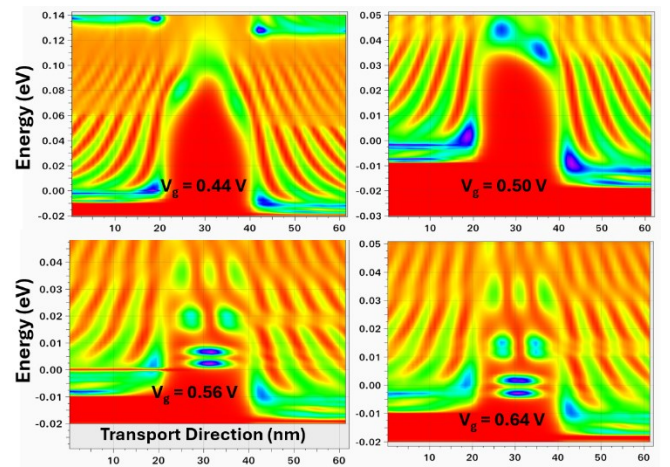


Fig. 4. Density of states resolved in energy along the transport axis at $T = 20 \text{ K}$, $V_{ds} = 10 \text{ mV}$, for four different values of $V_g = 0.44, 0.5, 0.56, 0.64 \text{ V}$. Two localized states appear at $V_g = 0.56 \text{ V}$, slightly below the top of the barrier. These two states are pushed lower in energy as V_g increases, followed by other states showing a different symmetry.

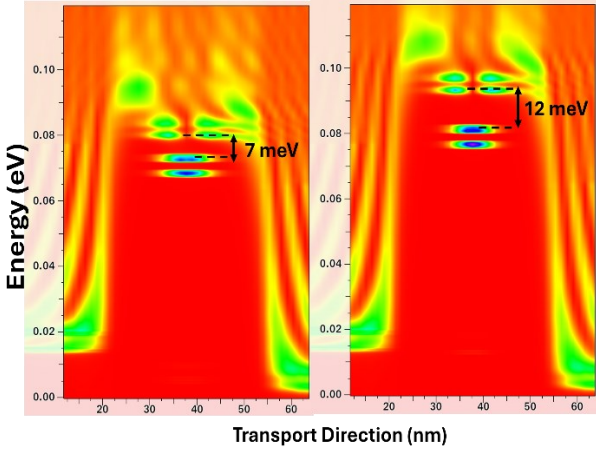


Fig. 5. DOS(E, x) along the transport axis at $T = 20$ K, $V_{ds} = 10$ mV, $V_g = 0.57$ V using long spacers of length 14 nm, and with two different dielectric constants $\epsilon = 12$ (left), $\epsilon = 4$ (right). A lower dielectric constant helps in confining the electronic levels.

The comparison between the FWHM and the energy-level splitting is key to the physical interpretation of the results. At $T = 20$ K, the FWHM of the two lowest levels is 2.6 meV and 2.8 meV, respectively, while the splitting between them is 5 meV — the states are therefore well resolved. At $T = 2$ K, the FWHM narrows to 1.8 meV for Level 1 and ~ 1.0 meV for Level 2, consistent with reduced phonon scattering at lower temperature. However, the additional ~ 1 meV sub-splitting of Level 1 observed at 2 K is comparable to its FWHM of ~ 1.8 meV, yielding a FWHM-to-splitting ratio of ~ 1.8 .

This confirms that individual state resolution within the sub-split manifold requires temperatures below 2 K, where further narrowing of the broadening would be needed to resolve the 1 meV splitting.

Both acoustic and optical phonon branches contribute to the broadening within the self-consistent Born approximation. At 2 K, acoustic phonon scattering is expected to dominate since the optical phonon occupation number $n_{BE} (\hbar\omega_{op}/kT)$ is exponentially suppressed for $\hbar\omega_{op} \sim 60$ meV $\gg kT \sim 0.17$ meV. The reduction in FWHM from 20 K to 2 K — by approximately 30% for Level 1 — is consistent with this acoustic-dominated regime.

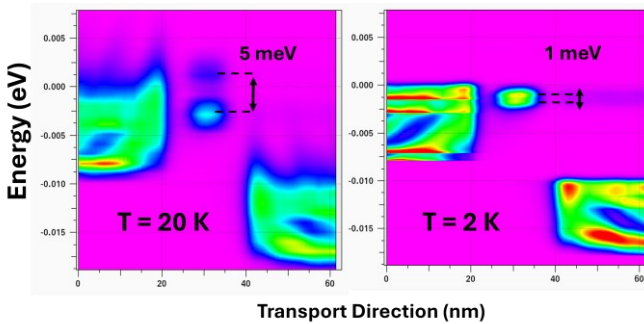


Fig. 6. Electronic density resolved in energy along the transport axis at $T = 20$ K vs 2 K, $V_{ds} = 10$ mV, $V_g = 0.64$ V. At $T = 20$ K, a 5 meV level splitting is observed. At $T = 2$ K, a second 1 meV splitting occurs for the lowest-energy levels, with the progressive filling of these levels remaining almost unchanged.

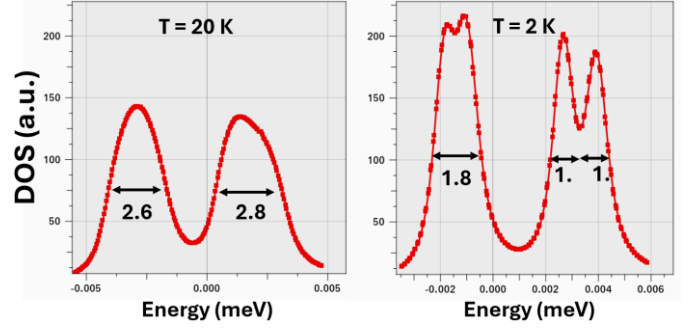


Fig. 7. Electron-phonon-induced broadening of the lowest-energy electronic states in the transistor channel at $T = 20$ K (left) and $T = 2$ K (right), with $V_{DS} = 10$ mV and $V_G = 0.64$ V. The broadening of each state is extracted from its full width at half maximum (FWHM). The NEGF simulations include both acoustic and optical phonon scattering within the self-consistent Born approximation.

D. Temperature-Dependent Transfer Characteristic

Fig. 3 shows the simulated drain current I_{ds} as a function of gate voltage V_g at four temperatures ranging from 300 K to 2 K, under low drain bias ($V_{ds} = 10$ mV).

At 300 K, the subthreshold region is broad and gradual due to thermal broadening of the Fermi-Dirac distribution, with thermionic emission over the gate-induced barrier dominating off-state conduction. As the temperature decreases, the carrier distribution sharpens toward a step-like function, resulting in a steeper subthreshold swing.

At 20 K and 2 K, the transfer characteristics nearly overlap, and the subthreshold slope approaches its thermal limit ($\sim kT/q$). This convergence indicates that the thermal energy becomes much smaller. Therefore, channel occupation is primarily governed by discrete quantum level alignment rather than thermal excitation. Fig. 6 provides a signature of this coupling and its effect on the tunneling current. Not only are the localized electronic levels filled when they align with the source electrode levels on the left part of the device, but they also contribute to tunneling, as the slight bluish echo reveals above the drain electrode levels on the right part of the device.

TABLE III. FWHM OF THE TWO LOWEST CONFINED ENERGY LEVELS EXTRACTED FROM FIG. 7 ($V_{DS} = 10$ mV, $V_G = 0.64$ V), COMPARED AGAINST THE LEVEL SPLITTINGS OBSERVED IN FIG. 6.

Quantity	Level 1 (lowest)	Level 2
FWHM $T = 20$ K	2.6 meV	2.8 meV
FWHM $T = 2$ K	1.8 meV	1.0 meV
Level splitting $T = 20$ K (from Fig. 6)	5 meV (between levels 1 and 2)	
Additional splitting $T = 2$ K (from Fig. 6)	1 meV (sub-splitting of level 1)	
FWHM / splitting ratio at 2 K	1.8 (broadening > sub-splitting)	

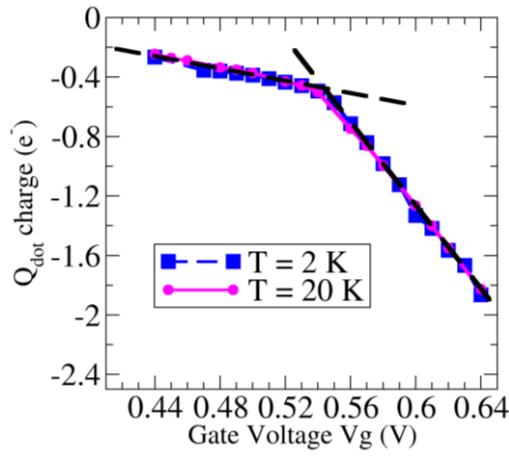


Fig. 8. Total electronic charge captured by the localized states of the lowest-energy function of V_g at $T = 2\text{ K}$ and 20 K . The total charge follows a quasi-linear law for $V_g = [0.56, 0.64]\text{ V}$.

E. Gate Coupling Capacitance and Lever Arm Factor

The net charge stored in the confined states increases linearly with gate voltage over the range $V_g = 0.56\text{--}0.64\text{ V}$, independently of temperature between 20 K and 2 K (Fig. 8). This behavior indicates a purely capacitive coupling regime, with an effective gate-coupling capacitance of approximately 2 aF . This capacitive behavior is corroborated by the density-of-states analysis shown in Fig. 9. The energies of the first three localized states in the channel shift linearly toward lower energies as the gate voltage increases, as illustrated in Fig. 10. From this linear dependence, a gate lever-arm factor of 27 meV/V is extracted.

IV. CONCLUSION

Atomistic NEGF simulations provide a detailed description of silicon nanowire FETs at cryogenic temperatures. The simulated subthreshold slope agrees with published experimental data at 300 K and 20 K , validating the temperature-dependent transport model. Strong transverse confinement and inner dielectric spacers induce localized quantum states that trap a few electrons and remain capacitively coupled to the gate. Low-temperature NEGF simulations further enable the extraction of an effective gate-coupling capacitance and the corresponding gate lever-arm factor, providing a quantitative characterization of the

confined states. Electron-phonon interactions broaden these states, limiting their individual resolution to temperatures below 2 K and contributing to the deviation from ideal subthreshold behavior through non-thermionic transport. These results demonstrate the importance of atomistic modeling for predicting the cryogenic operation of nanowire FETs and guiding the design of future quantum-compatible devices.

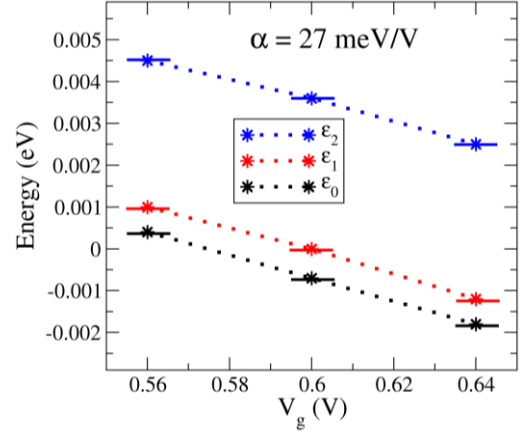


Fig. 10. Extraction of the gate lever-arm factor from the gate-voltage dependence of the first three localized energy levels.

REFERENCES

- [1] A. Razavih *et al.*, "Challenges and Limitations of CMOS Scaling for FinFET and Beyond Architectures," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 999-1004, 2019.
- [2] K.K. Likharev, "Single-Electron Devices and their Applications," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 606-632, 1999.
- [3] R. Lavieville *et al.*, "Quantum Dot Made in Metal Oxide Silicon Nanowire Field Effect Transistor Working at Room Temperature", *Nano Letters*, Vol. 15, pp. 2958-64 (2015).
- [4] P. Blaise *et al.*, "Nanoscale FET: How To Make Atomistic Simulation Versatile, Predictive, and Fast at 5nm Node and Below," *Proc. SISPAD*, Kobe, Japan, 2020, pp. 249-252.
- [5] S. Steiger *et al.*, "Nemo5: A Parallel Multiscale Nanoelectronics Modeling Tool", *IEEE Transactions on Nanotechnology*, vol. 10, pp. 1464-1474, 2011.
- [6] D.A. Lemus *et al.*, "Mode-Space-Compatible Inelastic Scattering in Atomistic Nonequilibrium Green's Function Implementations", *J. Computational Electronics*, vol. 19, pp. 1389-1398 (2020).
- [7] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS Transistor Model," *IEEE Transactions on Electron Devices*, vol. 65, no. 9, pp. 3617-3625, 2018.

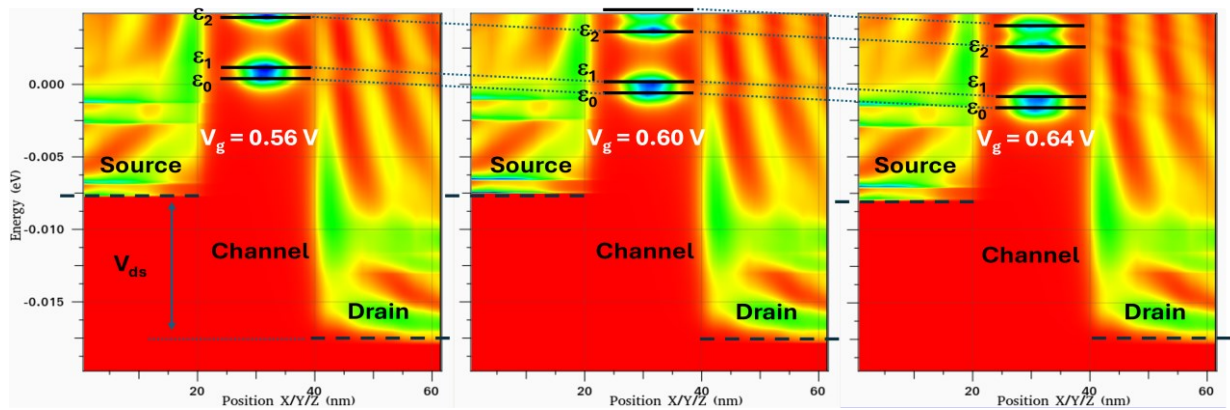


Fig. 9. Spatially and energetically resolved density of states along the transport direction. The source, channel, and drain regions are identified. The first three localized states in the channel are highlighted by thick black lines. Their linear energy shift with increasing gate voltage is emphasized by dotted guide lines drawn between successive bias points $V_g = 0.56\text{ V}$, 0.60 V , and 0.64 V .