

# Modeling of Soft Errors in CFET SRAM Using Machine Learning-Assisted Circuit Simulation

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**Abstract**—This study explores the use of machine learning methods in combination with the circuit-level simulator SPICE to analyze the effects of radiation on nanosheet-based CFET SRAMs. A regression model was developed to reproduce the radiation-induced threshold voltage drop of individual transistors by predicting body voltage pulses, and its accuracy in predicting SRAM bit-flip errors was evaluated through comparisons with TCAD simulation results. Although limitations still remain, the current model is able to capture the dependence of soft-error occurrence in CFET SRAMs on the direction and intensity of radiation.

**Index Terms**—SPICE, simulation, machine learning, CFET, SRAM.

## I. INTRODUCTION

From the past, radiation-induced soft errors has been known to cause reliability issues in ICs. This phenomenon may occur in the event of a radiation impact, which generates unintended carriers in the device and therefore leads to an imbalance of internal voltage. For example, radiation impacting SRAMs may cause data corruption called a single event upset (SEU) [1].

The soft error durability of a device depends on its structure. In the case of the recent 3-dimensional complementary FET (CFET) structure [2], several studies have shown that, depending on the transistor structure utilized (e.g., FinFET or nanosheet FET), a CFET device may experience transient responses of varying severity [3], [4]. Furthermore, in our previous study, we demonstrated that, due to the high density of transistors in CFET SRAM cells, multiple transistors may be hit at the same time by a single radiation track, resulting in complex circuit behavior [5]. This suggests that accurately predicting SRAM behavior requires accounting for the mutual interactions among multiple transistors. In addition, the error probability depends in a complex manner not only on the incident position, but also the direction of the radiation track. However, a comprehensive investigation of various conditions requires a large number of simulations, which is impractical using only a TCAD simulator.

This study focuses on the combination and the utilization of machine learning and the circuit-level simulator SPICE in simulating the effects of radiation strikes on a CFET SRAM cell. First, we propose a machine learning model to reproduce TCAD-generated data for radiation-induced transient currents in transistors within a SPICE environment. The model is then

applied to an SRAM cell, and its validity is evaluated by comparing the results with TCAD simulations. Finally, a large number of simulations are demonstrated using the model to investigate how the response of a CFET SRAM depends on the intensity and incident direction of the radiation.

## II. SIMULATION METHOD

A nanosheet-based CFET SRAM model was made according to the 3A rules [6] with the TCAD simulator Hy-DELEOS [7] (Fig. 1; top). Figure 1 also shows the circuit representation of the CFET SRAM, whose characteristics were reproduced using SPICE as demonstrated in Fig. 2.

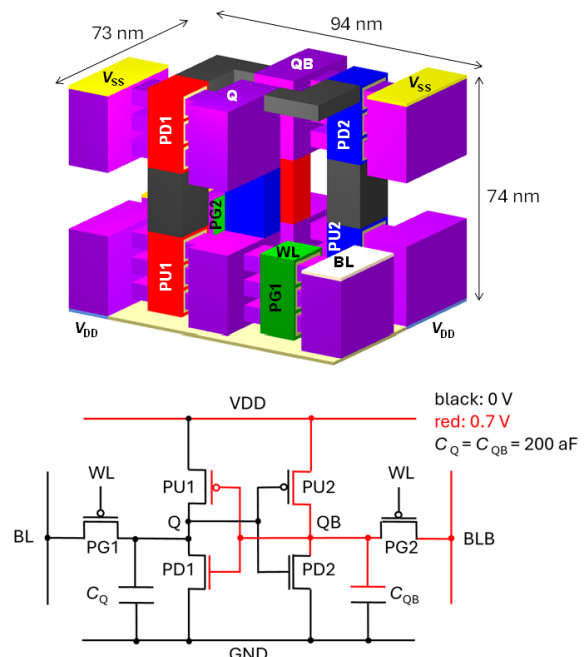


Fig. 1. (top) Dimensions of the CFET 6T-SRAM cell simulated in this study constructed in our previous work [5] based on the 3A rules [6]. (bottom) Circuit diagram of 6T-SRAM cell simulated using SPICE. Capacitances  $C_Q$  and  $C_{QB}$  are attached to nodes Q and QB, respectively, to reproduce TCAD results (see, Fig. 2). The wire colors indicate the initial bias conditions for the soft-error simulation.

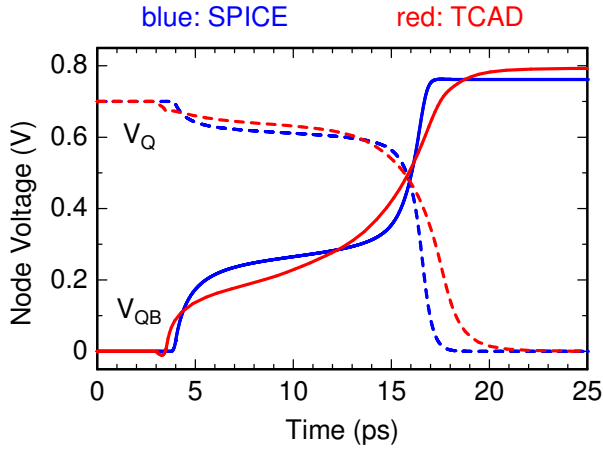


Fig. 2. Simulation results of the transient write characteristics of the SRAM. The values of  $C_Q$  and  $C_{QB}$  were adjusted via this simulation.

In our previous work [5], we identified the parasitic bipolar effect (PBE), induced by charge collection due to radiation incidence, as the primary cause of CFET SRAM bit upsets, and analyzed the essential mechanism using a simple and computationally efficient SPICE-based method [8] to reproduce this phenomenon. In that approach, a pulse voltage was applied to the substrate of the MOSFET circuit model to mimic the transient shift in  $V_{th}$  caused by PBE. However, the pulse waveform, which is characterized by the peak voltage  $V_{peak}$  and fall time  $t_{fall}$  had to be manually fitted for each set of radiation incidence conditions. Therefore, in this study, we aim to determine these parameters automatically using a machine learning approach as shown in Fig. 3.

We performed a large number of TCAD simulations on individual NMOS and PMOS transistors over a range of linear energy transfer (LET) values and particle-track positions and incident directions, thereby generating a dataset of transient drain current waveforms,  $I_D(t)$ , for various radiation incidence conditions. From this dataset, the two SPICE model parameters,  $V_{peak}$  and  $t_{fall}$ , required to reproduce each transient drain current waveform  $I_D(t)$ , were extracted. First,  $V_{peak}$  was determined so that the peak drain current in the SPICE simulation matched that obtained from TCAD. Then, with  $V_{peak}$  fixed,  $t_{fall}$  was optimized to minimize the root mean square error (RMSE) between the  $I_D(t)$  waveforms obtained from SPICE and TCAD.

Two regression models were then constructed to suggest the values of  $V_{peak}$  and  $t_{fall}$  that reproduce  $I_D(t)$ . Firstly,  $V_{peak}$  is estimated from the deposited charge  $Q_i$ , which can be straightforwardly obtained by integrating the generated e-h pairs within the  $i$ -th section of the transistor based on the incident track. We assumed a regression equation that follows

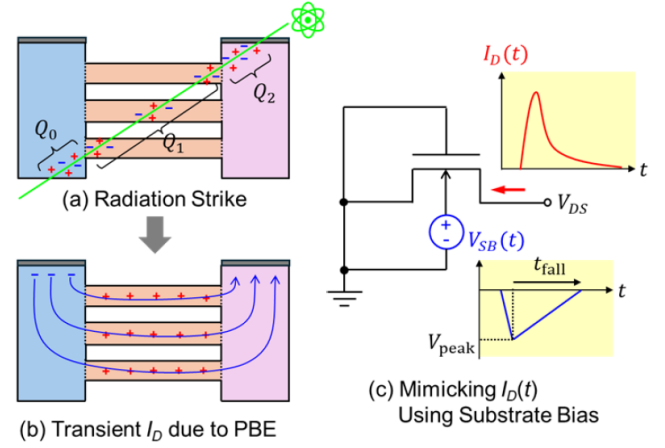


Fig. 3. Schematic illustration of the proposed model. An incident particle generates e-h pairs  $Q_{dep}$  along its track (a), and a portion of the holes is collected in the channel region, inducing the PBE (b). This effect is mimicked by applying a substrate bias to the MOSFET SPICE model, and the regression model infers the waveform of  $V_{SB}(t)$  from  $Q_{dep}$  which can be calculated from the radiation condition.

the power law:

$$V_{peak}(track) - V_0 = \left( \sum_{i=0}^{N-1} w_i Q_i(track) \right)^\alpha, \quad (1)$$

where  $V_0$  is the minimum  $V_{SB}$  to induce the threshold voltage shift, and  $w_i$  and  $\alpha$  are fitting parameters. We adopted an empirical model in which the weighted sum of the deposited charge in each section,  $\sum_i w_i Q_i$ , is raised to the power of  $\alpha$ . Then,  $t_{fall}$  was obtained from the following regression equation:

$$t_{fall}(V_{peak}) = a(V_{peak} - V_0)^\beta, \quad (2)$$

which was assumed based on the strong correlation between  $V_{peak}$  and  $t_{fall}$ . In this study, we divided a single transistor into  $N = 3$  sections, i.e., source, channel, and drain, with the intention of reflecting the effect that charge collection occurs more readily from the drain than from the source [9]. Regression was done using the Levenberg-Marquardt method [10] as shown in Fig. 4, and Fig. 5 plots  $I_D(t)$  predicted by SPICE using the fitted parameters (i.e.,  $V_{peak}$  and  $t_{fall}$ ) together with the corresponding TCAD results. From Fig. 5, it can be seen that, although some discrepancies remain, the proposed model successfully reproduces the overall characteristics of the transient drain current waveforms.

### III. SIMULATION RESULTS AND DISCUSSION

Figure 6 presents the verification results of the regression model; good agreement between the TCAD simulation results and the model predictions was observed after fine-tuning of the model parameters, with all cases yielding the same bit-flip/no-bit-flip outcome. However, there are discrepancies in terms of the timing and slope characteristics of the voltage

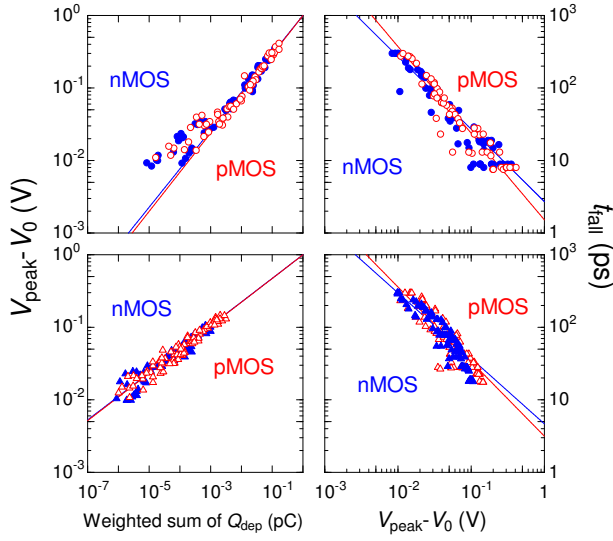


Fig. 4. Regression model fitting results for  $V_{\text{peak}}$  (left) and  $t_{\text{fall}}$  (right). Fitting was performed under two conditions, i.e.,  $|V_{DS}| = 0.7$  V (top) and  $|V_{DS}| = 0.05$  V (bottom), taking into account the bias condition of the SRAM in standby.

waveform. To understand the accuracy limitation of this model, further LET sweep simulations were performed for the track direction (d) as shown in Fig. 7. It can be seen that the bit-flip threshold in the TCAD simulation is higher than that of the SPICE regression model, with values of approximately  $0.025 \text{ pC}/\mu\text{m}$  and  $0.033 \text{ pC}/\mu\text{m}$ , respectively. This discrepancy is presumed to be mainly due to the lack of subthreshold conduction modeling in the transistor model used in this study

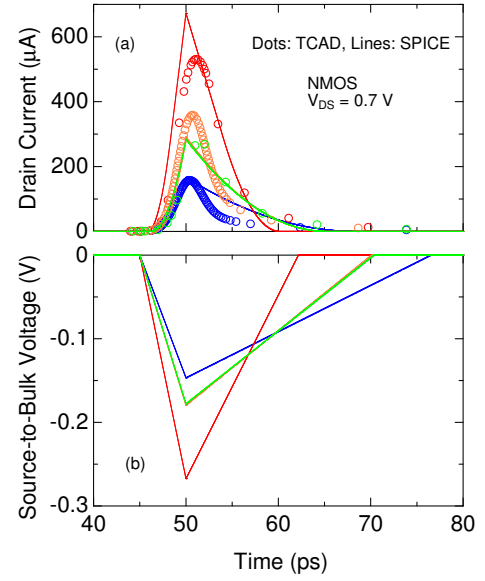


Fig. 5. Predicted waveforms of  $I_D(t)$  for an NMOS transistor biased at  $V_{DS} = 0.7$  V subjected to four randomly selected radiation tracks with various LETs, incident positions, and directions (a). Waveforms of  $V_{SB}(t)$  are shown in (b).

(i.e., Level 1).

Although several model limitations remain, we believe that the proposed approach can capture the radiation-condition dependence of bit-flip errors in CFET SRAM with significantly reduced computational cost. In fact, a single simulation requires less than one CPU second using SPICE, whereas TCAD simulations typically take several CPU days. This improvement allows many more simulation trials under various conditions to be executed, thereby enabling a more comprehensive understanding of the phenomenon.

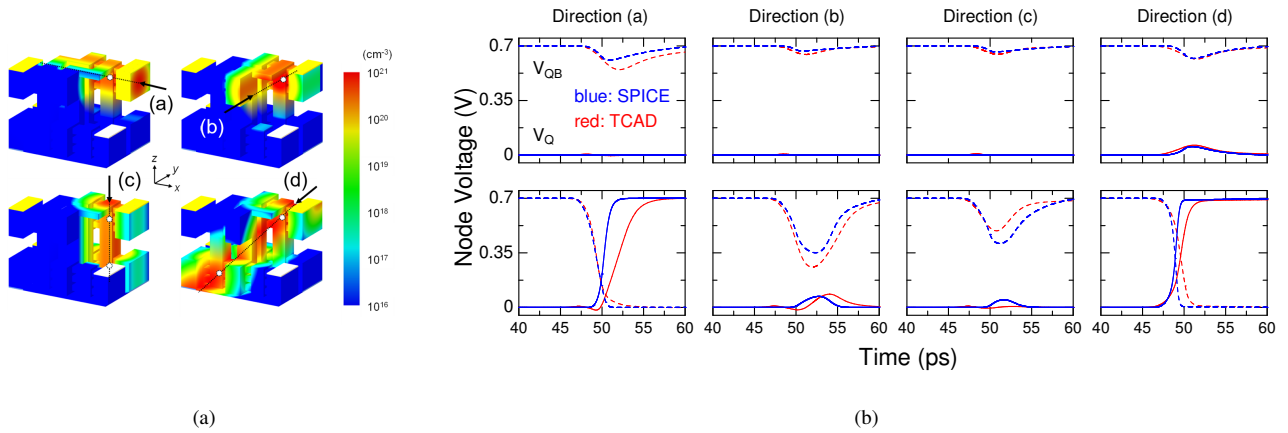


Fig. 6. Validation result of the proposed model. Radiation strikes generating e-h pairs at around  $t = 50$  ps, with two different LET values (top =  $0.0193 \text{ pC}/\mu\text{m}$ , bottom:  $0.096 \text{ pC}/\mu\text{m}$ ) and four incident directions (a) were considered. (b) The transient node voltage responses obtained from TCAD simulations (red) are compared with those predicted by the proposed model (blue).

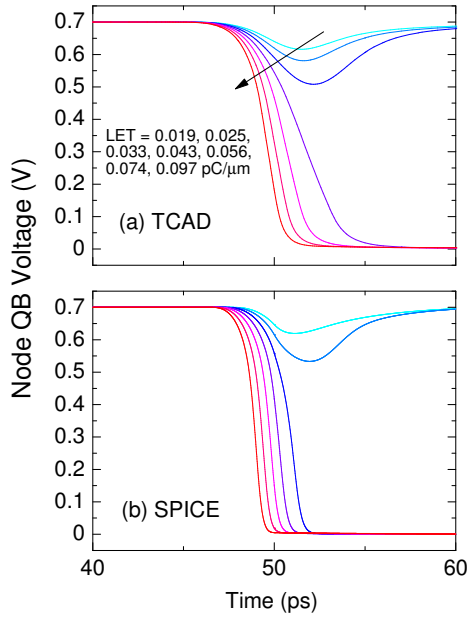


Fig. 7. Results of the LET sweep simulation for direction(d) simulated with TCAD (top) and SPICE (bottom). Only  $V_{QB}(t)$  is shown.

To showcase this point, the dependence of the threshold LET on the various incident direction is demonstrated at several locations in the CFET SRAM cell as shown in Fig. 8. Owing to the structural characteristics of CFETs, it is found that complex directional dependence arises due to multiple charge collection effects [5]. For target location (iii), which was also examined in Fig. 6, bit flips occur at relatively low LET values over a wide range of incident directions. This behavior is attributed to the PBE in transistor PD2, which turns the transistor on and discharges the charge stored at QB. However, when radiation is incident in the vertical direction, the PBE is also induced in transistor PU2, causing the effects of the two transistors to partially counteract each other and making a bit flip less likely (see Fig. 8 (c)).

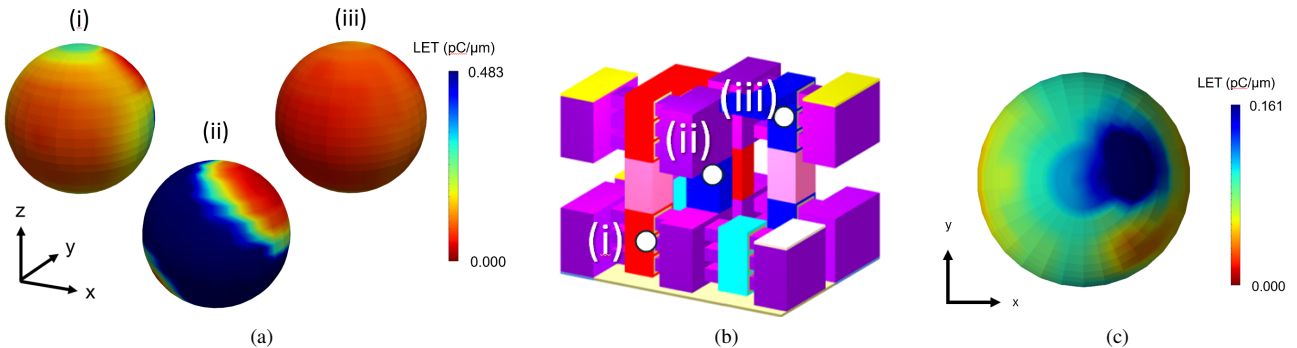


Fig. 8. (a) Minimum threshold LET required to induce a bit flip in the CFET SRAM cell, as predicted by the proposed model. The angular dependence of the threshold LET is shown on a spherical plot, where the red regions indicate the most sensitive directions for bit-flip occurrence. (b) Three target locations considered in this study: (i) the center of PU1, (ii) the center of the SRAM cell, and (iii) the center of PD2. (c) Top view of case (iii), where the LET range is reduced to one-third of that in (a) for clearer visualization of the variation.

#### IV. SUMMARY

A workflow utilizing circuit-level simulation and a machine learning based-regression model has been proposed to allow a massive number of simulations of soft errors in a nanosheet-based CFET SRAM cell, showing good agreement with computationally expensive TCAD simulations. Using the proposed model, the angular distribution of the threshold LET for radiation incident from various directions was visualized. This approach could provide a useful method for estimating the soft-error probability in CFET SRAM cells.

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