

Impact of Thermal Expansion Mismatch-Induced NMOS Metal Gate Stress on MBCFET Performance

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Abstract—This paper presents a systematic investigation of thermomechanical stress induced in Si nanosheet channels by the thermal expansion mismatch of metal gates during high-temperature deposition in Multi-Bridge Channel Field Effect Transistors (MBCFETs). Using quantum corrected drift-diffusion device simulation, we analyze the three-dimensional stress distributions in the Si channel as functions of gate metal thickness, coefficient of thermal expansion (CTE), and nanosheet width (wNS). The results demonstrate that increasing gate metal CTE from $2 \times 10^{-6}/\text{K}$ to $23 \times 10^{-6}/\text{K}$ raises channel resistance (ΔR_{ch}) by approximately 3.8%. Under fully-filled gate conditions, significant edge stress concentration is observed in StressXX (S_{xx}), while StressZZ (S_{zz}) exhibits a saturation behavior. Furthermore, reducing nanosheet width from 100 nm to 20 nm amplifies the tensile StressYY (S_{yy}) by twice higher, leading to additional linear drive current improvement (ΔI_{odlin}) of up to +1.5%. These findings provide critical design guidelines for gate stack optimization and stress-aware engineering in scaled MBCFET technology nodes.

Keywords—MBCFET, Residual Stress, Coefficient of Thermal Expansion (CTE), TCAD

I. INTRODUCTION

As semiconductor devices continue to scale down, the Multi-Bridge Channel Field Effect Transistor (MBCFET) has emerged as a promising successor to conventional FinFET architectures, offering superior electrostatic control and enhanced scalability to meet increasingly demanding target specifications [1-3]. The multi-stacked horizontal nanosheet configuration of the MBCFET enables precise modulation of the effective channel width while suppressing short-channel effects, making it one of the most viable device platforms for sub-3 nm technology nodes [4,5].

A distinctive structural feature of the MBCFET is that each Si nanosheet channel is fully surrounded by the gate metal in a gate-all-around (GAA) configuration. This enclosure introduces a unique and non-trivial mechanical coupling between the gate metal and the Si channel region that has no direct analog in planar or FinFET structures. During high-temperature gate stack deposition, the metal gate undergoes thermal expansion and conformally envelops the nanosheet. Upon cooling to room temperature, the coefficient of thermal expansion (CTE) mismatch between the gate metal candidates and surrounding materials such as nitride, high-k material, Si generates residual mechanical stress in the channel [6,7]. Depending on the specific gate metal material and its CTE relative to Si (CTE of Si approximately $3 \times 10^{-6}/\text{K}$), non-negligible compressive or tensile stress components can be induced along all three spatial directions, potentially affecting key

device parameters such as channel resistance (R_{ch}) and linear over drive current (I_{odlin}) [8].

The impact of this gate metal-induced stress is expected to become increasingly significant as device geometry continues to scale. In particular, as the nanosheet width (wNS) decreases, the mechanical boundary conditions imposed by the surrounding gate metal become geometrically more dominant, amplifying the transverse stress component in the Si channel. This geometry-dependent stress behavior can give rise to local layout effects (LLE), which are performance variations that depend on the specific nanosheet width and gate fill condition in a given layout, and which are difficult to predict or control without a systematic understanding of the underlying stress mechanisms [9,10]. Despite the critical importance of these effects, comprehensive studies that simultaneously address uniaxial stress sensitivity, gate metal property dependence, and nanosheet geometry effects in MBCFETs remain limited in the literature, with prior work focusing primarily on intentional strain engineering rather than fabrication-induced thermomechanical stress [11-13].

In this work, quantum-corrected drift-diffusion(DD) transport simulations are employed to systematically analyze the impact of gate metal stress on the Si channel in NMOS MBCFETs. The effects of uniaxial and isotropic stress conditions, gate metal thickness, CTE, and nanosheet width on key device parameters are investigated in detail. The results provide mechanistic insight into the stress transfer pathway from the gate metal to the Si channel and offer quantitative design guidelines for stress-aware gate stack engineering in scaled MBCFET devices.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

Fig. 1(a) shows the simulated three-dimensional MBCFET structure, consisting of three vertically stacked Si nanosheet channels in a GAA configuration with source/drain (S/D) epitaxial regions at both ends. The x-cut cross-section [Fig. 1(b)] illustrates the gate stack wrapping conformally around each nanosheet along the channel length direction, and the y-cut cross-section [Fig. 1(c)] shows the lateral enclosure of the nanosheet by the metal gate and high-k dielectric in the width direction. The inter-sheet spacing is 8 nm and the inner spacer material is SiO_2 . The key structural parameters are summarized in Table I.

The gate stack comprises a HfO_2 high-k dielectric with an equivalent oxide thickness (EOT) of 1 nm and a metal gate layer. The metal gate thickness (T_{Metal}) is varied between 2 nm and 5 nm to examine both not-fully-filled and fully-filled conditions in the inter-sheet space. The wNS is varied from 20 nm to 100 nm to investigate width-

dependent stress behavior. N-type channel doping is assumed throughout, with S/D regions formed by Si:P epitaxy.

The piezo resistivity model was employed to capture stress-induced carrier mobility modifications, where the mobility change tensor is related to the stress tensor via the piezoresistive coefficients of Si. DD simulations incorporating stress-modified mobility were then performed to extract electrical characteristics including I_D - V_G curves, R_{ch} , and I_{on} at $V_{DS} = 50$ mV and $V_{GS} = V_{DD} + 0.4$ V. To isolate the directional sensitivity of the Si channel, uniaxial mechanical stress boundary conditions were independently applied to the gate metal along the X (channel transport), Y (width), and Z (vertical) directions as depicted in Fig. 1. The resulting stress components in the Si channel and corresponding ΔR_{ch} were extracted to map the directional stress sensitivity. For parametric studies, the gate metal CTE was varied from $2 \times 10^{-6}/K$ to $23 \times 10^{-6}/K$ [14,15], and T_{Metal} was varied between 2 nm and 5 nm.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows ΔR_{ch} of the Si nanosheet channel when uniaxial stress is independently applied along the X, Y, and Z directions. The channel resistance is most sensitive to S_{XX} , exhibiting a ΔR_{ch} of +6.8% per GPa of applied stress. This is attributed to the direct suppression of longitudinal electron mobility via the piezoresistive effect along the [100] transport direction. S_{YY} produces a moderate ΔR_{ch} response of +3.1% per GPa, while S_{ZZ} shows the weakest coupling at +1.4% per GPa. Figs. 2(b)-(e) show the resulting S_{XX} , S_{YY} , and S_{ZZ} components induced in the Si channel when uniaxial stress is applied to the gate metal along the X, Y, Z, and combined directions, respectively. A key observation is that even when stress is applied to the gate metal along a single direction, stress components are induced in the Si channel along all three axes. This multi-directional stress coupling arises from Poisson effects and the mechanical constraints imposed by the fully enclosing GAA geometry. The gate-all-around structure forces the nanosheet to respond to metal deformation in all spatial directions simultaneously, which is a defining mechanical characteristic of the MBCFET that fundamentally distinguishes it from FinFET or planar devices.

Figs. 3(a)-(c) show S_{XX} , S_{YY} , and S_{ZZ} in the Si channel as a function of gate metal thickness. As T_{Metal} increases from 0.5 nm to 6 nm, all three stress components increase due to the greater mechanical constraint exerted by the thicker metal layer during thermal contraction. The larger sensitivity of S_{XX} and S_{YY} relative to S_{ZZ} is consistent with the more effective stress transmission through the lateral and longitudinal gate walls in the GAA geometry, where the nanosheet perimeter is fully enclosed by the gate metal. Figs. 3(d)-(f) show the CTE dependence of S_{XX} , S_{YY} , and S_{ZZ} at $T_{Metal} = 5$ nm. As the gate metal CTE increases from $2 \times 10^{-6}/K$ to $23 \times 10^{-6}/K$, the thermal mismatch with Si grows proportionally, leading to a monotonic increase in all three stress components. These results indicate that the choice of gate metal material, through its CTE value, is the primary process lever controlling the magnitude of stress imposed on the Si channel.

Fig. 3(a)-(c) show S_{XX} , S_{YY} , and S_{ZZ} in the Si channel as a function of gate metal thickness, revealing distinct behaviors for each stress component as the inter-sheet space

transitions from a not-fully filled to a fully-filled condition. S_{XX} increases gradually and continuously with increasing gate metal thickness throughout the entire range. In contrast, S_{YY} exhibits a sharp increase once the fully-filled condition is reached, driven by the additional lateral confinement imposed when the metal gate completely occupies the inter-sheet space. S_{ZZ} , on the other hand, saturates beyond the fully-filled state, as the vertical stress equilibrium is established once complete top and bottom gate contact with the nanosheet is achieved, and additional metal volume no longer introduces further vertical constraint.

Fig. 4 shows S_{XX} contour plots along the nanosheet width direction for the fully-filled ($T_{Metal} = 5$ nm) and not-fully-filled ($T_{Metal} = 2$ nm) gate conditions, extracted at the inner nanosheet layer. In the fully-filled condition, ΔS_{XX} reaches -0.76 GPa, approximately 55% higher than the center value of -0.49 GPa. This edge stress amplification is a direct structural consequence of the MBCFET GAA geometry: at the nanosheet corners, stress contributions from the top, bottom, and sidewall gate regions superimpose, creating a localized stress concentration that is absent in the center of the channel. In the not-fully-filled condition, the edge stress concentration is substantially reduced. S_{XX} remains within -0.72 to -0.81 GPa across the nanosheet width, indicating a considerably more uniform stress distribution. This contrast highlights that the gate metal fill condition in the inter-sheet space is a critical determinant of lateral stress non-uniformity within the nanosheet, and must be carefully controlled in process integration to avoid localized performance degradation.

Fig. 5(a) shows ΔR_{ch} as a function of T_{Metal} for a fixed CTE of $23 \times 10^{-6}/K$. As T_{Metal} increases from 0.5 nm to 2.5 nm, which is not-fully-filled regime, ΔR_{ch} increases gradually due to the combined effect of growing compressive S_{XX} , which directly degrades longitudinal electron mobility, and the weak tensile S_{ZZ} contribution. Once the T_{Metal} exceeds the fully-filled condition, however, ΔR_{ch} recovers toward its initial value. This recovery is attributed to the sharply increased tensile S_{YY} that arises under the fully-filled state, which partially compensates the mobility degradation induced by compressive S_{XX} , resulting in a net reduction of ΔR_{ch} beyond the fully-filled threshold. When the gate metal material with a large CTE value is used without achieving the fully-filled condition, the beneficial mobility gain associated with the sharp increase in tensile S_{YY} cannot be realized, since this S_{YY} enhancement is a consequence of the fully-filled geometry. As a result, only the detrimental compressive S_{XX} contribution remains active, and ΔR_{ch} degradation of up to +4.5% can be induced as shown in Fig. 5 (b).

Fig. 6(a) shows the width dependence of S_{XX} , S_{YY} , and S_{ZZ} as wNS scales from 100 nm to 20 nm. While S_{XX} and S_{ZZ} show increase of +19.8% in compressive stress and decrease of -23.6% in tensile stress, respectively, S_{YY} exhibits a markedly stronger width dependence, increasing by a factor of 2 from -0.13 GPa at wNS = 100 nm to -0.26 GPa at wNS = 20 nm. This strong amplification of S_{YY} with decreasing nanosheet width is attributed to the increasing dominance of the gate metal sidewalls as the nanosheet narrows. When wNS is large, the lateral gate walls impose stress over a relatively small fraction of the nanosheet volume, and the stress state is primarily governed by the top

and bottom gate contacts. As w_{NS} decreases, however, the sidewall-to-volume ratio increases substantially, and the lateral confinement by the gate metal becomes the dominant mechanical boundary condition, driving a sharp increase in the transverse stress component as shown in Fig. 6(b).

Fig. 6(c) shows ΔI_{odlin} , which is the difference between with and without gate metal-induced stress at each w_{NS} , as a function of $1/w_{NS}$, and the observed trend originates directly from the S_{YY} differences identified in Fig. 6(a). At $w_{NS} = 100$ nm, the relatively small S_{YY} results in a ΔI_{odlin} degradation of -0.77% . As w_{NS} decreases, however, S_{YY} increases substantially, and its tensile contribution to carrier mobility becomes increasingly dominant, leading to a progressive improvement in ΔI_{odlin} that reaches $+1.5\%$ at the narrow nanosheet width investigated. This reversal from degradation to improvement with decreasing w_{NS} demonstrates that the stress state in the Si channel is strongly geometry-dependent. Furthermore, this width-dependent behavior of ΔI_{odlin} has direct implications for local layout effects (LLE), as devices with different nanosheet widths within the same layout will experience different levels of gate metal-induced stress and consequently exhibit non-uniform performance characteristics even under nominally identical process conditions.

IV. CONCLUSION

In this work, we have systematically investigated the thermomechanical stress induced by gate metal CTE mismatch in Si nanosheet channels of MBCFETs using DD transport simulation. The Si channel exhibits the highest resistance sensitivity to longitudinal stress (S_{xx}), while the GAA geometry enables multi-directional stress transmission from the gate metal to the channel through Poisson coupling. Both gate metal thickness and CTE are shown to be critical process parameters: increasing CTE from $2 \times 10^{-6}/K$ to $23 \times 10^{-6}/K$ results in a ΔR_{ch} increase of approximately 3.8% , while thicker gate metal further amplifies all three stress components. Under fully-filled gate conditions, S_{xx} is significantly concentrated at the nanosheet edges as a structural consequence of the GAA geometry, while S_{zz} saturates with increasing gate fill level. As nanosheet width scales from 100 nm to 20 nm, S_{YY} increases by 2-times higher, driving ΔI_{odlin} improvement from -0.77% to $+1.5\%$ and giving rise to a geometry-dependent local layout effect. These findings provide quantitative guidelines for gate metal selection, thermal budget control, and nanosheet width design in scaled MBCFET technology nodes.

V. RECERENCES

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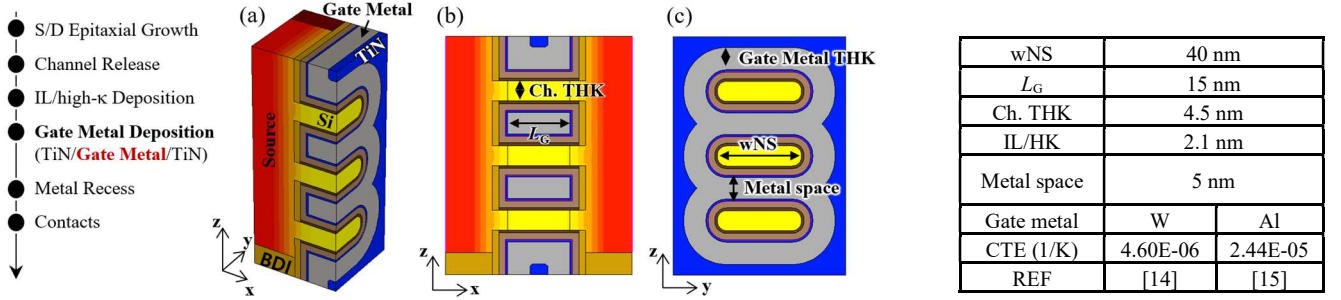


Fig. 1 MBCFET Process flow and (a) 3D structure, (b) y-cut, and (c) x-cut cross-sectional view.

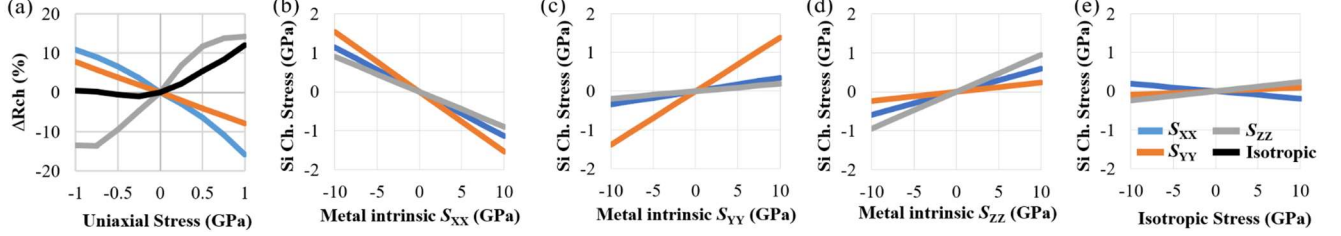


Fig. 2 (a) ΔR_{ch} as a function of uniaxial stress applied to the Si channel beneath the gate. The reference is defined as the unstressed Si channel condition. StressXX (S_{XX}), StressYY (S_{YY}), and StressZZ (S_{ZZ}) induced in the Si channel when uniaxial stress is applied the gate metal in the (b) x-, (c) y-, and (d) z-direction respectively, and (e) under isotropic stress condition. Due to the film stress effect, the stress applied to the gate metal induces an opposite-directional stress in the Si channel along the same direction, while the stresses in the other two directions exhibit the same kind of stress as the applied stress

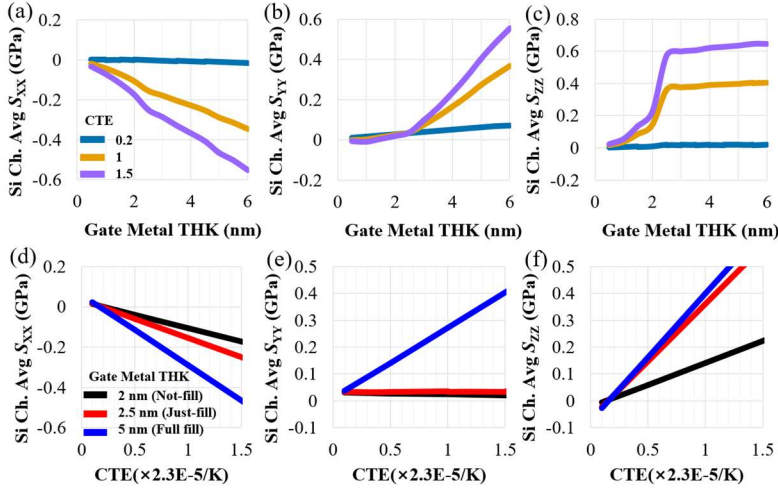


Fig. 3 Stress induced in the Si channel as a function of gate metal thickness and coefficient of thermal expansion (CTE), where $CTE(\times 2.3E-5/K) = 0.2$ corresponds to W and $CTE = 1.2$ corresponds to Al. Note that gate metal thickness of 3nm and above represents a fully filled structure.

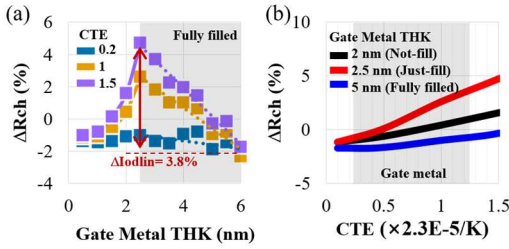


Fig. 5 ΔR_{ch} as a function of gate metal thickness and CTE. In the fully filled structure, a material with larger CTE induces greater S_{XX} , which can degrade Rch. However, as the gate metal thickness further increases, the larger S_{YY} tends to compensate for this degradation.

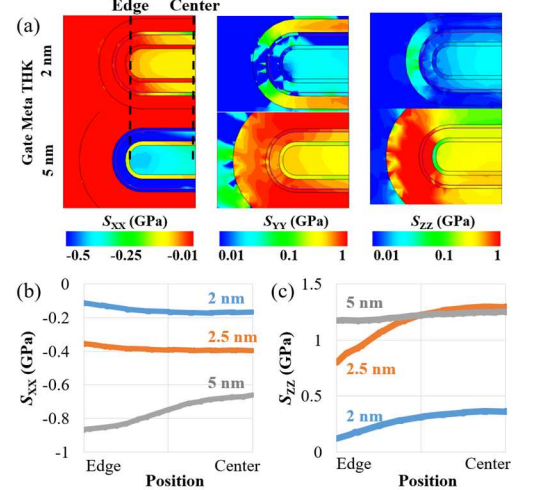


Fig. 4 (a) Width-direction contour plots of the gate metal stress for thicknesses of 2 and 5 nm. (b), (c) S_{XX} , S_{ZZ} profile extracted along the channel-direction from the contour plot in (a), confirming the increase of S_{XX} , S_{ZZ} at the edge region.

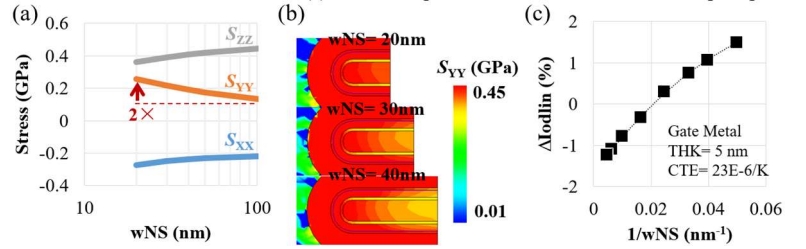


Fig. 6 (a) S_{XX} , S_{YY} , and S_{ZZ} as a function of channel width. (b) S_{YY} contour plots for wNS = 20, 30, and 40 nm, showing that S_{YY} increases as wNS decreases due to the increasing edge effects. (c) Iodlin ratio as a function of $1/wNS$ with and without stress, demonstrating that for wNS < 50 nm, the increasing edge effects lead to a measurable Iodlin gain. (Iodlin = $I_{ds} @ V_{gs} = V_{th} + 0.4$ V, $V_{ds} = 0.05$ V)