

Multiscale Modeling of Channel Surface Roughness: Impact on Front-End-of-Line And Circuit Performance for Advanced Logic Technology

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Abstract—Channel surface roughness is a critical process-induced performance limiter and variability source for the nanosheet-based Gate-All-Around technology. In this work, we evaluate the device and circuit-level performance impact of integrating low silicon surface roughness process for the advanced GAA technology by deploying our calibrated MSCO™ modeling platform. Our analysis demonstrates a 2% circuit-level performance improvement under iso-power conditions and a 4% circuit-level power reduction at iso-performance, attributable to enhanced front-end-of-line (FEOL) transistor drive strength resulting from improved silicon surface roughness.

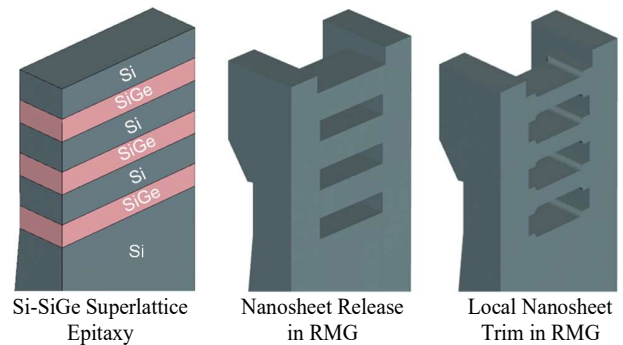
Keywords—Surface Roughness, Gate-All-Around, Field Effect Transistor, Carrier Mobility, Channel Surface Roughness, DTCO, TCAD

I. INTRODUCTION

As CMOS technology continues to scale, the industry has transitioned from FinFETs to GAA transistors to overcome fundamental limitations in fin scaling and device electrostatics [1][2][3][4]. In FinFETs, continued gate length scaling requires narrower and taller fins to maintain sufficient channel width and drive current; however, aggressively narrowing fin widths and increasing fin height are constrained by mechanical stability, process complexity, and fin patterning limits, introducing the problem of high silicon channel surface roughness which degrades electrostatic control and carrier mobility of the FinFET channel. GAA architectures address these challenges by replacing fins with stacked nanosheets that are fully surrounded by the gate, enabling superior electrostatic control independent of lateral scaling. This geometry brings channel thickness scaling feasibility to be precisely tuned to balance performance and leakage, while stacked channels recover drive current without relying on extreme fin height. However, GAA transistors also see the impact of surface roughness as in FinFET [5][6][7]. The channel surface roughness in GAA mainly stems from Germanium inter-diffusion during the Silicon-SiGe superlattice epitaxy and the thermal budget seen by the stack in subsequent steps, followed by etch selectivity limitations during selective nanosheet release and local nanosheet trim process steps prior to HKMG deposition as shown in Fig 1(a). Therefore, while the superlattice epitaxy process in GAA is

Sources of Channel Surface Roughness & First Principles Modeling of Impact on Mobility

(a) Key Process Steps Contributing to Channel Surface Roughness



(b) First Principles Modeling of Mobility Impact

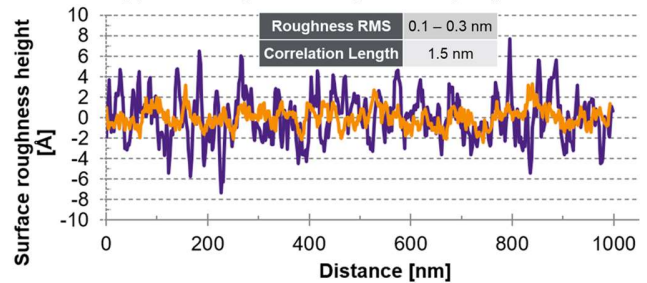


Fig. 1. (a) Device structures and cross-sectional view of nanosheet channel of nMOS and pMOS GAA transistors at the 1.4 nm technology node during key process steps contributing to channel surface roughness. (b) The surface roughness metrics shows the surface roughness height extracted (Purple: Roughness RMS = 0.3 nm; Yellow: Roughness RMS = 0.1 nm) for first principles modeling of mobility impact.

expected to lead to lower nanosheet thickness/width variability compared to FinFET fin width variability owing to SAQP and etch processes [8][9], channel surface roughness can pose as a unique variability source and performance detractor for GAA architecture. In this work, we capture channel surface roughness effects on carrier mobility at the 1.4 nm technology node using first-principles modeling and project the impact on the FEOL and circuit-level performance through our Materials-to-Systems Co-Optimization (MSCO™) [10] platform.

II. MODELING FRAMEWORK

An advanced carrier mobility calibration framework, based on first principles band structure calculations and drift-diffusion

Framework to Project PPA Impact of Channel Surface Roughness

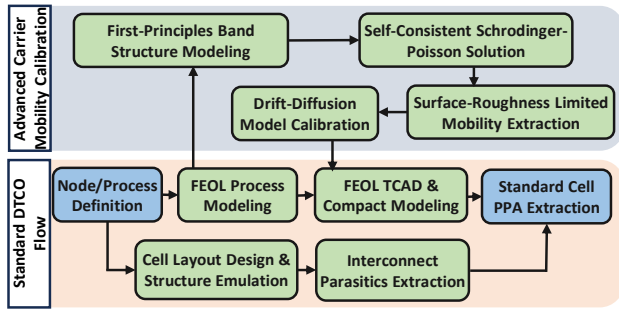


Fig. 2. Modeling Framework to project PPA for surface roughness improvement.

1.4 nm Gate-All-Around (GAA) Structures & Dimensions

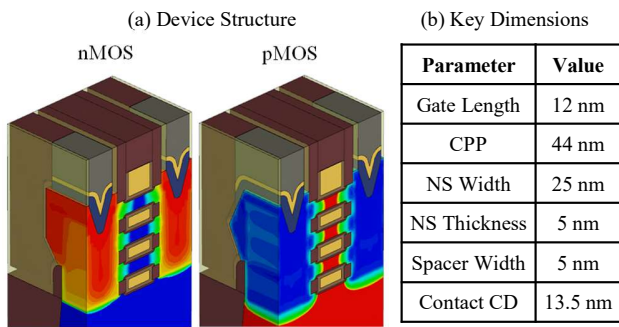


Fig. 3. (a) Device structures and cross-sectional view of nanosheet channel of nMOS and pMOS GAA transistors at the 1.4 nm technology node along with (b) key device dimensions.

transport modeling, is incorporated into our standard DTCO flow to assess the impact of surface roughness on carrier mobility, FEOL performance and circuit level PPA, as detailed in Fig. 2. The 3-nanosheet stack GAA transistors with the dimensions projected for the 1.4 nm technology node (Fig. 3) are used in this study [1][11]. The channel surface roughness profile is modeled using an exponential autocorrelation function with RMS values in the range typically reported [5][6][7]. TCAD Drift-diffusion transport models are closely calibrated to self-consistent Schrödinger-Poisson and sub-band Boltzmann transport equation solutions for channel surface roughness patterns ranging from 0.5 nm down to 0.1 nm RMS, keeping the correlation length fixed, and for different gate bias conditions. Henceforth, the calibrated TCAD setup is used to assess FEOL performance impact and extract compact models for different surface roughness scenarios to project the impact at the circuit-level PPA in presence of Middle-of-Line (MOL) and Back-end-of-Line (BEOL) interconnect parasitics.

III. RESULTS AND DISCUSSION

Figure 4 shows the calibration of the electron and hole mobilities between TCAD and to first-principles modeling for different RMS values of surface roughness. RMS values of 0.3 nm are used as the benchmark for this analysis [5][6][12]. The carrier mobility increases by 40% for electrons and 20% for holes at nominal 0.7 V gate bias by reducing RMS surface roughness from 0.3 nm to 0.1 nm. The FEOL On-resistance (R-

First Principles to TCAD Calibration

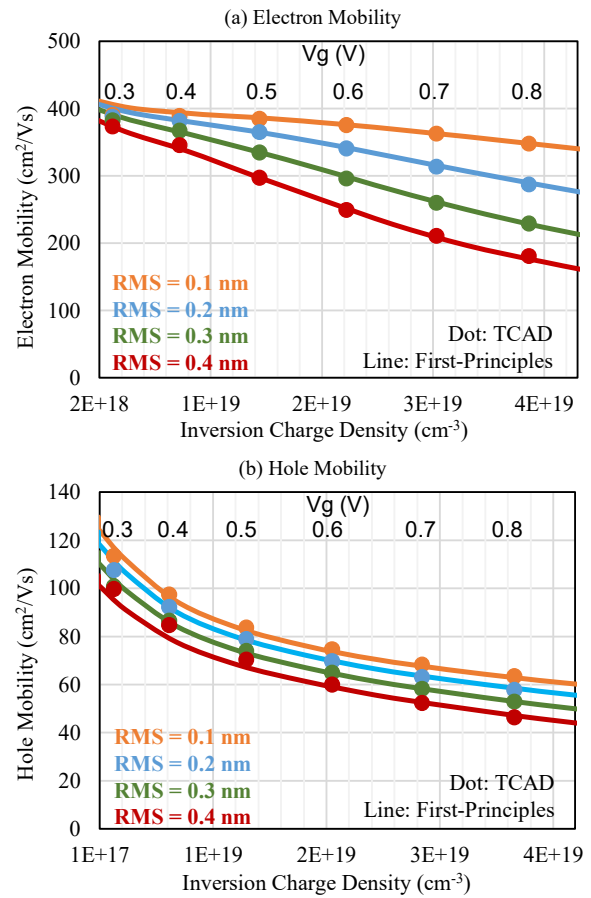


Fig. 4. The calibration of TCAD (a) electron and (b) hole mobility to the carrier mobility extracted from the first-principles modeling for different RMS surface roughness ranging from 0.1 nm to 0.4 nm. The mobility obtained from TCAD is matched to first-principles modeling through calibration of mobility versus channel inversion charge density at each gate bias ranging from 0.3 V to 0.8 V.

FEOL nMOS R-On & I-On Projection

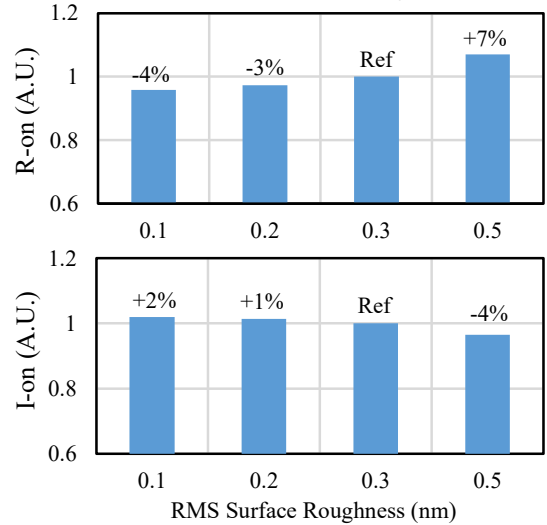


Fig. 5. FEOL nMOS R-on projection shows 4% R-on improvement and 2% I-on improvement by reducing RMS surface roughness from 0.3 nm to 0.1 nm for 1.4 nm nMOS devices.

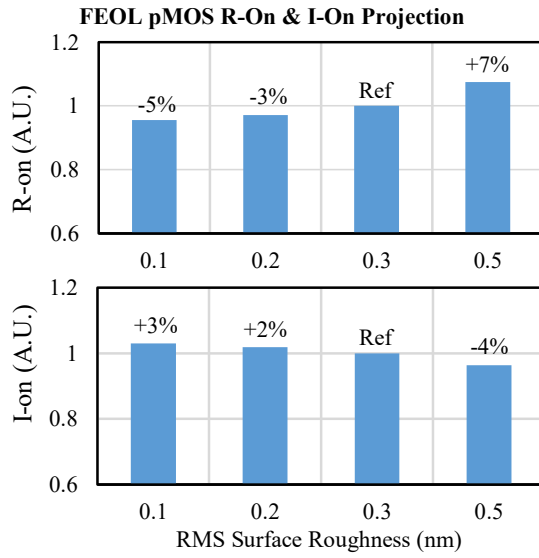


Fig. 6. FEOL pMOS R-on projection shows 5% R-on improvement and 3% I-on improvement by reducing RMS surface roughness from 0.3 nm to 0.1 nm for 1.4 nm pMOS devices.

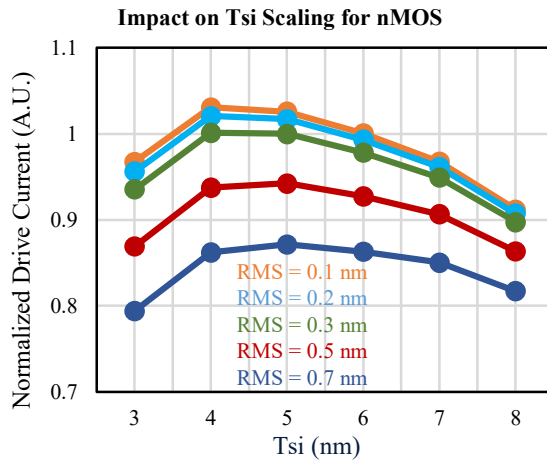


Fig. 7. Impact of silicon nanosheet thickness (Tsi) scaling for the drive current of nMOS indicates drive current loss for Tsi below 5 nm along with higher surface roughness impact.

Inverter Ring-Oscillator PPA Projection

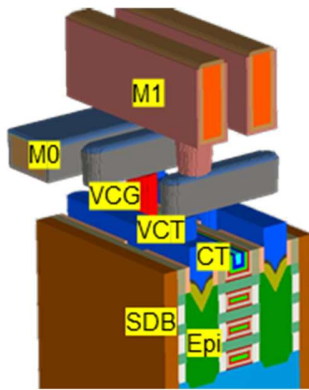


Fig. 8. Inverter-based Ring-Oscillator (RO) PPA projection.

On) in Fig. 5 and Fig. 6 improves by 4% and 5% for nMOS and pMOS, respectively, driven by mobility improvement as surface roughness is scaled from 0.3nm to 0.1nm RMS. The different sensitivity of nMOS and pMOS R-On to surface roughness arises due to differences in contribution of the corresponding channel resistance, the component of R-On directly affected by roughness-induced scattering. Correspondingly, the nMOS and

Inverter Ring-Oscillator PPA vs Channel Surface Roughness

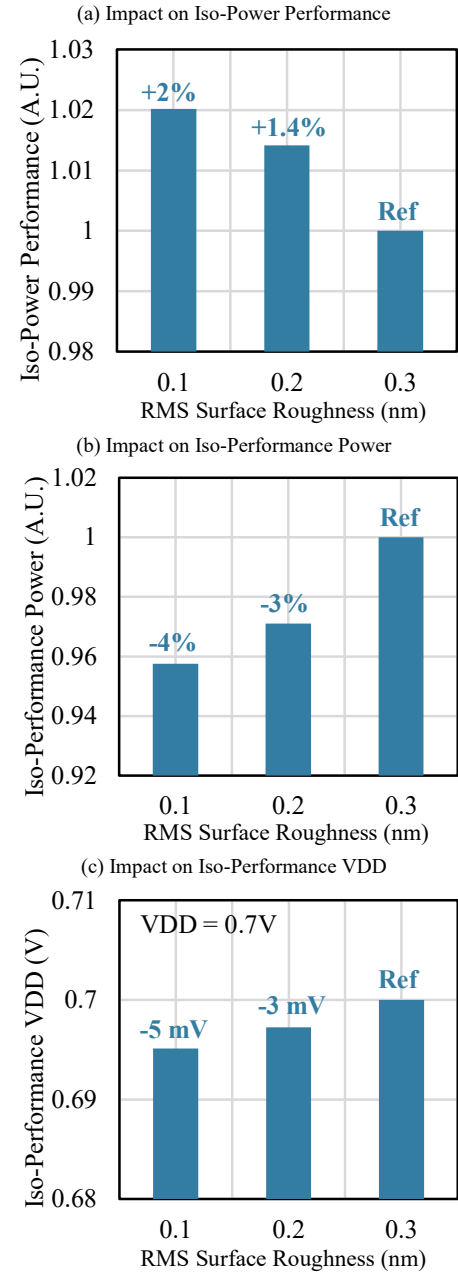


Fig. 9. Projected Inverter-based Ring-Oscillator performance impact of RMS surface roughness. (a) Impact on iso-power performance shows 2% performance improvement at the same circuit-level power w/ RMS surface improved from 0.3 nm to 0.1 nm. (b) Impact on iso-performance power shows 4% power improvement at the same circuit performance w/ RMS surface improved from 0.3 nm to 0.1 nm. (c) Impact on iso-performance VDD shows 5 mV VDD voltage reduction at the same circuit performance w/ RMS surface improved from 0.3 to 0.1 nm.

pMOS FEOL drive-strength (I-On at fixed off-current) undergo 2% and 3% improvements, respectively.

Additionally, we investigate the significance of reducing channel surface roughness in the context of nanosheet width scaling. Figure 7 shows that nanosheets thinner than 5 nm experience greater drive-current loss, coinciding with an increased sensitivity to surface roughness that scaling nanosheet thickness beyond 5 nm leads to diminishing returns in I-On improvement owing to the increase in inversion charge density being offset by constriction of the conduction path. Higher drive-strength loss due to surface roughness scattering is also seen as nanosheet thickness is scaled. The results demonstrate that without meaningful improvements to surface roughness, further nanosheet width scaling leads to diminishing performance returns, making channel surface roughness reduction a critical enabler for extending nanosheet architectures to more aggressive dimensions.

For more extensive benchmarking analysis of surface roughness impact, the combined impact on performance and power is investigated for both the inverter and more complex AOI-based ring-oscillator (RO) circuits, plotted in Fig. 9. The RMS surface roughness improvement results in ~1% performance enhancement at constant power consumption for every 1 Å reduction in roughness RMS, primarily attributed to the improved carrier mobility and reduced FEOL R-On. For power-critical applications, reducing roughness RMS can lead to up to 4% power reduction and allow VDD scaling by up to 5 mV without compromising performance.

IV. SUMMARY

In conclusion, our results show that lowering silicon surface roughness is an effective strategy for reducing GAA channel resistance and boosting FEOL as well as circuit performance and power consumption. A reduction in roughness from 0.3 nm to 0.1 nm achieves up to a 2% increase in transistor-level drive strength, along with 2% higher performance and 4% lower power at the ring-oscillator level. These findings demonstrate that the process flow updates to lower channel surface roughness are critical for power-efficient performance scaling in advanced GAA technology nodes. Our results also demonstrate that improving channel surface roughness is essential for enabling continued nanosheet width scaling to more aggressive dimensions.

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