

Impact of 4F² DRAM Access Transistor Design on Floating Body Effect and Retention

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Abstract—Future DRAM nodes will deploy an access transistor with a floating body, susceptible to transient hole storage and accompanying retention degradation. In this work, we present a framework for evaluating 4F² DRAM access transistor floating body effect (FBE) sensitivity to design and operating parameters, and quantify the performance impact of bit-cell with ‘d1’ state. Among the investigated scenarios, bit-cells with higher source/drain junction overlap show the strongest effect on FBE hole storage and dynamic retention loss. We observe that, for FBE ΔV_T greater than ~250 mV, an FBE dependence on bit-line voltage bias leads to degraded dynamic retention, rather than an increased absolute amount of FBE ΔV_T .

Keywords—4F² DRAM, Floating Body Effect, DRAM, Field Effect Transistor, Memory, DTCO, TCAD

I. INTRODUCTION

To continue DRAM advancement beyond 6F², new 4F² and 3D DRAM architectures have been proposed, which necessitate for the first time the deployment of a multi-gate access transistor [1]. Fig. 1 pictorially contrasts the 6F² and 4F² DRAM access transistors. In the 4F² architecture, the Vertical Channel Transistor (VCT) is elevated above the substrate, with the body sandwiched (“floating”) in between the Bit-Line (BL) and Storage Node (SN), in contrast to the 6F² saddle channel structure, in which the body is connected to the substrate contact. Fig. 2a plots hole storage over time for various access transistors in the hold state. In the 6F² architecture, generated holes flow into the substrate before they can accumulate and cause a

6F² DRAM Saddle Transistor Versus 4F² DRAM Vertical Channel Transistor

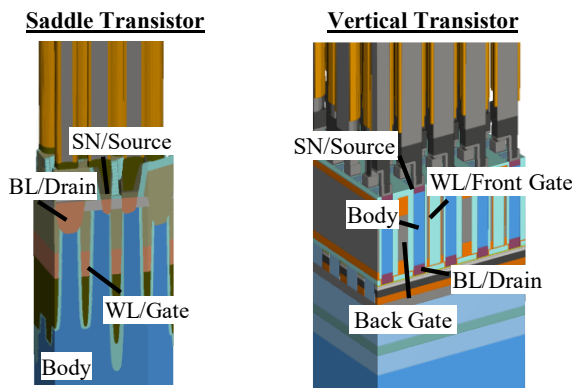


Fig. 1. 4F² DRAM Vertical Channel Transistor (VCT) enables pitch scaling and cell footprint to shrink from 6F² to 4F², but introduces a “floating” body which is not directly electrically connected to the substrate.

Floating Body Effect Hole Storage

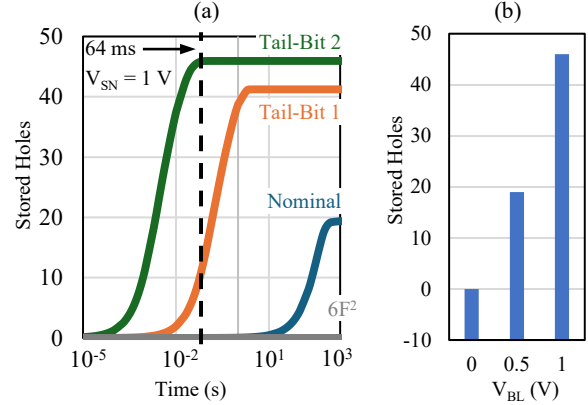


Fig. 2. The 4F² transistor stores holes in the hold state depending on the BL bias condition. (a) For a tail-bit transistor, enough holes may accumulate within the 64 ms refresh period to cause a V_T shift which degrades retention. (b) The number of stored holes increases with increased BL bias.

threshold voltage shift, ΔV_T . In the 4F² architecture, holes generated in the hold state accumulate in the body of the transistor [2][3]. For a nominal bit with low hole generation rate, the time required to generate any holes may be significantly greater than 64 ms, the refresh period of the DRAM array, and is therefore negligible. For “tail-bits” with process variations or defects, the generation rate may be high enough that there are

Tail-bit FBE ΔV_T and Retention Impact

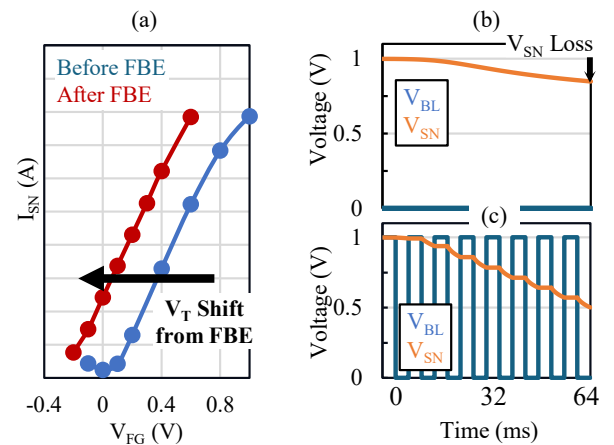


Fig. 3. (a) Transient I_d - V_g characteristic is recorded before FBE and after holes from FBE are accumulated in order to assess the FBE V_T shift. DRAM bit-cell retention is measured to assess impact of FBE on (b) static and (c) dynamic retention.

holes stored in the body within 64 ms (Tail-Bit 1). For the worst-case tail bits (Tail-Bit 2), the body may even become saturated with holes within the refresh period. Additionally, BL bias (V_{BL}) during the hold state increases the hole-generating electric field at the BL junction and forms a potential barrier which increases the number of holes stored (Fig. 2b). Crucially, these holes remain stored in the body for a short time even when V_{BL} is changed, e.g. reduced to 0 V during dynamic retention conditions. The ΔV_T from these excess holes leads to a higher transient leakage than would be expected from the steady state leakage, which can lead to catastrophic retention loss [4]. This hole storage poses a significant reliability risk for 4F² DRAM since it is both process- and history-dependent, making it difficult to deploy array-level algorithmic mitigation approaches. In this work, we deploy our DRAM Materials to Systems Co-Optimization (MSCOTM) [5] framework to analyze 4F² DRAM ‘d1’ retention sensitivity to process and temperature-induced floating body effects.

II. MODELING FRAMEWORK

The VCT and storage capacitor shown in Fig. 1 is simulated with the dimensions projected for a 10nm-class DRAM technology node. The driving phenomena for hole generation in the hold condition are modeled with Hurkx band to band tunneling and Shockley-Reed-Hall generation. For FBE ΔV_T benchmarking, the device is biased in the ‘d1’ hold condition for 64 ms with $V_{SN} = 1$ V and V_{BL} either 1 V or 0 V to generate and store holes in the body, as illustrated in Fig. 2a. Then, a series of fast voltage ramps and settling periods are applied to the Word-Line (WL)/Front Gate (FG) and Drain/BL electrodes for various front gate biases V_{FG} in order to measure the Id-Vg characteristic (Fig. 3a) with stored holes in the body – that is, before they flow out of the BL electrode. This curve is compared to the Id-Vg characteristic before the 64 ms hole accumulation period is applied. The shift in the Id-Vg characteristic is recorded as the FBE ΔV_T . After ΔV_T benchmarking, mixed mode simulations with electrode voltage sources and SN capacitor are used to benchmark bit-cell retention. Electrodes are set with a similar fast voltage ramp and settling period, and the storage node is set floating at $t = 0$ seconds. Both static retention (Fig. 3b), in which V_{BL} is kept constant at 0 V, and dynamic retention (Fig. 3c), in which V_{BL} toggles between 1 V and 0 V, are compared. The device of Fig. 3 shows worse retention from dynamic toggling due to the enhanced hole storage and V_T shift when $V_{BL} = 1$ V.

III. RESULTS AND DISCUSSION

Fig. 4 summarizes the device parameters investigated in this work, focusing on source/drain (S/D) junction profiles, back-gate overlap, front-gate oxide thickness, and silicon body thickness. Fig. 5a plots representative source/drain doping profiles for the reference device and device with junction roll-off of +9 nm/dec versus the reference device. As the junction roll-off becomes more gradual, the transverse electric field near the gate edges is enhanced, which results in a large GIDL current at low V_{FG} (Fig. 5b). As GIDL increases, the FBE ΔV_T shown in Fig. 5c increases from more hole storage, especially for $V_{BL} = 1$ V, in which both the SN and BL junctions contribute to hole

VCT Device Parameters

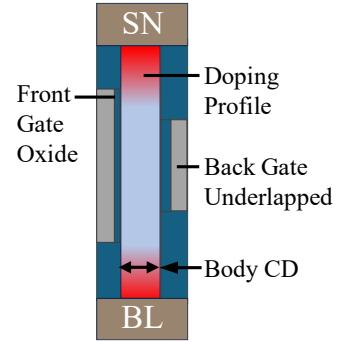


Fig. 4. Impact of Source/Drain Junction profiles, Back Gate Overlap to Junctions, Front Gate Oxide Thickness, and body thickness on FBE and dynamic retention were studied.

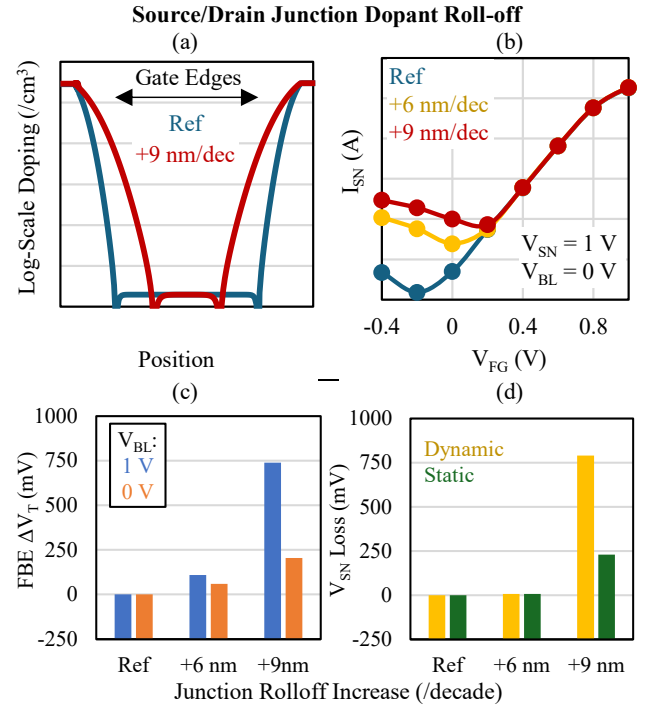


Fig. 5. (a) Gradual source/drain junctions enhance the electric field under the gate, (b) resulting in large GIDL current in the I_{SN} vs V_{FG} characteristic; (c) FBE V_T shift and (d) dynamic retention loss are abruptly increased at +9 nm/decade junction roll-off vs the reference device.

generation, and the potential barrier from the BL bias assists with hole storage. For the most extreme case of +9 nm/dec, $\Delta V_T = 740$ mV at $V_{BL} = 1$ V and $\Delta V_T = 220$ mV at $V_{BL} = 0$ V. Even though the bit-cell ‘d1’ state is retained during static retention (< 250 mV storage node loss), the dynamic retention loss is a staggering 790 mV. Fig. 6 investigates the effect of back-gate overlap, pictorially shown in Fig. 6a. During retention, the back gate is negatively biased to reduce leakage. The negatively biased, overlapped back gate slightly increases V_T and significantly enhances the electric field across the junctions, resulting in GIDL (Fig. 6b) and a steady increase in FBE with

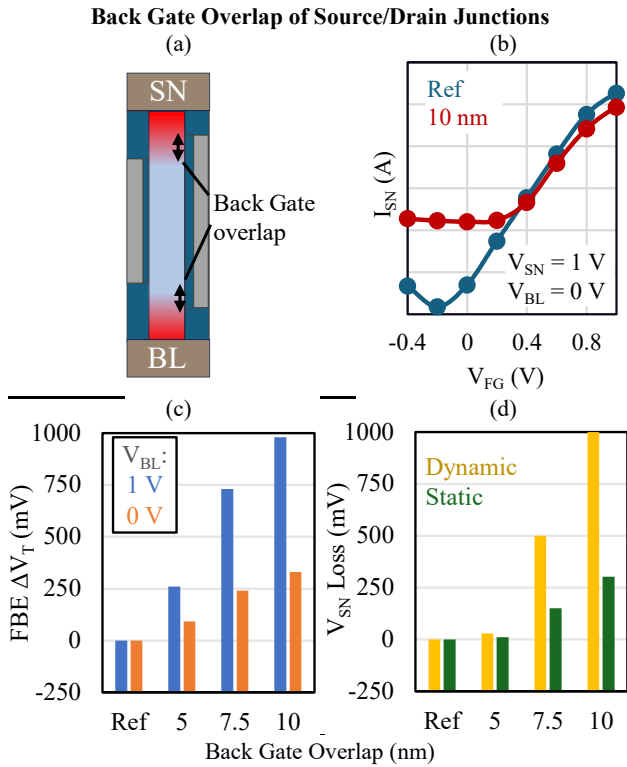


Fig. 6. (a) As the length of the negatively biased back gate is increased and overlaps the S/D junction profiles, (b) V_T is slightly increased and a large GIDL increase is seen from increased field at the junctions; (c) FBE and (d) dynamic retention are degraded; the most extreme cases cause complete loss of 'd1'.

overlap (Fig. 6c). Compared to the S/D junctions with +9 nm/dec roll-off, the 10 nm overlapped back gate has similar FBE for the $V_{BL} = 0$ V cases but worse FBE for $V_{BL} = 1$ V. Next, the front gate oxide thickness was reduced. Reduced front gate oxide thickness enhances the transverse electric field, showing a mild increase in FBE (Fig. 7a), but no degradation in retention was seen (Fig. 7b). Unlike prior trends, increased body thickness shows a very similar FBE ΔV_T for both $V_{BL} = 1$ V and $V_{BL} = 0$ V (Fig. 8a). In this case, sufficiently large body thickness creates

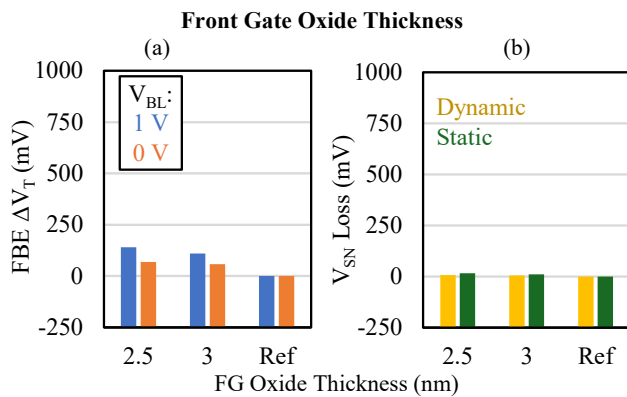


Fig. 7. Reduced Front Gate Oxide thickness to 2.5 nm causes only (a) a small increase in FBE but (b) no impact on dynamic retention.

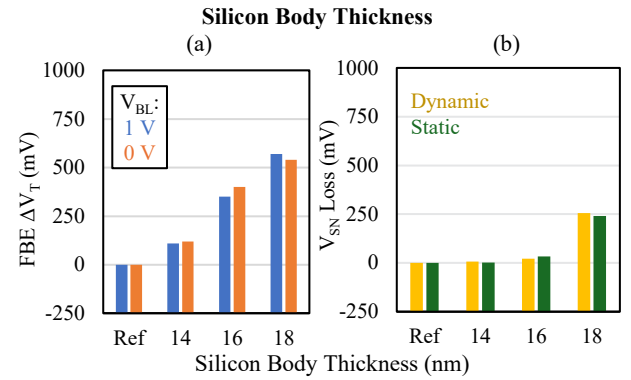


Fig. 8. Increased body thickness increases volume for hole storage, resulting in (a) similar FBE for $V_{BL} = 1$ V and 0 V, indicating a similar amount of holes are stored; therefore, (b) static and dynamic retention are degraded similarly.

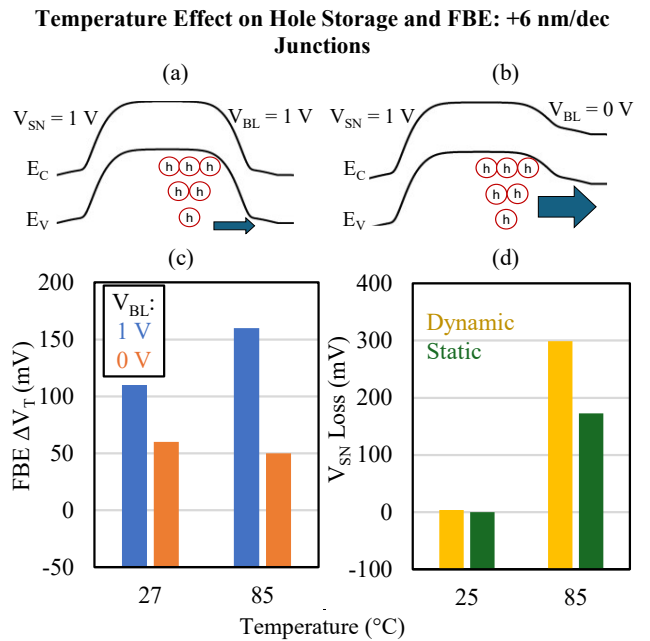


Fig. 9. (a) As the length of the negatively biased back gate is increased and overlaps the S/D junction profiles, (b) V_T is slightly increased and a large GIDL increase is seen from increased field at the junctions; (c) FBE and (d) dynamic retention are degraded; the most extreme cases cause complete loss of 'd1'.

a large volume for, and resultant amount of, hole storage, regardless of the electrostatic potential barrier at the BL junction. A resultant abrupt increase in both static and dynamic retention loss is seen at a relatively large 18 nm CD (Fig. 8b). Since the hole-induced FBE ΔV_T is similar for both values of V_{BL} , holes stored when $V_{BL} = 1$ V do not result in an increased leakage when $V_{BL} = 0$ V versus the static retention case. Therefore, although there is significant FBE, dynamic retention is not significantly more degraded than static retention. Finally, FBE at 85 $^{\circ}$ C was examined for the device with +6 nm/dec junction roll-off. At increased temperature, both the hole generation rate and average kinetic energy are increased. The band diagrams of Fig. 9a describe the impact for both BL

voltages. When $V_{BL} = 1$ V, the BL-side potential barrier is able to store the increased quantity of holes in the body, and the FBE ΔV_T is increased (Fig. 9b). When $V_{BL} = 0$ V, these holes with increased kinetic energy escape the body at the BL terminal, so there is a net reduction in FBE ΔV_T . At 85°C, the increased leakage degrades both static and dynamic retention loss when $V_{BL} = 0$ V, and additionally dynamic retention is degraded due to increased FBE at $V_{BL} = 1$ V.

IV. SUMMARY

In summary, we have developed a framework to analyze the impact of FBE on 4F² DRAM transistor ΔV_T and retention. Junctions overlap with the front and back gates cause moderate ‘d1’ static retention loss and catastrophic dynamic retention loss due to the large FBE at $V_{BL} = 1$ V. For cases in which the FBE ΔV_T at $V_{BL} = 1$ V and 0 V are similar, the dynamic retention loss is similar to the static retention loss.

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