

Efficient DC Simulation of Monolithic CFETs Using a Quasi-1D Approach

(Invited)

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Abstract—Recently, there have been some efforts to accelerate the technology computer-aided design (TCAD) device simulation by using an approximate solution at a target bias condition. In this work, we introduce two different approaches to generate such an approximate solution and discuss the importance of the applicability issue. As an application of the quasi-one-dimensional (quasi-1D) approach with region-wise analysis, the static noise margin of a complementary field-effect transistor (CFET) static random-access memory (SRAM) cell is efficiently calculated.

Index Terms—CFET, SRAM, TCAD, device simulation, process emulation, quasi-1D model

I. INTRODUCTION

The monolithic complementary field-effect transistor (CFET) [1] has been actively investigated as a strong candidate for the next-generation device architecture beyond the nanosheet MOSFET. Since it has multiple NMOS and PMOS channel stacks as well as a complicated middle-of-line (MOL) structure, its technology computer-aided design (TCAD) simulation becomes a non-trivial task. Exploration of the optimal device option requires repeated simulations over many structural variations. As a result, an efficient simulation method for CFETs is practically important.

In this work, we provide a brief overview of recent attempts to accelerate the TCAD device simulation and present an application to a CFET static random-access memory (SRAM) cell. In Section II, we briefly introduce the process emulator and the device simulator [2] used in this work. In Section III, two different approaches to generate an approximate solution are reviewed, with an emphasis on the quasi-one-dimensional (quasi-1D) approach with region-wise analysis. In Section IV, a CFET SRAM cell is efficiently simulated with the quasi-1D approach. The conclusion is made in Section V.

II. SIMULATION FRAMEWORK

A state-of-the-art semiconductor device has a complicated three-dimensional structure, which results from a long se-

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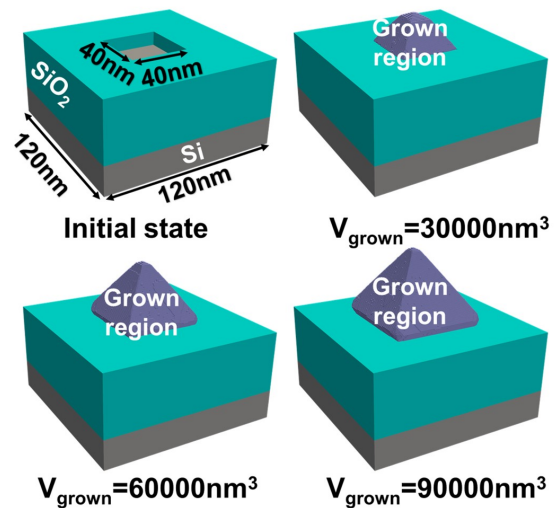


Fig. 1. Snapshots of the grown region during the KLMC simulation of the selective epitaxial growth. A test structure with a 40 nm-by-40 nm square trench is considered.

quence of fabrication steps. It becomes increasingly difficult to prepare a realistic structure by simply drawing the final structure using a structure editor. Instead, process emulators (for example, [3]–[6]) are actively being used. Our in-house process emulator was initially based on the level-set method [7]. We have recently converted it into a voxel-based code for robust implementation. The emulator has been applied to several device structures, including forksheet FETs [7] and CFETs [8], [9]. In most cases, simple geometric operations are applied to emulate process steps such as deposition and etching. However, in the case of source/drain selective epitaxial growth, it is difficult to reproduce realistic shapes of source/drain regions with geometric operations. Therefore, the kinetic lattice Monte Carlo (KLMC) simulation [10] is integrated into the process emulator, as shown in Fig. 1. After the KLMC simulation, the atomistic epitaxial structure is converted into voxels for further process emulation.

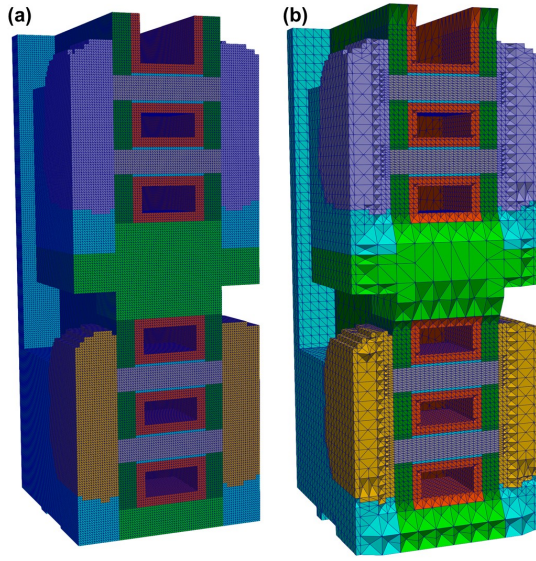


Fig. 2. Meshing results for the CFET structure: (a) original fine mesh with a uniform voxel spacing of 0.5 nm obtained from voxel-based process emulation and (b) coarse mesh for device simulation.

Since we adopt the voxel-based description during the process emulation, the final device structure is naturally partitioned into small voxels. However, the total number of these voxels is too large to be directly used in device simulation. In this work, the total number of vertices is significantly reduced by introducing a coarse mesh, as shown in Fig. 2. The user can specify the maximum element size in each region and the maximum face size on each region interface. The resultant mesh is directly used in our in-house device simulator [2], [11].

III. ACCELERATION OF DEVICE SIMULATIONS

The idea to skip the time-consuming bias ramping procedure by obtaining a good initial guess at the target bias condition can be found in several early works [12], [13]. However, such attempts have not been widely adopted in practice, presumably due to robustness and generality issues. As a result, the bias ramping scheme is almost universally used in modern device simulators, and it accounts for a large portion of the device simulation time. As the demand for faster device simulation grows, the efficiency improvements studied decades ago become practically important again. In this context, we revisit this idea.

A method to use an approximate solution generated by a trained neural network was proposed in [14] and later expanded and improved [15]–[18]. Related approaches have been reported by other groups (for example, [19], [20]). From these studies, we can find that a trained neural network can provide a sufficiently accurate initial solution for device simulation. Since the training cost is not negligible, it is desirable to use a once-trained neural network in a wide range of applications. However, for an unseen device outside the training range, or even for a new device architecture, such

applicability is not guaranteed. An alternative approach, free from this applicability issue, is preferable.

Instead of a purely data-driven approach, we construct a model which mimics the original system as closely as possible. The derivation procedure of a compact model for the MOSFET can be a useful guide for this attempt. While the final expression of any compact model considers the relations among terminal quantities, its derivation is rigorously performed with the gradual channel approximation [21] and the Pao-Sah double integral [22]. However, the rigorous derivation alone does not yield a closed-form expression. In order to obtain a simple final expression suitable for circuit simulation, a number of additional approximations are introduced. Among them, the charge model, which relates the channel charge to the gate voltage, is of central importance.

By focusing only on gate-all-around structures, we can greatly reduce the modeling complexity while maintaining a wide application range. The BSIM-CMG model, an industry-standard compact model for multigate MOSFETs, adopts a universal charge model [23]. We have found that the universal charge model can be rigorously derived from any gate-all-around MOS cross-section [24]. Inspired by such generality, we adopt this charge model and solve the current continuity equation along the channel direction. Since the numerical solution is obtained only along one dimension, this model is named the quasi-1D model. This quasi-1D model was first applied to long-channel MOSFETs [25]. The simulation domain contains the ungated regions, which simplifies the boundary conditions. Although it works well in long-channel devices, application to short-channel devices requires additional effort. In [26], the lateral electric field is included in the charge model, going beyond the gradual channel approximation. With these extensions, a channel stack with a short gate length can be simulated accurately. Since the CFET has multiple channel stacks connected through the source/drain regions, the entire device structure cannot be described with the quasi-1D model alone. Therefore, by applying the region-wise analysis [27], the non-channel regions are identified and modeled as linear networks characterized by their admittance parameters.

It is noted that the applicability of this approach is guaranteed by the generality of the universal charge model, which holds for any gate-all-around cross-section [24]. Moreover, since no training procedure is involved, a new device structure can be handled with minimal preparation.

IV. SRAM RESULTS

The quasi-1D solution can be used as an initial guess for the TCAD simulation. Moreover, when its accuracy is sufficiently high, the quasi-1D model itself can be directly used to obtain the electrical characteristics. In this section, we demonstrate the application of the quasi-1D model to the simulation of a CFET SRAM cell. Fig. 3 illustrates the CFET structure and its corresponding quasi-1D representation used in this work.

Prior to the SRAM simulation, the on-current characteristics of the NMOS and PMOS devices constituting the CFET are rapidly obtained through accelerated TCAD simulation. The

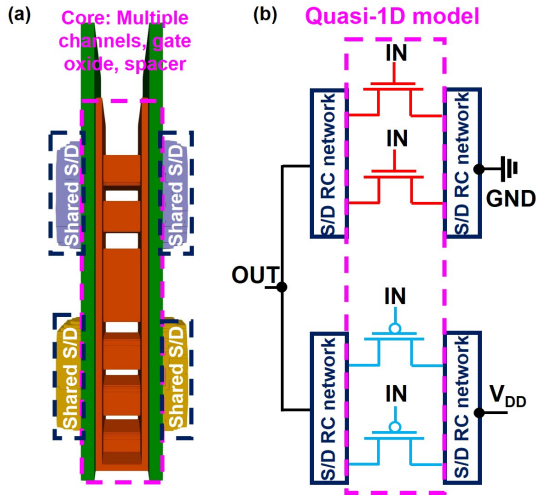


Fig. 3. Illustration of (a) the CFET structure and (b) its corresponding quasi-1D representation. The multiple channels and shared source/drain regions are represented by quasi-1D models and source/drain RC networks, respectively.

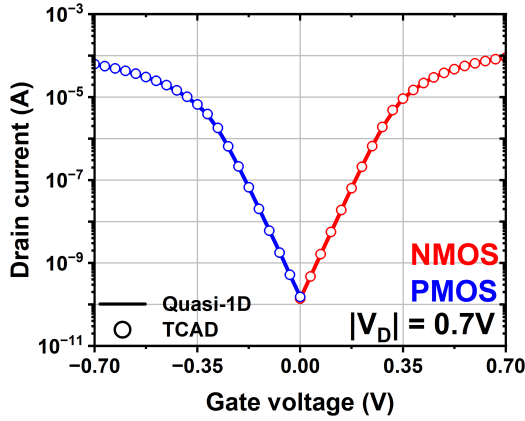


Fig. 4. Comparison of the current–voltage characteristics obtained using TCAD and the quasi-1D model. The quasi-1D model is calibrated under the on-current condition.

extracted on-current characteristics are then used to calibrate the quasi-1D model. Both simulations employ the Mujsaba mobility model [28] and the high-field saturation model [29]. The same set of model parameters is used in both simulations, and no additional model parameters are introduced in the quasi-1D model. Furthermore, a simplified density-gradient model [30] is adopted to account for quantum confinement effects. Fig. 4 presents the current–voltage characteristics, showing excellent agreement between the TCAD and quasi-1D results.

Subsequently, the calibrated quasi-1D model is directly applied to the CFET SRAM simulation without any further calibration. A conventional six-transistor SRAM cell, consisting of four NMOSFETs and two PMOSFETs, is considered in this study. The voltage transfer characteristics of the CFET SRAM cell obtained using TCAD and the quasi-1D model are compared under the hold, read, and write operating conditions

in Fig. 5. The static stability of the SRAM cell is evaluated through the hold static noise margin (HSNM), read static noise margin (RSNM), and write static noise margin (WSNM) extracted from the voltage transfer characteristics. The quasi-1D model accurately reproduces the voltage transfer characteristics under the hold, read, and write operating conditions, and all extracted noise margins show good agreement with the TCAD results.

In addition, Fig. 6 compares the simulation times required to obtain the voltage transfer characteristics for the extraction of each SNM. All simulations are performed using the same maximum step size of 0.014 V for each bias-ramping step and a single CPU core. The simulation time of the quasi-1D model includes the time required for the region-wise structure analysis. As shown in Fig. 6, the quasi-1D model is at least 13.9 times faster than TCAD in this example. These results demonstrate that the quasi-1D model can be used not only to accelerate TCAD simulations but also to efficiently reproduce electrical characteristics with accuracy comparable to that of TCAD.

V. CONCLUSION

Recent approaches to accelerate the TCAD device simulation have been reviewed, with an emphasis on the quasi-1D model with region-wise analysis. As a practical application, the voltage transfer characteristics of a CFET SRAM cell have been calculated. The quasi-1D model reproduces the noise margins accurately, while it is much faster than the TCAD simulation. Since its applicability is supported by the generality of the universal charge model, the quasi-1D model can be applied to other gate-all-around devices with minimal preparation.

REFERENCES

- [1] J. Ryckaert, P. Schuddinck, P. Weckx, G. Bouche, B. Vincent, J. Smith, Y. Sherazi, A. Mallik, H. Mertens, S. Demuyne, T. Huynh Bao, A. Veloso, N. Horiguchi, A. Mocuta, D. Mocuta, and J. Boemmel, "The complementary FET (CFET) for CMOS scaling beyond N3," in Proc. Symp. VLSI Technol., pp. 141–142, 2018.
- [2] S.-M. Hong, I. K. Kim, S.-W. Jung, M.-S. Jang, P.-H. Ahn, T. Oh, G.-T. Jang, and K.-W. Lee, "G-Univers: A collection of in-house technology computer-aided design simulators as a platform for developing new simulation capabilities," in Proc. EDTM, 2025.
- [3] M. Hargrove, S. Wen, D. Yim, K. Egelhofer Ruegger, P. Nanja, S. Sarkar, B. Lowe, B. Vincent, J. Ervin, and D. M. Fried, "Review of virtual wafer process modeling and metrology for advanced technology development," J. Micro/Nanopattern. Mater. Metrol., vol. 22, Art. no. 031209, 2023.
- [4] Z. Stanojević, G. Strof, F. Schanovsky, K. Steiner, O. Baumgartner, C. Kernstock, and M. Karner, "Cell Designer – a comprehensive TCAD-based framework for DTCO of standard logic cells," in Proc. ESSDERC, pp. 202–205, 2018.
- [5] T. Reiter and L. Filipovic, "ViennaPS: A flexible framework for semiconductor process simulation," SoftwareX, vol. 32, Art. no. 102453, 2025.
- [6] W. Choi, H.-K. Noh, H.-H. Park, A.-T. Pham, S. Jin, B. Lee, C. Ahn, H. Kubotera, and D. S. Kim, "Hierarchical simulation of monolithic CFETs using atomistic and continuum models," in Proc. SISPAD, 2024.
- [7] I. K. Kim, S.-C. Han, G. Park, G.-T. Jang, and S.-M. Hong, "Effect of Si separator in forksheet FETs on device characteristics investigated by using in-house TCAD process emulator and device simulator," in Proc. SISPAD, pp. 225–228, 2023.

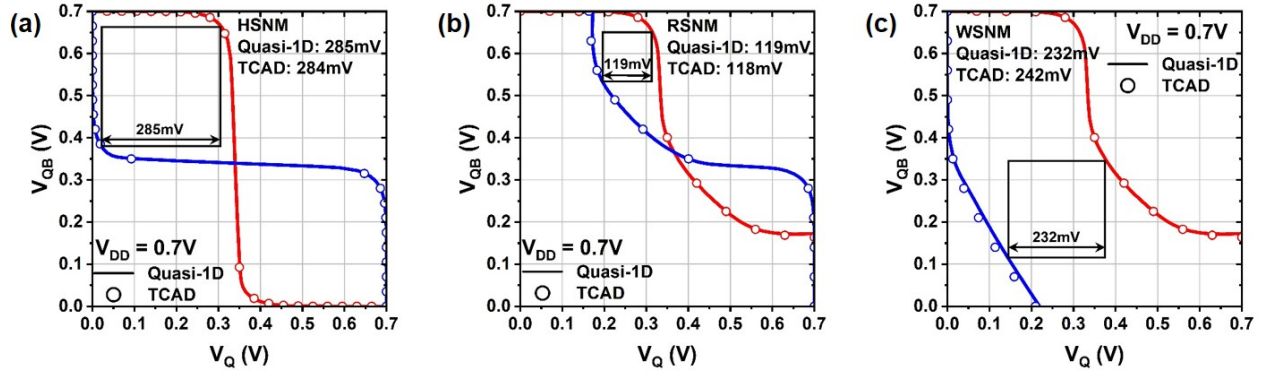


Fig. 5. Comparison of the voltage transfer characteristics of the CFET SRAM cell obtained using TCAD and the quasi-1D model. The voltage transfer characteristics are represented by the storage node voltages V_Q and V_{QB} . The HSNM, RSNM, and WSNM extracted from the corresponding curves are also compared. Excellent agreement is observed between the TCAD and quasi-1D results. (a) HSNM, (b) RSNM, and (c) WSNM.

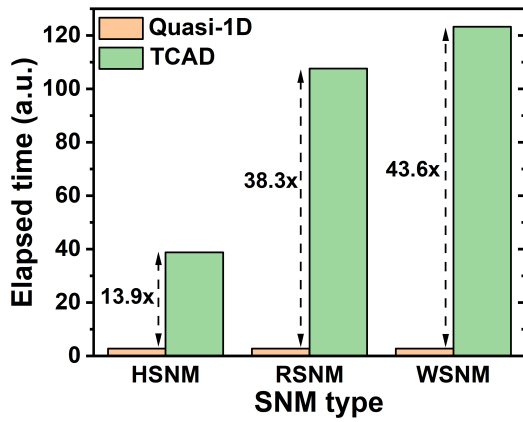


Fig. 6. Comparison of the elapsed times for the voltage transfer characteristics used to extract HSNM, RSNM, and WSNM.

- [8] S.-W. Jung, I. K. Kim, K.-W. Lee, and S.-M. Hong, "Process emulation and device simulation of monolithic CFET inverter and transmission gate with split-gate structure," in Proc. SISPAD, 2024.
- [9] M.-S. Jang, S.-W. Jung, and S.-M. Hong, "Stress simulation of CFET inverters with unmerged SiGe S/D and wrap-around contact," in Proc. SISPAD, 2025.
- [10] R. Chen, W. Choi, A. Schmidt, K.-H. Lee, and Y. Park, "A new kinetic lattice Monte Carlo modeling framework for the source-drain selective epitaxial growth process," in Proc. SISPAD, pp. 9–12, 2013.
- [11] S.-M. Hong and J.-H. Jang, "Numerical simulation of plasma oscillation in 2-D electron gas using a periodic steady-state solver," IEEE Trans. Electron Devices, vol. 62, pp. 4192–4198, 2015.
- [12] K.-C. Wu, R. F. Lucas, Z.-Y. Wang, and R. W. Dutton, "New approaches in a 3-D one-carrier device solver," IEEE Trans. Computer-Aided Design, vol. 8, pp. 528–537, 1989.
- [13] B. Meinerzhagen, H. K. Dirks, and W. L. Engl, "Quasi-simultaneous solution method: A new highly efficient strategy for numerical MOST simulations," IEEE Trans. Electron Devices, vol. 32, pp. 2131–2138, 1985.
- [14] S.-C. Han and S.-M. Hong, "Deep neural network for generation of the initial electrostatic potential profile," in Proc. SISPAD, 2019.
- [15] S.-C. Han, J. Choi, and S.-M. Hong, "Electrostatic potential profile generator for two-dimensional semiconductor devices," in Proc. SISPAD, pp. 297–300, 2020.
- [16] S.-C. Han, J. Choi, and S.-M. Hong, "Acceleration of semiconductor

- device simulation with approximate solutions predicted by trained neural networks," IEEE Trans. Electron Devices, vol. 68, pp. 5483–5489, 2021.
- [17] S.-C. Han, J. Choi, and S.-M. Hong, "Acceleration of three-dimensional device simulation with the 3D convolutional neural network," in Proc. SISPAD, pp. 52–55, 2021.
- [18] S.-C. Han, I. K. Kim, and S.-M. Hong, "Accelerated simulation and performance optimization of 3D multigate logic transistors by using neural networks," in Proc. EDTM, 2023.
- [19] W.-J. Lee, W.-T. Hsieh, B.-H. Fang, K.-H. Kao, and N.-Y. Chen, "Device simulations with a U-Net model predicting physical quantities in two-dimensional landscapes," Sci. Rep., vol. 13, Art. no. 731, 2023.
- [20] W. Jang, S. Myung, J. M. Choe, Y.-G. Kim, and D. S. Kim, "TCAD device simulation with graph neural network," IEEE Electron Device Lett., vol. 44, pp. 1368–1371, 2023.
- [21] W. Shockley, "A unipolar 'field-effect' transistor," Proc. IRE, vol. 40, pp. 1365–1376, 1952.
- [22] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors," Solid-State Electron., vol. 9, pp. 927–937, 1966.
- [23] J. P. Duarte, S.-J. Choi, D.-I. Moon, J.-H. Ahn, J.-Y. Kim, S. Kim, and Y.-K. Choi, "A universal core model for multiple-gate field-effect transistors. Part I: Charge model," IEEE Trans. Electron Devices, vol. 60, pp. 840–847, 2013.
- [24] K.-W. Lee and S.-M. Hong, "Derivation of a universal charge model for multigate MOS structures with arbitrary cross sections," IEEE Trans. Electron Devices, vol. 69, pp. 3014–3021, 2022.
- [25] K.-W. Lee and S.-M. Hong, "Acceleration of semiconductor device simulation using compact charge model," Solid-State Electron., vol. 199, Art. no. 108526, 2023.
- [26] K.-W. Lee and S.-M. Hong, "Quasi-1D model for bridging TCAD simulation and compact modeling of gate-all-around MOSFETs," in Proc. ICMC, 2025.
- [27] K.-W. Lee, I. K. Kim, S.-W. Jung, M.-S. Jang, and S.-M. Hong, "Combining quasi-one-dimensional modeling with region-wise structure analysis for rapid technology computer-aided design simulations of gate-all-around MOSFETs," Commun. Eng., vol. 4, Art. no. 165, 2025.
- [28] S. A. Mujtaba, "Advanced mobility models for design and simulation of deep submicrometer MOSFETs," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, USA, 1995.
- [29] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," IEEE Trans. Electron Devices, vol. 22, pp. 1045–1047, 1975.
- [30] A. Wettstein, A. Schenk, and W. Fichtner, "Quantum device-simulation with the density-gradient model on unstructured grids," IEEE Trans. Electron Devices, vol. 48, pp. 279–284, 2001.