

Fast exchange energy simulation in Si spin qubits for point defect variability assessment

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Abstract—Exchange energy is a key parameter in silicon spin qubits. Here we introduce a new methodology for fast calculation of exchange energy. This methodology is applied to gate geometry and voltage optimization, aiming to reduce the detrimental effects of point-charge defects on the exchange-mediated coupling between qubits. The results demonstrate the efficiency of the optimization and use of a back gate to reduce point defect.

Index Terms—FD-SOI spin qubit, point defect, variability, exchange energy, two qubit gate.

I. INTRODUCTION

Variability is a major obstacle to scaling quantum computers. FD-SOI spin qubits are a promising candidate to address this challenge as they benefit from decades of microelectronics expertise in variability reduction [1]. Point defects remain a source of variability in these devices. [2] Charges trapped in point defects are detrimental for the exchange energy J between two qubits which directly governs the speed of two-qubits gate operations [2]. Previous studies have assessed the impact of point defects on J using a variety of computational approaches, including Full Configuration Interaction (FCI) [2], other many-body Hamiltonian techniques [3], and Monte Carlo methods [4]. These approaches are computationally expensive, limiting the exploration of device geometries, optimal bias ranges, and their direct use by experimentalists. In this work, we present an efficient methodology based on a single-particle Effective Mass Approximation (EMA) [5] Hamiltonian combined with post-processing. We apply this method to explore device geometries, optimize gate voltage ranges in the presence of point defects, and compare our simulations against experimental data.

II. DEVICE

The device under study is based on a FD-SOI architecture and is depicted in Fig.1. Two plunger gates (P_1 and P_2) are used to form the two potential wells required for the double dot in the silicon channel. The potential barrier between the dots can be tuned via the exchange gate Ex_1 . The regime of interest is one in which two electrons are loaded into the double dot from a reservoir, after which a negative voltage is applied to gates Ex_0 and Ex_2 to suppress any coupling with the reservoirs. A back gate (BG) allows the electron position to be controlled along the channel height (z axis). The geometrical parameters explored in this work are the width of

the exchange gates (L_{Ex}) and the distance between the channel and the bottom of the exchange gates (H_{Ex}). Two H_{Ex} (L_{Ex}) have been explored, H_1 and H_2 (respectively L_1 and L_2) with $H_1 < H_2$ (respectively $L_1 < L_2$). The energy difference of an electron in the potential well formed by P_1 and the one formed by P_2 is commonly referred to as the detuning, denoted ϵ . The point defect introduced in the simulations are placed in the area in between P_1 and P_2 as indicated by the yellow point in Fig. 1.

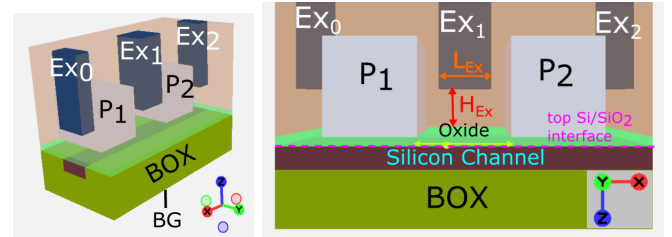


Fig. 1. (Left) 3D model of the device. (Right) Cut along channel of the device. H_{Ex} is indicated and L_{Ex} is indicated. Point defects are located at the interface between the silicon channel and oxide layers, along the region spanned by the yellow arrow.

III. METHODOLOGY

The first step in estimating the impact of a point defect on J is to compute the electrostatic potential in its presence. Since the only electrons in the system are the two loaded beneath the gates, we solve the linearized Poisson equation using QTCAD [6]. Linearity is exploited following [7]: the potential contribution ϕ_g of each gate (or point defect) is simulated individually, and the potential for an arbitrary configuration is obtained as $V_{\text{total}} = \sum_g V_g \phi_g$, where V_g is the voltage applied to gate g . In previous works [8], t_c is extracted at zero detuning ($\epsilon = 0$) by enforcing a symmetric configuration ($V_{P_1} = V_{P_2}$, $V_{Ex_0} = V_{Ex_2}$) and inspecting the two lowest EMA energy levels. In the presence of a point defect the system is no longer symmetric, and optimization techniques are required to restore $\epsilon < t_c$, at the cost of tens of EMA calculations. To avoid this overhead we instead operate at $\epsilon > t_c$ and perform a single EMA calculation to extract the energy splitting ΔE and the associated wavefunctions ψ_1 and ψ_2 . The ratio $\frac{t_c}{\epsilon}$, inferred from ψ_1 and ψ_2 , is then used together with ΔE to extract t_c using the theoretical form of a two-level Hamiltonian.

The exchange energy is then estimated using perturbation theory as $J = \frac{4t_c^2}{E_c}$ [9]. The impact of a point defect can be partially reduced by increasing V_{Ex1} , the upper limit being the formation of a spurious ground state under gate $Ex1$ (also referred to as the third dot throughout the remainder of this article). An optimization procedure for V_{Ex1} yields the maximum attainable J before such a state forms.

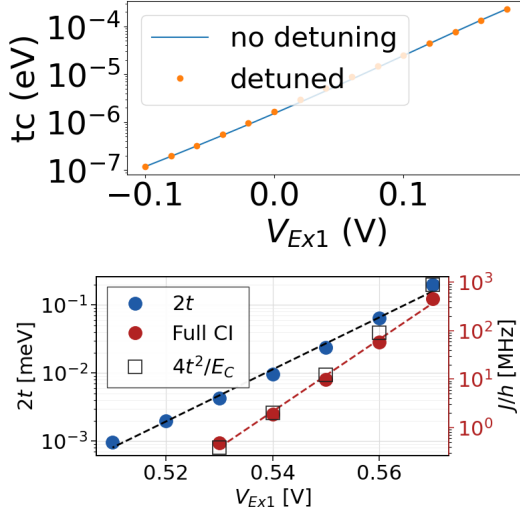


Fig. 2. (Top) Comparison of a EMA calculation of tunnel coupling depending on V_{Ex1} in a perfectly symmetric case (blue line) and with the method presented in methodology section with a detuning of 10^{-5} eV (orange circle). (Bottom) Comparison of J calculations depending of V_{Ex1} with full CI simulations (red point) and the methodology presented below (square) in a different FD-SOI device.

IV. RESULTS

A. Point defect simulations

The tunnel coupling extraction method at $\epsilon > t_c$ is benchmarked against the conventional $\epsilon = 0$ approach, showing excellent agreement (Fig. 2 top). The estimate of J using perturbation theory is compared to full CI on the bottom of Fig. 2. The perturbation theory method is 50 times faster than the full CI. This result should be nuanced quantitatively, as other studies report a discrepancy between the exact exchange energy and this approximation in SiGe devices [10]. It nevertheless allows us to obtain an upper bound for the exchange energy and to qualitatively compare the designs and the effects at play.

Top of Fig 3 shows maximum attainable energy J optimized over V_{Ex1} for a single point defect introduced at various positions along and across the channel at the top Si/SiO₂ interface. The target value for J is 4×10^{-8} eV, corresponding to a gate speed of 10 MHz, and the reported yield corresponds to the fraction of defect positions for which this threshold can be reached (highlighted in blue). Defects located beneath gate $Ex1$ can effectively be compensated by tuning V_{Ex1} . A wider $Ex1$ gate allows a larger fraction of defect positions to be compensated.

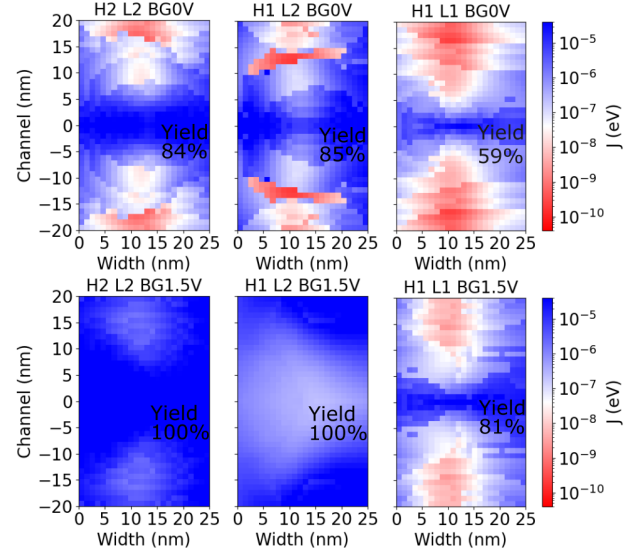


Fig. 3. (Top) Colormap of maximal J depending of the position of the defect for different pairs H_{ex} and L_{ex} . Each point defect position corresponds to a square on the colormap and the color represent the maximum achievable J . (Bottom) Same figures but with a positive voltage V_{BG} .

These observations can be understood from the potential landscape (Fig. 4). To compensate for the defect-induced potential without forming a spurious third dot, gate $Ex1$ must induce a potential as uniform as possible along the channel. The case with the smallest L_{ex} is the more likely to form a spurious dot. The t_c is exponentially dependant on the potential barrier in between the potential well. In the case of a third dot the maximum of the potential barrier is not under the gate $Ex1$ anymore but in between P_i and $Ex1$, in a region where it is more difficult to correct the system using the different gates.

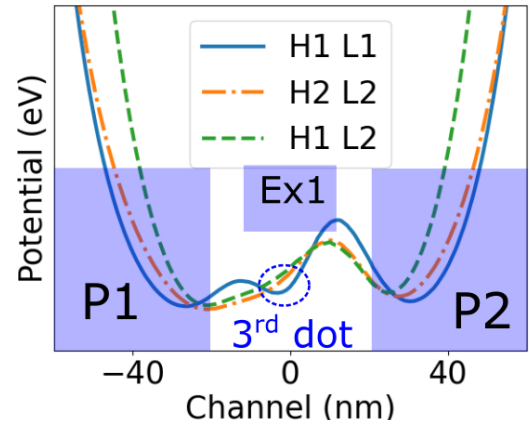


Fig. 4. Cut of the potential along the channel for the different H_{ex} and L_{ex} with a point defect between $Ex1$ and $P2$. A third dot is seen in the $H1 L1$ case.

Applying a positive back-gate voltage V_{BG} further improves the yield across all geometries (Fig. 3), as it displaces the electrons away from the top interface defects. This result

quantitatively demonstrates the effectiveness of back-gate tuning in mitigating point defect variability. Some defects are also present at the bottom Si/SiO₂ interface (between the channel and the BOX), although their density is generally lower than at the top gate oxide interface [11]. Displacing the electrons away from the top interface via the back gate therefore brings them closer to the bottom interface, which, while less defective, remains a source of variability.

To account for both interfaces, we ran simulations with a single point defect at the top interface and, separately, at the bottom interface. In these simulations, we tuned the back-gate voltage to find the best trade-off between the wave function position at the top and bottom interfaces. For geometry L2 and H2, it is possible to find a back-gate voltage V_{int} for which the exchange energy remains above 4×10^{-8} eV for any position of a single point defect, whether at the bottom or top interface (Fig. 5). This sweet-spot voltage V_{int} does not fully resolve the point defect issue, however. As mentioned, the quantity $J = \frac{4t_c^2}{E_c}$ is more of an upper bound than a precise value for the exchange energy. A single defect at the top interface corresponds to a defect density on the order of 10^{-10} cm⁻², close to the state-of-the-art value for the best interfaces in the silicon MOSFET industry [12]. There is a non-negligible chance of finding more than one defect at the top or bottom interface and in this case it seems difficult to compensate the potential with the backgate or the gate Ex_1 .

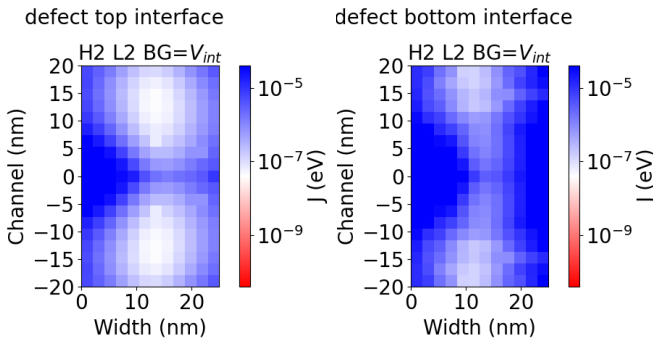


Fig. 5. (Left) Colormap of maximal J depending of the position of the defect located at the top interface for different pairs for H2/L2 geometry. Each point defect position corresponds to a square on the colormap and the color represent the maximum achievable J . (Right) Same figures but with point defect at the bottom interface

B. Comparison with experiments

The devices are first calibrated at room temperature (RT) using the Sentaurus software [13]. They are then operated as transistors by sequentially activating different gates. The source-to-drain current is measured as a function of the gate voltages P_i . This procedure is used to characterize the capacitive coupling of each gate type through subthreshold swing measurements [14].

The first gates investigated are the plunger gates P_i . The subthreshold swing provides a measure of their capacitive coupling to the channel, while the threshold voltage (V_{th})

can be used to verify that the gate workfunction is correctly calibrated. The influence of the back gate is assessed by monitoring the shift in V_{th} as a function of V_{BG} . The same characterization is performed for the exchange gates Ex_i , whose barrier height can be tuned through the fabrication process.

As shown in Fig. 6, the calibration yields a good agreement between simulations and experiment for the room temperature (RT) electrostatics of the P_i gates. The back-gate dependence is also well captured by the calibration. Notably, both in experiment and simulation, the subthreshold swing is larger for $V_{BG} = 0$ V. This can be explained by the fact that in this regime the potential minimum is located under Ex_1 rather than under the P_i gates. Consequently, the measured subthreshold swing reflects the capacitive coupling of P_i to the region underneath Ex_1 , rather than to the region directly beneath P_i itself. This behavior is no longer observed for positive back-gate voltages, where the potential barrier is restored under P_i .

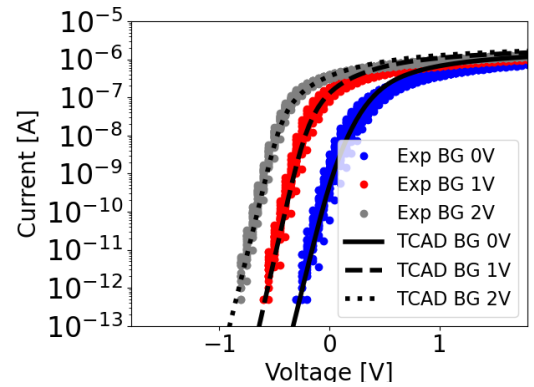


Fig. 6. Comparison between RT measurements of I_{SD} versus P_i gates voltage and Technology Aided Computer Design (TCAD) simulations.

Our methodology relies on t_c , whose dependence on V_{Ex_1} can be extracted from experimental measurements. In the isolated regime, a single electron can be localized under gate P_1 by applying a higher voltage on this gate. A fast voltage pulse is then applied to gate P_2 to create a deeper potential well beneath it, making the P_2 site energetically favorable. The electron will tunnel from P_1 to P_2 , and the characteristic time for this transition to occur is proportional to $1/t_c$. This measurement can be repeated for different values of V_{Ex_1} , allowing the dependence of t_c on V_{Ex_1} to be extracted [15].

This procedure was performed for several process splits with different exchange gate heights H_{Ex} .

The comparison between the experimental t_c tunability and the simulations is shown in Fig. 7. All splits were calibrated at RT as described previously. The simulated t_c as a function of V_{Ex_1} shows good agreement with the experimental data. As expected, the process splits with larger H_{Ex} exhibit lower t_c tunability. The tunability is approximately linear in V_{Ex_1} , consistent with expectations from the Wentzel–Kramers–Brillouin (WKB) [16]. Assuming the approximation $J \approx 4t_c^2/E_c$ holds, the tunability of J would be approximately 46 dec/V for

process split 1. This is larger than values reported by other groups working on silicon spin qubits, which range from 9 dec/V to 28 dec/V [17] [18].

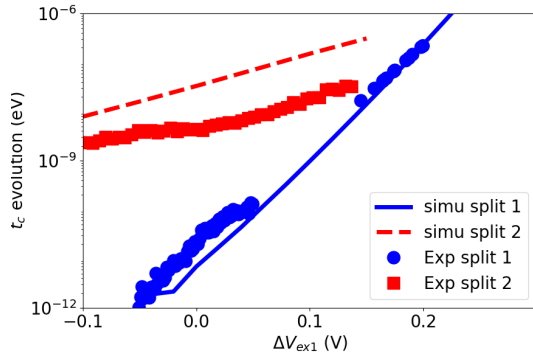


Fig. 7. Comparison of t_c evolution between simulations and experiment for two different H_{ex} (split 1 and split 2).

V. CONCLUSION

The proposed methodology achieves a tenfold speedup in the simulation of exchange energy J and was used in the context of point defect. This gain in computation time enables the investigation of various gate voltage configurations and point defect effects on the tunnel coupling, thereby guiding both device design and experimental measurements. The back gate proves effective in reducing the impact of top-interface point defects. The exchange gate width L_{Ex} is found to be the dominant factor governing the ability to compensate point defect variability via V_{Ex1} . The computational efficiency of the method, combined with its experimental validation, makes it a valuable tool for the real-time interpretation of two-qubit gate experiments.

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