

PrimeSim D2D: A Scalable, Machine Learning-assisted Data-Driven Modeling Framework for Fast DTCO

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Abstract— This work introduces PrimeSim D2D, a data-to-design (D2D) modeling framework designed to overcome the modeling bottleneck in design-technology co-optimization (DTCO). Integrated with Synopsys PrimeSim simulator, PrimeSim D2D combines lookup table (LUT) and neural network (NN) techniques to deliver accurate, efficient, and noise-resilient device models. NN models complement LUTs or operate independently to smooth noisy data, addressing limitations of conventional data-driven approaches. The framework incorporates advanced methods for geometry and temperature scalability, process variation (PV), local layout effects (LLE), and junction modeling. By enabling robust interpolation, and perturbation-based PV/LLE handling, PrimeSim D2D achieves high accuracy across diverse conditions with significantly reduced turnaround time, making it practical for DTCO workflows and real-world designs.

Keywords—DTCO, compact model, machine learning, process variation, local layout effect

I. INTRODUCTION

Design-technology co-optimization (DTCO) has become the key methodology for advancing semiconductor technologies by enabling concurrent technology and design development [1]. A major bottleneck in DTCO is compact model generations, which traditionally requires extensive parameter extraction from measurements or TCAD data that can take days to weeks (Fig. 1). Existing automated approaches using genetic algorithms [2] or machine learning (ML) [3], [4] are limited in handling the hundreds of parameters in standard models, and emerging devices exacerbate this challenge due to novel physics and lack of established models.

Neural network (NN)-based models [5], [6] and lookup table (LUT) [7] approaches have been proposed to accelerate model creation. NN models learn device behavior directly from data, while LUT models offer fast turnaround without sacrificing fidelity. However, both lack quasi-physical parameters critical for modeling process variation (PV) and local layout effects (LLE), and they face scaling challenges across geometry ranges. NN models require large datasets and long training times, while LUT models struggle with noisy data. There is an attempt to include quasi-physical parameters in NN models to handle PV and LLE [8], which still require further validations. To address these issues, we introduce PrimeSim D2D, a solution supporting LUT and NN models with PV/LLE perturbation, noise-resilient modeling, and advanced interpolation for practical process design kit (PDK) usage.

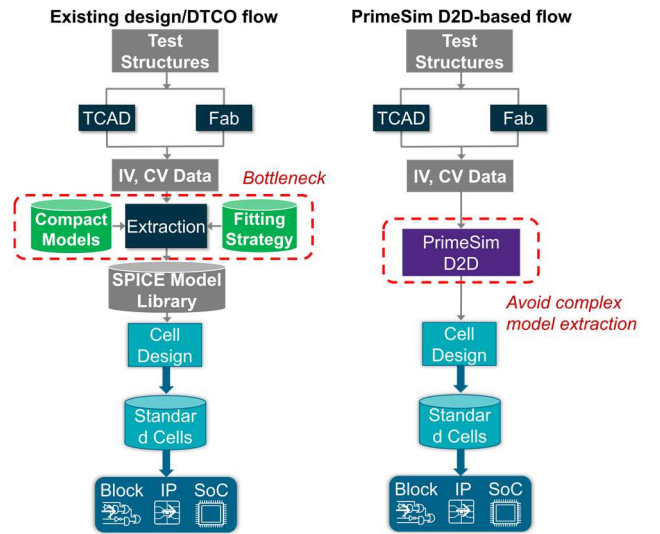


Fig. 1. The existing DTCO flow and the PrimeSim D2D-based flow. PrimeSim D2D avoids the model development and extraction bottlenecks by directly creating data-based models.

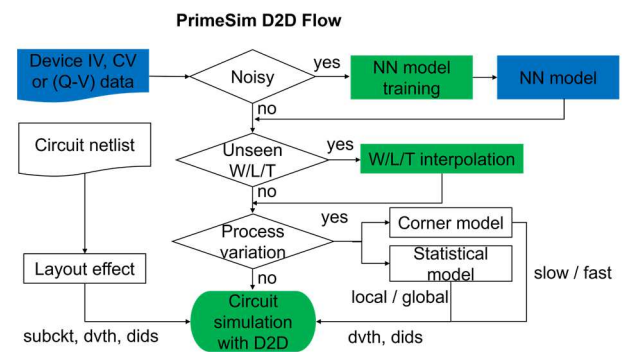


Fig. 2. The modeling flow of PrimeSim D2D. PrimeSim D2D supports LUT and NN models. NN models can be used to smooth out data noises. It contains advanced interpolation techniques for unseen W/L/T. It also supports process variation and layout effect modeling through perturbation and subcircuit methods.

II. FRAMEWORK

Fig. 2 illustrates the modeling flow of PrimeSim D2D. User-provided device IV/CV/QV data is imported into PrimeSim to construct LUT-based models using robust interpolation and extrapolation techniques, ensuring accuracy

and continuity. When measured data contains noise, LUT models may suffer from convergence issues. To mitigate this, PrimeSim D2D employs NN-based models that smooth noisy data. As shown in Fig. 3, by choosing the appropriate model architecture to avoid overfitting, the model can generate smooth IV and CV curves when the data contains noise. The simulator automatically trains NN models and converts them into built-in SPICE-compatible representations for optimized performance. NN models can either generate smooth LUTs derived from NN outputs or be directly evaluated as SPICE NN models during circuit simulation. SPICE NN models offer two key advantages: reduced memory footprint compared to full LUTs and fully analytical behavior with C-infinite continuity across all bias regions to enable analog/RF design usage.

In DTCO, a critical task is optimizing device geometry and sizing for circuit design while ensuring robust circuit performance across varying operating conditions. Consequently, models must exhibit scalability across device width (W), length (L), and temperature (T), as temperature strongly influences electrical characteristics and circuit behavior. PrimeSim D2D enables users to provide device data at multiple W/L/T points and applies interpolation and extrapolation to construct LUT models over the entire range. For D2D-NN, a global neural network model capturing geometry and temperature dependence is not employed, as such models significantly increase complexity and training time. Instead, we introduce an NN interpolation technique that links local NN models (Fig. 4). There are two ways to do that. We can either generate LUT for each NN model and use LUT interpolations, or we can directly interpolate different NN models and create intermediate models. This enables computation of intermediate models within the W/L/T space and facilitates accurate circuit performance analysis under different temperature conditions without training a complex global model. Fig. 5 demonstrates the scalability of D2D. Our interpolation technique allows accurate prediction for currents even when the relationship is nonlinear, for example I_D vs L. Overall, the D2D-LUT or NN interpolation demonstrates good accuracy across the W/L/T space.

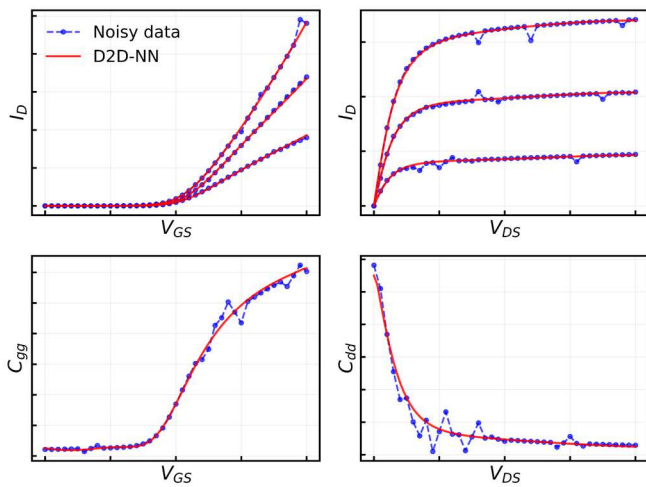


Fig. 3. D2D-NN uses neural network to smooth out the noisy data and provide smooth and continuous models for current and charge/capacitance.

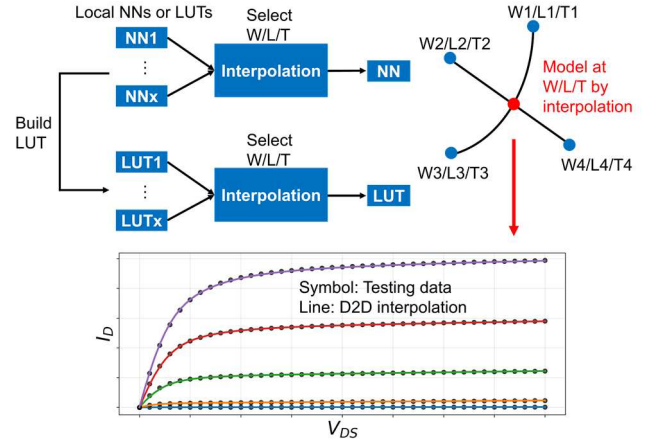


Fig. 4. The flow diagram of creating interpolated models from NNs or LUTs. Local NN or LUT models are created from the data. NN models can directly go through interpolation to create interpolated models for selected W/L/T. They can also be used to generate corresponding LUTs and generate interpolated tables.

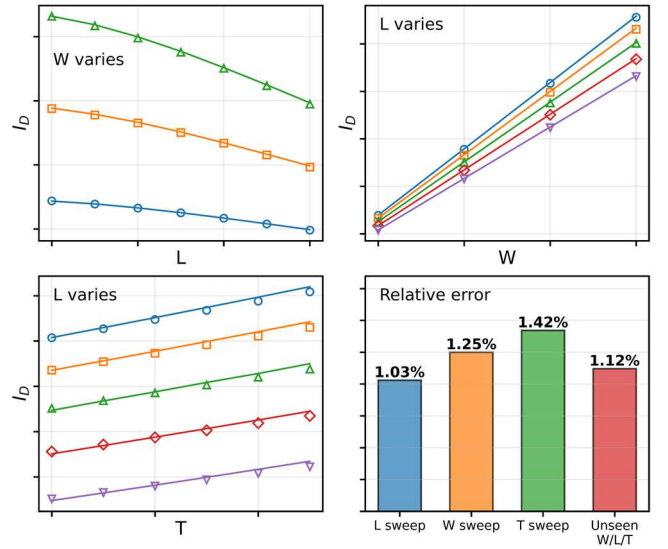


Fig. 5. D2D predicted I_D along various L, W, and T. Different line colors represent different W, L or T as stated in the figure inset. The relative error along L, W, T direction, and all unseen W/L/T combinations in the testing data are about 1%. Symbol: data. Line: D2D.

III. PROCESS VARIATION AND LOCAL LAYOUT EFFECT

In practical chip design, manufacturing-induced process variation (PV) and local layout effects (LLE) are critical to circuit performance. PV and LLE can significantly impact other device properties such as mobility and threshold voltage. These variations must be incorporated into production-level device models to ensure accurate prediction of circuit behavior under real-world conditions. For traditional compact models, PV and LLE are modeled by altering key model parameters, such as V_{TH0} and U_0 in BSIM [9]. D2D employs a perturbation technique and subcircuit approach to model PV and LLE. For a simple MOSFET model as (1) where μ is the effective mobility, V_T is the threshold voltage, and $f()$ is a nonlinear function, a threshold voltage shift can be expressed as an effective V_{GS} offset, and mobility perturbation acts as a scaling factor on I_{DS} . Accordingly, the perturbation technique

modifies the nominal drain current I_{DS0} to account for PV and LLE with (2). Device-specific shifts in μ and V_T are characterized as $dids$ and $dvth$ within the D2D framework [1], [10].

$$I_{DS} \propto \mu f(V_{GS} - V_T) \quad (1)$$

$$I_{DS} = I_{DS0}(V_{GS} - dvth) \times (1 + dids) \quad (2)$$

However, the perturbation approach becomes insufficient when additional physical phenomena, such as contact resistance and short-channel effects (SCE), are considered. D2D employs subcircuit modeling to capture layout-induced parasitic resistance and capacitance. D2D also introduces an equivalent voltage source to account for SCE as an additional gate-voltage offset, shown in Fig. 6. For example, drain-induced barrier lowering (DIBL) can be seen as a shift in the threshold voltage and can be modeled by this extra voltage source. Users can utilize subcircuit element to flexibly define their own variation sources. Fig. 7 demonstrates process corner modeling and the statistical distribution simulated by D2D. By only using $dvth$ and $dids$, D2D can reproduce the variation from PDK models with relatively good accuracy for DTCO. Moreover, because current perturbation is not uniform across all bias regions, D2D introduces a regional $dids$ approach to independently adjust I_{DS} in different operation regions. The total $dids$ and $dvth$ will be the combination of the PV and LLE impacts.

In addition to intrinsic MOSFETs, junctions play a critical role in transistor design, which exhibit geometry dependence distinct from that of the core MOSFET [9]. To address this, D2D provides separate models for junction currents and capacitances. In addition to the LUT or NN models for the intrinsic devices, LUT of NN for junction currents and capacitances can be provided with specific scaling equations to enable accurate junction design considering junction area, sidewall perimeter, and gate edges as shown in Fig. 6.

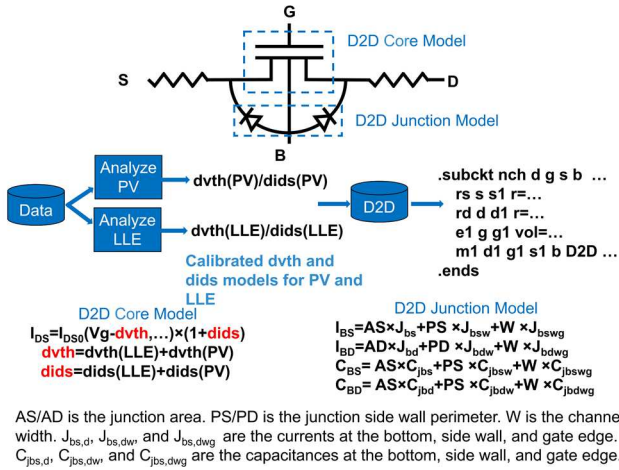


Fig. 6. The schematic diagram of D2D model includes a core transistor model, process variations (PV), local layout effects (LLE), junction diodes, and a subcircuit for contact resistances.

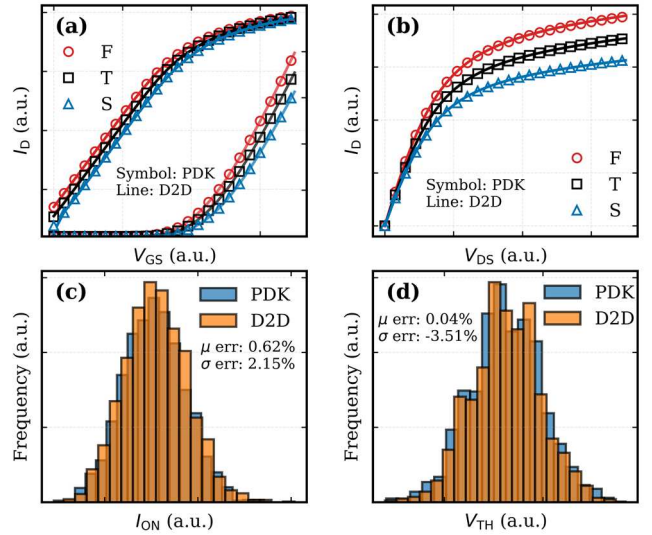


Fig. 7. (a)(b) Fast (F), Typical (T), and Slow (S) corner modeling using D2D. (c)(d) local variation simulations of D2D versus PDK models.

IV. RESULTS AND DISCUSSION

First, we compare the model accuracy and efficiency for PrimeSim D2D using a 17-stage ring oscillator (RO). Fig. 8 shows that both D2D-LUT and D2D-NN can achieve less than 1% error with more than 70% of runtime reduction. When the data contains noise, D2D-NN can produce accurate results while the conventional LUT models will experience convergence difficulty. Then, we validate PrimeSim D2D with post-layout simulations. A post-layout inverter with PDK models is used as a reference. Layout and PV-induced mobility and threshold voltage shift are characterized and fitted with $dids$ and $dvth$. Fig. 9 shows the comparison of the inverter nominal timing simulations from the PDK model and D2D. The model gives accurate results at various slew and load combinations. Fig. 10 demonstrates the statistical timing delay distributions where D2D can accurately reproduce the distributions.

Table I summarizes overall performance. Our work provides faster model generation and faster circuit simulation speed compared to the existing methodologies.

TABLE I. Performance comparison of different compact models.

	BSIM-CMG (level 72)	[5], [6], [8]	D2D-LUT	D2D-NN
Extraction time	Days to weeks	No	No	No
Training time	No	>1hr (global)	No	~10min (local)
Code	C/C++	Verilog-A	C/C++	C/C++
Scaling	Global + binning	Global Training	Local + Interp.	Local + Interp.
PV and LLE	Yes	Partial	$dids$ $dvth$ subckt	$dids$ $dvth$ subckt
Noise-resilient	Manual fitting	Not shown	By NN-created LUT	Auto
Simulation speed	1×	1.5×	3.8×	2.7×

* Interp. = interpolation, subckt=subcircuit

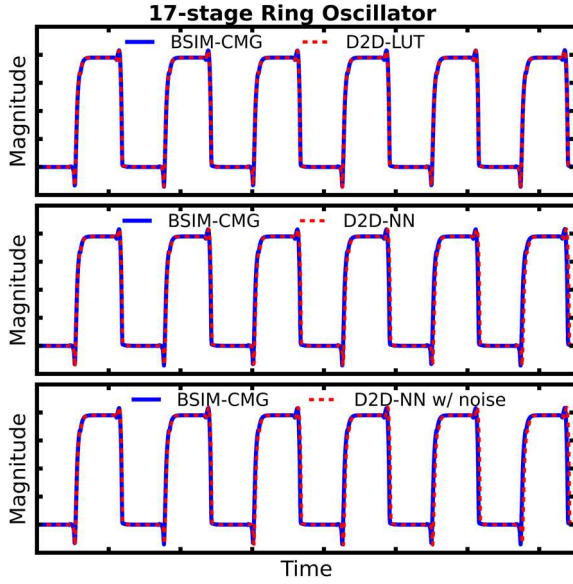


Fig. 8. 17-stage ring oscillator simulation using BSIM-CMG and D2D. D2D-NN can smooth the model to achieve robust simulation while normal LUT will face convergence issue.

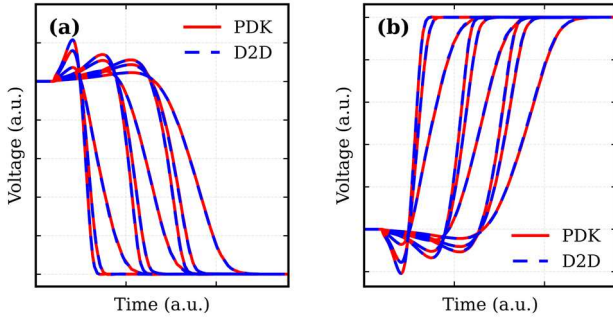


Fig. 9. A post-layout inverter characterization under various load and slew combinations simulated by PDK and D2D models. Perturbations are used to model μ and V_T shifts caused by layouts. (a) high to low. (b) low to high.

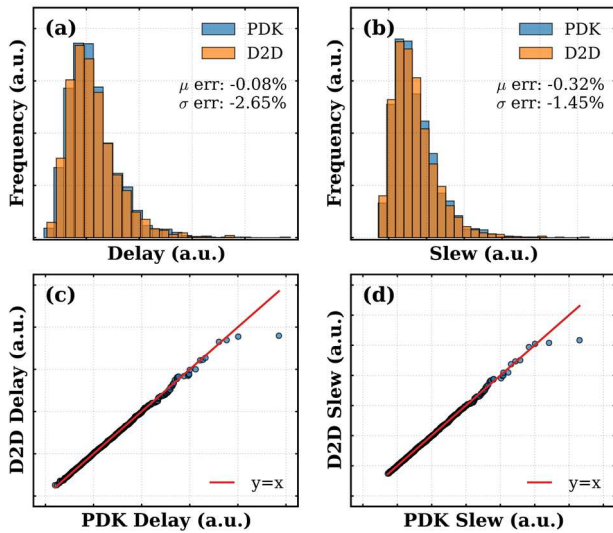


Fig. 10. Statistical delay and slew of a post-layout inverter simulated by PDK and D2D models.

V. CONCLUSION

We present PrimeSim D2D, a machine-learning assisted data-to-design modeling framework. D2D incorporates both LUT and NN models to generate accurate and efficient SPICE device models. By eliminating time-consuming model extraction and leveraging fast, SPICE-compatible device models, PrimeSim D2D significantly reduces turnaround time (TAT), enabling rapid design iterations within DTCO workflows.

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