

Joule heating and thermal transport in 2D materials for device applications

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Abstract—Heat dissipation and thermal management is a rising concern for nanoelectronic devices and threatens to curtail their adoption in integrated circuits, sensors, and energy converters. Joule heating due to dissipation in the channel region of nanoelectronic devices causes increased temperature and may lead to mobility degradation and long-term reliability issues. Here we study thermal transport and cross-plane thermal boundary conductance in a variety of “beyond graphene” 2D materials and few-layer stacks on several amorphous and crystalline substrates using a combination of first principles methods and Boltzmann transport of phonons. We employ machine learning to accelerate the discovery of 2D-substrate pairings with enhanced thermal conductance. Beyond that, we couple electronic and thermal transport to study dissipation in field effect MOS transistors and show that heat dissipation is non-uniform and that self-heating reduces mobility. We find that judicious selection of the number of layers and substrate can significantly reduce the deleterious effects of Joule heating.

Keywords—phonons, Joule heating, 2D materials

I. INTRODUCTION

The persistent down-scaling of nanostructures, such as electronic devices, sensors, NEMS, and nanocomposites, increases the surface-to-volume ratio and introduces atomic-scale disorder at boundaries and interfaces. To avoid these issues, the nanoelectronics community has turned to intrinsically two-dimensional (2D) materials platforms. 2D materials have tremendous potential for next-generation nanoelectronics due to their atomic flatness and absence of dangling bonds, which prevents scattering from interface roughness. However, heat dissipation and its removal from hot spots in the monolayer remains a critical concern to the design of 2D-based devices [1]. Thermal currents flowing in an atomic layer can either dissipate through source/drain contacts in a transistor configuration, or through a supporting substrate via van der Waals (vdW) coupling to it. When a 2D material is supported by a substrate, the interfacial area formed between it and the substrate is often far larger than the lateral source/drain contact area. Thus, the majority of waste heat is removed across the 2D-substrate interface and then via the substrate.

The thermal boundary conductance (TBC) between the 2D layer and substrate should be well characterized for reliable 2D device performance. Interfaces formed between 2D vdW materials and 3D substrates are fundamentally different than same-dimension 3D-3D and 2D-2D interfaces due to the presence of a vdW gap and the different dimensionalities of the phase spaces on either side of the interface. In this work,

we further develop the understanding of lattice thermal transport, both in-plane and cross-plane, in 2D mono and few-layer materials from first principles and apply those insights to better understand semiconductor devices that have 2D materials as channels.

Our work builds on vibrational properties of the 2D materials calculated from Density Functional Theory combined with Boltzmann transport equation for phonons. Our recent work aims to tackle the question of selecting the best substrate for each 2D material from the point of view of heat dissipation and apply these results to 2D devices. We deployed machine learning (ML) to quantify the sensitivity of the thermal boundary conductance (TBC) to each of the properties of 2D materials and substrates in order to identify which properties have the most impact on the TBC. We also coupled our thermal transport model to a few-layer (FL) electronic transport model, which is based on a coupled Schrödinger-Poisson solver in the cross-plane direction, to achieve a more complete electro-thermal simulation of FL 2D devices. We conclude that electronic properties cannot be accurately analyzed separately from the thermal as Joule heating causes increased resistance, particularly in FL stacks where the temperature is layer dependent.

II. METHODS

Both electronic and thermal properties of 2D materials have drawn intense scrutiny from both the experimental and simulation sides. Several papers measured the TBC between various monolayers and 3D substrates, with the silicon dioxide (SiO₂) substrate being the most commonly studied, reporting a wide range of values, which was attributed to various processing conditions and inconsistent sample quality. Therefore, it is imperative to build predictive methods for quantifying the TBC between 2D MLs or FLs and various substrates. Here, we report on our progress in developing and using a model based on the combination of phonon dispersions from first-principles density functional perturbation theory simulations and a 2D-3D interface thermal transport model [2, 3]. The model, described in more detail in our previous publications, computes the TBC for 2D/3D interface from a Landauer-like formula

$$G_{2D}(T) = \int C(\omega, T) D_{2D}(\omega) \Gamma_{3D}(\omega) d\omega \quad (1)$$

where $D_{2D}(\omega)$ is the vDOS of the 2D material, $C(\omega, T)$ is the modal heat capacity, and $\Gamma_{3D}(\omega)$ is the interface phonon transfer rate due to the coupling between flexural phonons in the 2D material and phonons in the 3D material. This rate

involves the van der Waals (vdW) coupling spring constant K_a between the 2D layer and 3D material and is defined as

$$\Gamma_{3D}(\omega) = \frac{\pi D_{3D}(\omega) K_a^2}{2 m_{3D} m_{2D} \omega^2} \quad (2)$$

where m_{3D} and m_{2D} are the masses of 3D and 2D atoms in contact at the interface, D_{3D} is the vDOS of the 3D material, and ω is the vibrational frequency of the phonons. Combining equations 1 and 2, we see that the TBC is related to the product of the vDOSes, amplified at low frequencies by the $1/\omega^2$ resonant term in the denominator of equation (2). First-principles density-functional perturbation theory (DFPT), as implemented in open-source Quantum Espresso [9], has been used to determine phonon dispersions, which are used to calculate the phonon group velocities $\vec{v}(q) = \nabla_q \omega(q)$ and phonon density of states as described in Ref. [8].

To further probe the role of interfacial phonon transport, we developed a coupled electro-thermal model for FL-WSe₂ stacks (Fig. 1a) where we simultaneously solve for the current and Joule heating by treating the stack as a resistor network (Fig. 1b). The source and drain contacts are connected to the topmost layer, with the substrate and gate below the

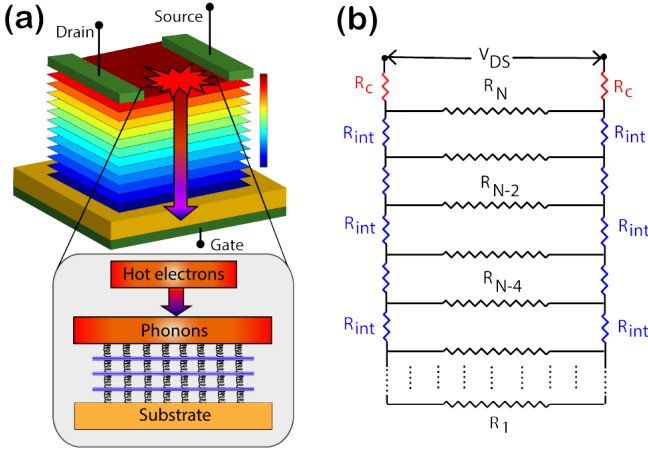


Figure 1. Schematic of a 2D few-layer device (a) and a resistor network representing the interlayer and layer resistances in a few-layer stack of 2D layers.

bottommost layer. Each layer has a different resistance, voltage, and current flowing through it. The current encounters additional resistance in the form of interlayer resistance, as well as the contact resistance above the topmost layer. To combine conductivities of individual layers into the electrical conductivity of few-layer 2D devices, we start from a resistor network model published in our prior work [6]. We combine it with a self-consistent Schrödinger–Poisson (SCSP) solver for the electron wavefunctions to obtain the carrier density in the through-plane direction, from which we compute layer-wise conductivity, current, and heat dissipation. To compute temperature resulting from the Joule heating, we add the thermal model described in the first part of this section and use it to quantify the heat transfer to the substrate.

III. RESULTS

Next, we employ our first-principles model to calculate the TBC of several beyond-graphene 2D materials, such as

silicene, germanene, stanene, BAs, GaAs, InAs, and blue and black phosphorene, on amorphous and crystalline substrates. A trend emerges that 2D materials with lower ZA branch frequencies have higher TBCs when placed on a-SiO₂ because of the better matching between the flexural (out-of-plane) ZA phonons and the low-frequency peak in the vibrational spectrum of amorphous materials. This is particularly evident in 2D boron arsenide (BAs), which we identify to have the highest TBC on amorphous substrates like SiO₂. On crystalline substrates, the TBC drops due to the mismatch in vibrational modes of soft flexural phonons and stiff acoustic phonons in the substrate, with hBN emerging as having the highest TBC of all the materials we studied. Our results provide selection criteria for 2D materials that improve interfacial heat transport in 2D devices with amorphous and crystalline substrates.

The resulting rise in temperature is obtained from a FL-TBC model [4] to shed light on self-heating and heat dissipation in such devices. We find that the temperature rise in the top layers is significantly larger than the bottom layers (Fig. 3e) because the bottom layers have higher TBC and conduct heat more efficiently to the substrate (Fig. 3d) [4,5]. The higher temperature of top layers, in turn, significantly reduces their mobility, which is strongly temperature dependent as they are shielded by the bottom layers from substrate impurity scattering. We also uncover that, unlike monolayer FETs, a significant amount of heat is dissipated laterally through the contacts in FL devices at high source-drain voltages due to relatively long thermal healing lengths of the top layers, especially in short-channel devices.

IV. CONCLUSIONS

We have studied thermal boundary conductance between a variety of 2D materials and 3D substrates. We find that amorphous SiO₂ is consistently the substrate with the highest TBC due to the high density of low-frequency vibrational modes that transfer heat efficiently across the van der Waals interface. We also find that 2D sheets with ample low-lying flexural modes, such as hBN, have high TBC and identify new materials such as 2D boron arsenide (BAs) as a potential new high thermal conductance insulating layer. Further, our electro-thermal model shows that self-heating in few-layer 2D MOS transistors impacts their performance through increased interlayer thermal resistance experienced by the layers near the top of the stack. In the absence of self-heating, the top layers have the lowest electrical contact resistance and thus carry the most heat but that picture evolves with self-heating as the layers near the top of the stack heat up and become more resistive. This causes current to re-route through the layers lower in the stack, that have experienced less self-heating as they have higher TBC due to their proximity to the substrate.

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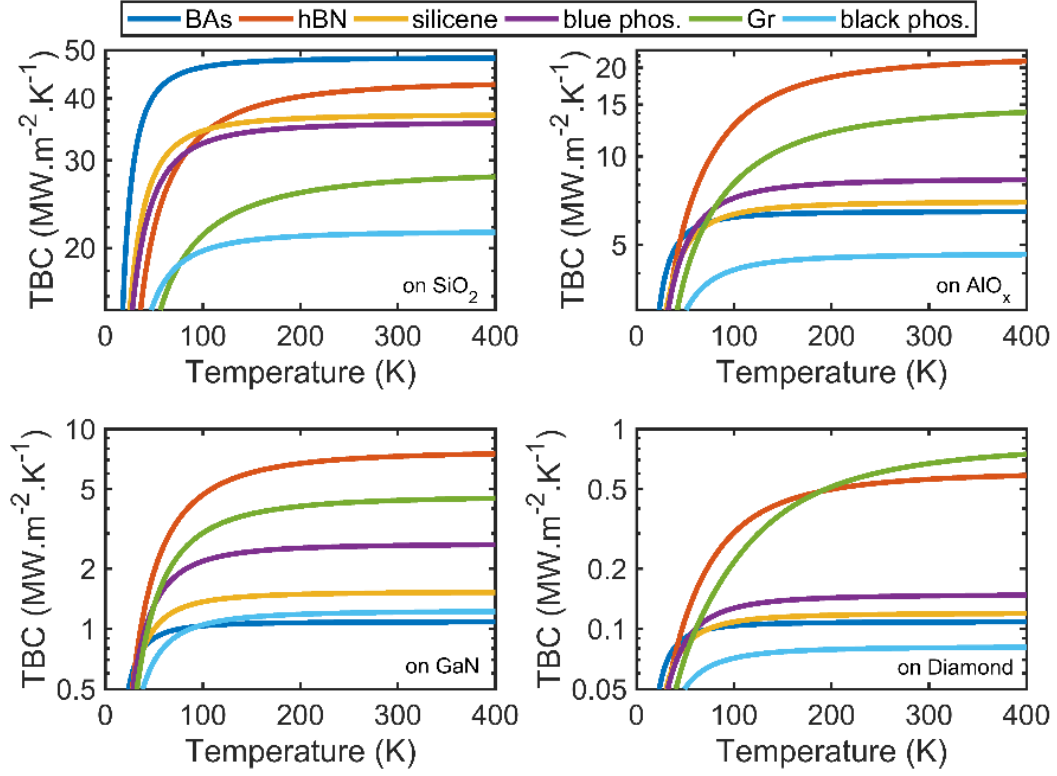


Figure 2. Thermal boundary conductance of “beyond-graphene” 2D materials on various substrates, including SiO₂ (top left), AlO_x (top right), GaN (bottom left), and diamond (bottom right), showing hBN has among the highest thermal conductance values across all temperatures and most substrates. Boron arsenide 2D sheets (BAs) also show high thermal conductance on amorphous SiO₂.

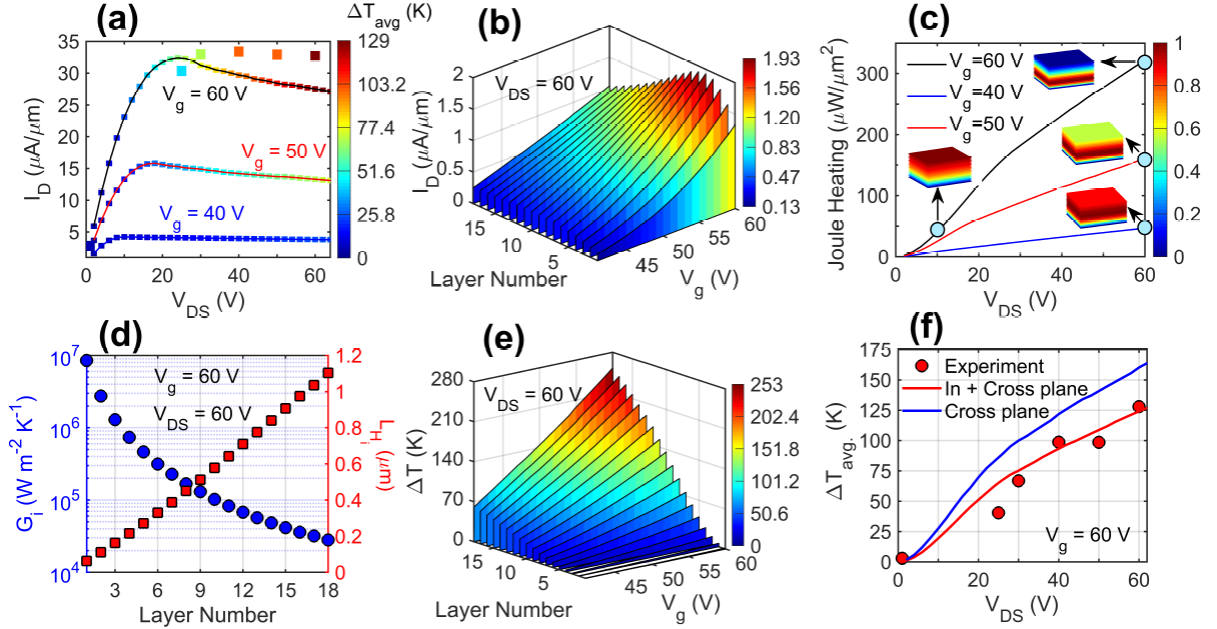


Figure 3 (below). Calculated I-V characteristics of a 13 layer WSe₂ device (a), layer-resolved current (b) and Joule heating as a function of drain voltage (c). The TBC is layer-dependent and layers furthest from the substrate have the most thermal resistance (d), resulting in layer-dependent temperature rise (e) and self-heating (f).

