

Modeling Counterclockwise Current Hysteresis in Oxide Thin-Film Transistors

Pranay Baikadi*, Benius Dunn*, Javier Meza-Arroyo*, Sara Ghazvini*, Julia W. P. Hsu*,
and William G. H. Vandenberghe*

*Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080 USA

Abstract—Hysteresis in oxide thin-film transistors (TFTs) is a desirable characteristic for neuromorphic computing, where history-dependent device behavior can emulate synaptic plasticity. In this work, a one-dimensional transient Poisson–Drift–Diffusion (PDD) solver is developed to model mobile oxygen vacancy redistribution within the gate dielectric of an oxide TFT under a triangular voltage sweep with different sweep rates. Parametric studies reveal that the hysteresis window increases with decreasing vacancy mobility and increasing vacancy concentration. The model shows good agreement with experimental transfer characteristics across multiple sweep speeds, providing a predictive framework for engineering hysteresis in oxide TFTs for neuromorphic applications.

Index Terms—TFT, hysteresis, vacancies, drift-diffusion, neuromorphic computing

I. INTRODUCTION

Oxide thin-film transistors (TFTs) have emerged as promising candidates for neuromorphic computing applications due to their ability to exhibit tunable hysteresis in their transfer characteristics [1]. This hysteresis, manifested as a history-dependent shift in threshold voltage, can mimic synaptic plasticity [2], [3], making it an attractive primitive for hardware implementations of brain-inspired information processing architectures such as physical reservoir computing (PRC). In PRC, a physical system with fading memory and nonlinear dynamics processes temporal inputs without requiring weight updates during training [4]. The tunable hysteresis of oxide TFTs makes them natural reservoir nodes, but exploiting this requires control over the hysteresis window and a predictive understanding of the physical parameters that set it.

In oxide TFTs, the counterclockwise (CCW) hysteresis has been attributed to the field-driven drift and diffusion of mobile charges, such as oxygen vacancies, within the gate dielectric [5], [6], as illustrated in Fig. 1. Yet this picture has largely been invoked qualitatively, and the quantitative dependence of the hysteresis window on material parameters, such as the vacancy mobility and density, and on the gate sweep rate has not been systematically established.

In this work, we develop a one-dimensional (1D) transient Poisson–drift–diffusion (PDD) solver that self-consistently couples the gate-oxide electrostatics to the drift and diffusion of mobile oxygen vacancies. Using this solver, we systematically examine how the hysteresis window depends on the vacancy mobility, the vacancy density, and the gate sweep rate

This work was supported by the Air Force Office of Scientific Research under award number FA2386-24-1-4041.

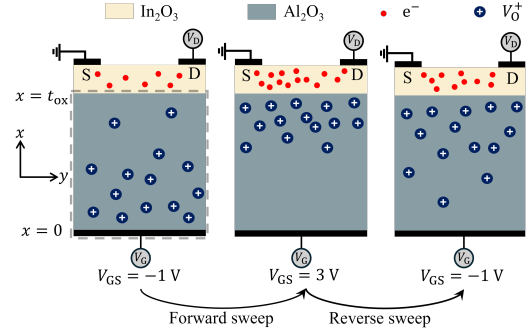


Fig. 1. Schematic illustration of vacancy migration through the dielectric under a triangular voltage sweep. The simulation domain consists of 1D cutlines through the gate dielectric (dotted gray rectangle), taken only at the $y = 0$ (S) and $y = L_{ch}$ (D).

(SR) in a In_2O_3 TFT with a Al_2O_3 gate dielectric, and validate the model against measured transfer characteristics.

II. METHODOLOGY

Fig. 1 shows a simulation schematic of the TFT investigated in this work, comprising an In_2O_3 channel, an Al_2O_3 gate dielectric, and aluminum (Al) as the gate metal. The simulation domain is a vertical cutline through the region bounded by the dashed gray rectangle, with the gate metal and the dielectric–channel interface forming the two boundaries of the 1D mesh. Electron and vacancy transport are assumed to occur predominantly along the horizontal (y) and vertical (x) directions, respectively. The gate dielectric is assumed to contain mobile oxygen vacancies with charge number $+1$ (V_O^+), whose total number is fixed at fabrication. The In_2O_3 channel is assumed to be n -type with negligible hole density and vacancy mobility. Interfaces between materials are taken to be ideal, with no interface traps or fixed charges. Furthermore, the gate dielectric boundaries are assumed to be perfectly blocking, preventing any carrier flux crossing between the dielectric and the channel or between the gate electrode and the dielectric.

A. The Poisson equation

Electrostatics in the gate dielectric are governed by the 1D Poisson equation

$$\frac{\partial^2 \psi(x, t)}{\partial x^2} = -\frac{z q_e}{\epsilon_{ox}} n_{v_o}(x, t), \quad (1)$$

where z is the (signed) vacancy charge number, q_e the elementary charge, ϵ_{ox} the dielectric permittivity, n_{v_o} the vacancy

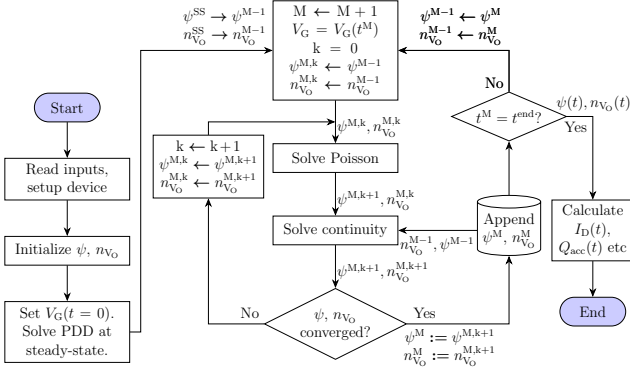


Fig. 2. Flowchart of our 1D transient PDD solver. Indices M and 'k' label the time level and the inner self-consistent iteration number respectively.

density, and ψ the potential. A finite-difference discretization at interior node i and time level M gives

$$\frac{2}{h_i + h_{i-1}} \left[\frac{\psi_{i+1}^M - \psi_i^M}{h_i} - \frac{\psi_i^M - \psi_{i-1}^M}{h_{i-1}} \right] = -\frac{zq_e}{\epsilon_{ox}} n_i^M. \quad (2)$$

At the metal–dielectric interface ($i = 0$), the potential is set through a piecewise Dirichlet condition,

$$\psi_0^M = \begin{cases} V_G - \phi_{ms} & \text{at the source,} \\ V_G - V_D - \phi_{ms} & \text{at the drain,} \end{cases} \quad (3)$$

where V_D is the drain bias and ϕ_{ms} is the metal–semiconductor workfunction difference. At the dielectric–channel interface ($i = N - 1$), the boundary condition is imposed in terms of the surface electric field and evaluated using the ghost-point method (assuming $h_{N-1} = h_{N-2}$), yielding

$$\frac{2}{h_{N-2}^2} (\psi_{N-2}^M - \psi_{N-1}^M) + \frac{2Q_s(\psi_{N-1}^M)}{\epsilon_{ox} h_{N-2}} = -\frac{zq_e}{\epsilon_{ox}} n_{N-1}^M, \quad (4)$$

where ψ_{N-1}^M is the surface potential ψ_s and Q_s is the semiconductor space-charge density. For an n -type channel material like In_2O_3 , Q_s is given by

$$Q_s(\psi_s) = -\text{sign}(\psi_s) Q_{s0} \sqrt{\exp(\psi_s/V_T) - \psi_s/V_T - 1}, \quad (5)$$

where $Q_{s0} = \sqrt{2q_e \epsilon_s N_D V_T}$, V_T is the thermal voltage, ϵ_s the channel permittivity, and N_D the doping level.

B. The continuity equation

Vacancy transport inside the gate dielectric is described in the drift–diffusion formalism, with the current density

$$J_{v_o} = -z^2 q_e n_{v_o} \mu_{v_o} \frac{\partial \psi}{\partial x} - zq_e D_{v_o} \frac{\partial n_{v_o}}{\partial x}, \quad (6)$$

where μ_{v_o} the low-field drift mobility per unit charge number, and D_{v_o} the diffusion coefficient. The 1D continuity equation

$$\frac{\partial n_{v_o}(x, t)}{\partial t} = -\frac{1}{zq_e} \frac{\partial J_{v_o}(x, t)}{\partial x}, \quad (7)$$

is discretized in space using the Scharfetter–Gummel (SG) scheme and in time using a backward-Euler step. At an interior node i and time level M this gives

$$-n_i^{M-1} = D_i n_i^M + U_i n_{i+1}^M + L_i n_{i-1}^M, \quad (8)$$

where the coefficients D_i , U_i , and L_i are given by

$$D_i = -\lambda_i \left[\frac{\mathcal{B}(\text{Pe}_{i+\frac{1}{2}})}{h_i} + \frac{\mathcal{B}(-\text{Pe}_{i-\frac{1}{2}})}{h_{i-1}} \right] - 1, \quad (9)$$

$$U_i = \lambda_i \left[\frac{\mathcal{B}(-\text{Pe}_{i+\frac{1}{2}})}{h_i} \right], L_i = \lambda_i \left[\frac{\mathcal{B}(\text{Pe}_{i-\frac{1}{2}})}{h_{i-1}} \right],$$

$\lambda_i = (2D_{v_o} \Delta_t^{M-1}) / (h_i + h_{i-1})$, $\mathcal{B}(x) = x / (e^x - 1)$ is the Bernoulli function, and $\text{Pe}_{i+\frac{1}{2}} = z(\psi_{i+1} - \psi_i) / V_T$ is the local Péclet number over $[x_i, x_{i+1}]$. To ensure charge conservation in the gate dielectric, we apply blocking boundary conditions $J_0 = J_{N-1} = 0$ at the boundary nodes $i = 0$ and $i = N - 1$.

C. Self-consistency

The flowchart of our simulation is shown in Fig. 2. The solver begins by reading the inputs such as the material constants, V_G profile, and initializing the potential ψ and vacancy density n_{v_o} . The gate bias V_G is then set to its $t = 0$ value and the coupled Poisson–continuity equations are solved at steady-state to establish the initial condition. This steady-state solution (ψ^{SS} , $n_{v_o}^{SS}$) then seeds the transient march.

At each time step, the Poisson–continuity system is solved by Gummel iteration, which decouples the two equations and solves them alternately, each with the other held fixed, until they are mutually self-consistent. Starting from the solution at the previous time level, the Poisson equation is solved for the $\psi^{M,k}$ using the vacancy density $n_{v_o}^{M,k-1}$, and the potential $\psi^{M,k}$ is then used to solve the continuity equation for the new density $n_{v_o}^{M,k}$. This inner loop repeats until the change in ψ and n_{v_o} between successive iterations falls below a prescribed tolerance. Each converged state is stored, and the march continues to the final time.

D. I_{DS} calculation

To calculate I_{DS} , we first perform the 1D PDD solves at the source and drain ends separately. Using the converged solution at the time level M at each end, the charge-sheet approximation is used to calculate the corresponding depletion charge densities as,

$$Q_{\text{dep},S/D}^M = \begin{cases} \sqrt{2\epsilon_s q_e (-\psi_{s,S/D}^M) N_D}, & \psi_{s,S/D}^M \leq 0, \\ 0, & \psi_{s,S/D}^M > 0, \end{cases} \quad (10)$$

where $\psi_{s,S/D}^M$ is the surface potential at the source/drain end. The accumulation charge follows as

$$Q_{\text{acc},S/D}^M = Q_{s,S/D}^M - Q_{\text{dep},S/D}^M, \quad (11)$$

where $Q_{s,S/D}^M$ is the total space-charge density given by Eq. (5). Lastly, the gradual channel approximation is invoked to calculate the drain current I_{DS}^M as

$$I_{DS}^M = \mu_{el} \frac{W}{L} \left(\frac{Q_{\text{acc},S}^M + Q_{\text{acc},D}^M}{2} \right) V_D, \quad (12)$$

where μ_{el} is the electron mobility and W, L are the channel width and length respectively.

TABLE I
DEVICE AND MATERIAL PARAMETERS

Parameter	Value	Units
Channel width (W)	500	μm
Channel length (L)	100	μm
Channel thickness (t_{ch})	30	nm
Doping (N_D)	10^{19}	cm^{-3}
Electron mobility (μ_{el})	2.6	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$
In_2O_3 permittivity (ϵ_s)	9.0	—
In_2O_3 band gap (E_g)	2.7	eV
In_2O_3 affinity (χ)	3.5	eV
In_2O_3 effective DOS (N_c)	10^{18}	cm^{-3}
Al_2O_3 thickness (t_{ox})	70	nm
Al_2O_3 permittivity (ϵ_{ox})	9.0	—
Gate work function (ϕ_m)	4.3	eV
Drain-source bias (V_D)	0.5	V

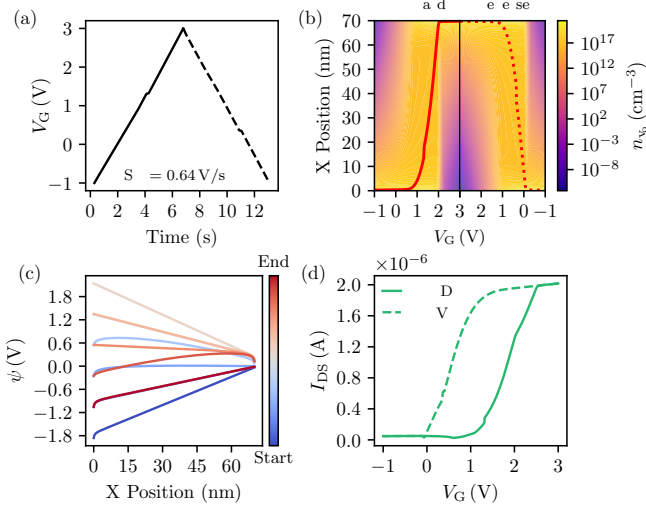


Fig. 3. (a) Triangular gate voltage waveform. (b) Evolution of n_{vo} across Al_2O_3 , with $\bar{x}_{\text{vo}}$ in red. (c) Evolution of ψ . (d) Simulated TFT transfer characteristics.

III. RESULTS AND DISCUSSION

In this section, the PDD solver is used to first explain the mechanism behind CCW hysteresis observed in our TFT devices. We then systematically investigate the effect of gate voltage sweep rate (SR), vacancy mobility μ_{vo} and density N_{vo} on hysteresis width. A complete list of parameters held fixed in all our simulations are tabulated in Table. I.

A. Origin of counterclockwise hysteresis

To understand the origin of CCW hysteresis, a symmetric triangular voltage waveform shown in Fig. 3(a) is applied to the gate, with V_G ramping from -1 V to 3 V and back with a sweep rate of 0.64 V/s. The density is consistent with reported defect densities in a- Al_2O_3 [7] and μ_{vo} is within the range of experimentally observed ionic transport in thin-film oxides [8].

Fig. 3(b) shows the spatiotemporal evolution of n_{vo} across the dielectric thickness, with the vacancy centroid $\bar{x}_{\text{vo}}$ overlaid (solid: forward sweep; dotted: reverse). At the beginning of the forward sweep, most of the vacancies are located near the gate-dielectric interface. As V_G increases, the positively charged oxygen vacancies migrate from the gate-dielectric in-

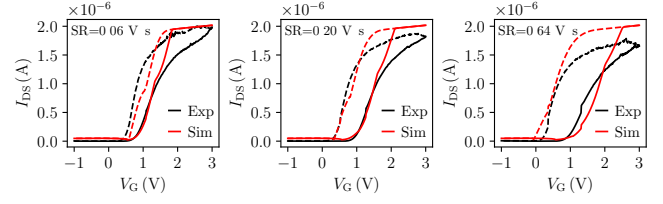


Fig. 4. Effect of SR ($= \frac{dV_G}{dt}$) on hysteresis width.

terface (~ 0 nm) toward the dielectric-channel interface (~ 70 nm). On the reverse sweep, however, the centroid retraces its path only after a pronounced delay due to the low μ_{vo} . Thus, the ionic redistribution cannot follow the gate sweep instantaneously, so the vacancy configuration at a given V_G depends on the sweep history and rate.

Fig. 3(c) shows the electrostatic potential ψ across the gate dielectric at successive instants of the gate sweep, colored from the start (blue) to the end (red) of the triangular waveform in Fig. 3(a). In the forward sweep, the positive bias repels the vacancies away from the gate-dielectric interface and the internal field drives them towards the dielectric-channel interface, where they accumulate. Due to the low μ_{vo} , we see that the field in the reverse sweep for a given V_G is not the same as during the forward sweep.

Lastly, Fig. 3(d) plots the resulting simulated transfer characteristics for the forward (solid) and reverse (dashed) sweeps. The reverse sweep turns on at a lower gate voltage than the forward sweep, so that for a given V_G the reverse-sweep current exceeds the forward-sweep value over most of the subthreshold and turn-on region. Equivalently, the threshold voltage is lower on the reverse sweep, and the loop is traced in a CCW sense. This shift between the two branches is a direct consequence of the history-dependent vacancy distribution established in Fig. 3(b) and (c).

B. Effect of sweep rate

In this section, we study the impact of the sweep rate (SR) of the triangular voltage waveform on the hysteresis width. Here, V_D is fixed at 0.5 V and SR is varied by an order of magnitude from 0.06 V s^{-1} to 0.64 V s^{-1} , while N_{vo} and μ_{vo} are the same as in section III-A. Fig. 4 compares the measured (black) and simulated (red) transfer characteristics at the three sweep rates, with the forward (solid) and reverse (dashed) branches shown for each. In both experiment and simulation, the hysteresis width increases with SR.

This trend can be explained by the finite time required for the oxygen vacancies to redistribute under the gate field. At the lowest sweep rate, the gate voltage changes slowly enough that the vacancies can closely follow it, so their configuration at a given V_G is nearly the same on the forward and reverse sweeps. As the sweep rate increases, the gate voltage changes faster than the vacancies can respond, so their configuration lags the applied bias and differs between the forward and reverse sweeps. This history-dependent vacancy distribution shifts the threshold voltage between the two branches, and the resulting separation grows with increasing SR.

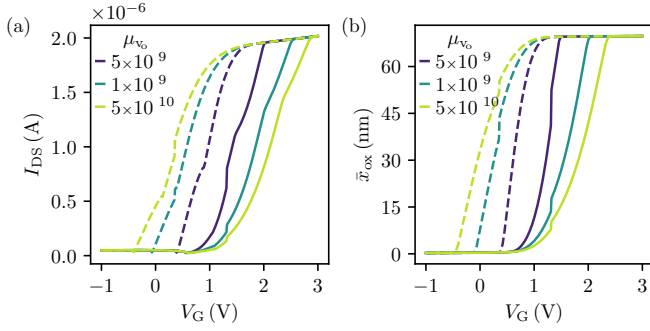


Fig. 5. Effect of μ_{v_o} (in $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$) on hysteresis width for a triangular gate sweep at 0.64 V/s . (b) Corresponding centroid trajectories.

C. Effect of μ_{v_o}

Fig. 5(a) shows the transfer characteristics for the three values of μ_{v_o} (with $N_{v_o} = 3.4 \times 10^{18} \text{ cm}^{-3}$), with the forward (solid) and reverse (dashed) sweeps shown for each. In every case the reverse branch turns on at a lower gate voltage than the forward branch, producing a CCW loop, but the separation between the two branches grows as μ_{v_o} is reduced, with the lowest and the highest μ_{v_o} yielding the widest and the narrowest hysteresis loops, respectively. Thus the hysteresis width increases monotonically with decreasing μ_{v_o} .

This trend is explained by the centroid loops in Fig. 5(b). Like the current, the centroid traces a forward–reverse loop whose width reflects how much the vacancy distribution at a given V_G differs between the two sweeps. As μ_{v_o} is reduced, the vacancies respond more slowly to the changing V_G and lag further behind, widening this loop just as in Fig. 5(a).

D. Effect of N_{v_o}

Fig. 6(a) shows the transfer characteristics for the three values of N_{v_o} (with $\mu_{v_o} = 10^{-9} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$). As expected, a higher N_{v_o} raises the overall channel conductance, increasing the on-current. In every case the reverse branch turns on at a lower gate voltage than the forward branch, producing a CCW loop. Interestingly, we see that the branch separation increases as N_{v_o} is increased, so that the highest and lowest densities yield the widest and narrowest hysteresis loops, respectively.

Unlike the case of μ_{v_o} , this trend does not arise from a difference in timing, as the centroid trajectories in Fig. 6(b) depend only weakly on N_{v_o} . The dominant effect is instead electrostatic, where at higher N_{v_o} , the same redistribution displaces more charge, producing a larger shift in the potential and hence in the threshold voltage. The hysteresis width is therefore set not only by the timing of the redistribution (μ_{v_o}) but also by the magnitude of the displaced charge (N_{v_o}).

IV. CONCLUSIONS

A transient Poisson–drift–diffusion solver was developed to investigate the mechanism behind CCW hysteresis in $\text{In}_2\text{O}_3\text{--Al}_2\text{O}_3$ TFTs. The Poisson equation was discretized using finite-differences and the continuity equation using the Scharfetter–Gummel scheme. The Gummel iterative method and backward-Euler time-stepping were used to achieve self-consistency at each time step.

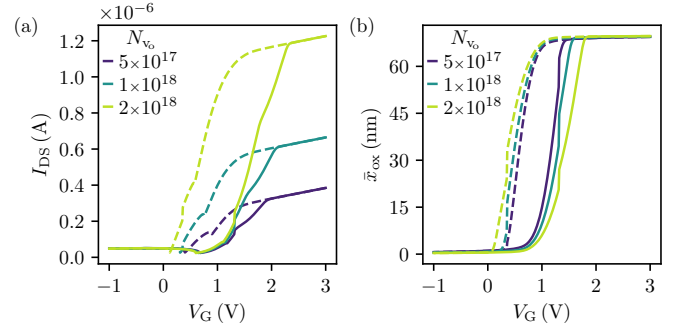


Fig. 6. (a) Effect of N_{v_o} (in cm^{-3}) on hysteresis width for a triangular gate sweep at 0.64 V/s . (b) Corresponding centroid trajectories.

Using the solver, we investigated the effect of sweep rate, μ_{v_o} and N_{v_o} on the hysteresis width of the transfer characteristics. We found that the width increases with sweep rate, as the faster V_G ramp outpaces the vacancy redistribution and drives the forward and reverse branch configurations further apart. A lower μ_{v_o} produces the same effect by slowing the redistribution, so that the vacancies lag further behind the applied bias. Lastly, a higher N_{v_o} also widens the loop, by increasing the amount of displaced charge and hence the shift in threshold voltage between the two sweeps.

ACKNOWLEDGMENT

We acknowledge the Texas Advanced Computing Center at The University of Texas at Austin for providing high performance computing resources. We would like to express our special thanks to Prof. Jen-Sue Chen at NCKU, Taiwan for the many helpful discussions during the course of this work.

REFERENCES

- [1] L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi, and Q. Wan, “Artificial synapse network on inorganic proton conductor for neuromorphic systems,” *Nature communications*, vol. 5, no. 1, p. 3158, 2014.
- [2] R. Chen, H. Yang, R. Li, G. Yu, Y. Zhang, J. Dong, D. Han, Z. Zhou, P. Huang, L. Liu *et al.*, “Thin-film transistor for temporal self-adaptive reservoir computing with closed-loop architecture,” *Science Advances*, vol. 10, no. 7, p. ead11299, 2024.
- [3] T. Lim, S. Lee, J. Lee, H. Choi, B. Jung, S. Baek, and J. Jang, “Artificial synapse based on oxygen vacancy migration in ferroelectric-like c-axis-aligned crystalline ingasno semiconductor thin-film transistors for highly integrated neuromorphic electronics,” *Advanced Functional Materials*, vol. 33, no. 8, p. 2212367, 2023.
- [4] J. Meza-Arroyo, B. Dunn, W. Xu, Y.-C. Chen, J.-S. Chen, and J. W. P. Hsu, “Bayesian optimization of multi-bit pulse encoding in $\text{In}_2\text{O}_3\text{--Al}_2\text{O}_3$ thin-film transistors for temporal data processing,” *npj Unconventional Computing*, vol. 3, no. 1, p. 6, 2026.
- [5] Z. Ye, Y. Yuan, H. Xu, Y. Liu, J. Luo, and M. Wong, “Mechanism and origin of hysteresis in oxide thin-film transistor and its application on 3-d nonvolatile memory,” *IEEE Transactions on Electron Devices*, vol. 64, no. 2, pp. 438–446, 2017.
- [6] K.-T. Chen, L.-C. Shih, S.-C. Mao, and J.-S. Chen, “Mimicking pain-perceptual sensitization and pattern recognition based on capacitance-and conductance-regulated neuroplasticity in neural network,” *ACS Applied Materials & Interfaces*, vol. 15, no. 7, pp. 9593–9603, 2023.
- [7] R. Nakamura, T. Toda, S. Tsukui, M. Tane, M. Ishimaru, T. Suzuki, and H. Nakajima, “Diffusion of oxygen in amorphous al_2o_3 , ta_2o_5 , and nb_2o_5 ,” *Journal of applied Physics*, vol. 116, no. 3, 2014.
- [8] S. Zafar, H. Jagannathan, L. F. Edge, and D. Gupta, “Oxygen vacancy mobility and diffusion coefficient determined from current measurements in $\text{tio}_2/\text{hfo}_2/\text{tin}$ stacks,” in *Proceedings of the International Conference on Solid State Devices and Materials*, vol. 669, 2010.