

# Enabling 4F<sup>2</sup> DRAM Junctionless Vertical Channel Transistors with Novel Oxygen Inserted Si Substrates – A TCAD Study

Albert Lu  
Atomera Inc.  
Los Gatos, CA, USA  
alu@atomera.com

Madhav Raj  
San Jose State University  
San Jose, CA, USA  
madhav.raj@sjsu.edu

Hui Yung Wong  
San Jose State University  
San Jose, CA, USA  
hiuyung.wong@sjsu.edu

Ilya Rumyantsev  
Atomera Inc.  
Los Gatos, CA, USA  
IRumyantsev@atomera.com

Shuyi Li  
Atomera Inc.  
Los Gatos, CA, USA  
lishuyi@atomera.com

Hideki Takeuchi  
Atomera Inc.  
Los Gatos, CA, USA  
htakeuchi@atomera.com

**Abstract**— For continued scaling of DRAM, the fundamental architecture change from the conventional 6F<sup>2</sup> cell to the 4F<sup>2</sup> cell employing a vertical channel transistor (VCT) is essential. The VCT device must provide sufficient  $I_{ON}$  for read/write operation while meeting retention-time targets through suppression of the floating body effect along with stringent off-state leakage ( $I_{OFF}$ ) control, via suppression of gate-induced drain leakage (GIDL). In this TCAD simulation work, oxygen-inserted silicon (OI-Si) implemented in the starting Si substrate is demonstrated to enable precise doping-profile control to satisfy these VCT requirements. The starting substrate approach eliminates two source/drain epitaxial steps and one wafer-bonding step, thereby providing a simpler and more cost-effective integration path for 4F<sup>2</sup> DRAM.

**Keywords**—4F<sup>2</sup> DRAM, Floating Body Effect, GIDL, Junctionless Transistors, LDD, Oxygen Inserted Si, VCT, TCAD

## I. INTRODUCTION

Dynamic random-access memory (DRAM) based on the conventional 6F<sup>2</sup> cell is approaching its scaling limit, necessitating a transition to the 4F<sup>2</sup> cell that employs a vertical channel transistor (VCT) [1]. However, the floating-body effect (FBE) becomes a major challenge in VCT devices [2]. Owing to the fully depleted channel structure, holes generated by gate-induced drain leakage (GIDL) accumulate in the channel, lowering the barrier height between the channel and the source/drain (S/D). This can trigger a parasitic bipolar junction transistor (BJT) action, leading to leakage of charges stored in the storage capacitor. Therefore, suppression of GIDL is critical, in addition to controlling subthreshold leakage. While introducing a body contact in parallel with the bit-line (BL) contact can mitigate hole accumulation, it incurs a penalty in terms of increased cell area.

For read/write operations, the VCT device must be able to provide sufficient drive current ( $I_{ON}$ ) to charge/discharge the BL and the storage node (SN) capacitances. Due to the small dimensions,  $I_{ON}$  in VCT is highly sensitive to S/D and contact resistances. Although higher S/D doping concentration enhances  $I_{ON}$ , it introduces a trade-off with elevated GIDL current. Furthermore, the relatively high thermal budget of DRAM fabrication processes, compared to logic devices, imposes significant constraints on doping profile control. In particular, the out-diffusion of S/D dopants

during the thermal gate oxidation process can substantially reduce the doping concentration, leading to increased resistance and thus  $I_{ON}$  degradation. To mitigate these thermal budget limitations, S/D regions are formed by selective epitaxial growth of in-situ doped SiP film [3], leading to increased process complexities, however.

In this work, TCAD Sentaurus simulations are employed to identify the optimum device structure that meets the requirements for the 4F<sup>2</sup> DRAM VCT. The effect of incorporating a body contact, device configuration difference between back-gate (BG) and gate-all-around (GAA) structures, optimum lightly-doped drain (LDD) and channel doping profiles, and the impact of metal gate work function (WF) on retention requirements are systematically investigated for various device structures. Next, process simulations emulating DRAM thermal budgets are performed. The results demonstrate that oxygen-inserted silicon (OI-Si) enables the realization of the desired doping profiles from pre-engineered starting substrates, potentially leading to substantial simplification of the 4F<sup>2</sup> DRAM fabrication process.

## II. 2D DEVICE SIMULATIONS OF VCT STRUCTURE

Doping profile requirements for the VCT cell were studied using 2D S-Device [4] mixed mode simulations. Fermi Dirac statistics, doping-dependent mobility, high field saturation, SRH recombination, and the modified Hurkx band-to-band tunneling model were enabled. Device structures were built in 2D S-Process [5] by defining doping

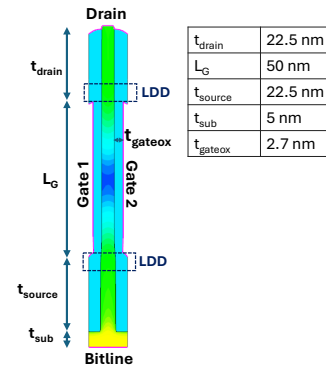


Fig 1: VCT Device Geometries. LDD regions (if used) are shown. For GAA, Gate 1 and Gate 2 are connected and for back gate, they are held separately.

profiles by in-situ doped epitaxial Si layers with minimum thermal budgets. VCT device geometries followed a half-pitch 6~8 nm nodes (**Fig. 1**). Device structures with the use of body contacts and LDD structures as well as back gate structure [6] were examined.

**Fig. 2** shows the effect of a body contact on the retention characteristics of “split BL” and “merged BL” structures. The split BL device provides holes in the channel with an escape path to the substrate contact, to mitigate the floating body effect. In contrast, holes in the merged BL device have no escape path to the substrate. **Figs. 2b** and **2c** compare retention characteristics of “1” and “0” states for 140 ms for split and merged BL structures, respectively. 8 ms of 1 V BL pulses were applied every 12 ms with the word line (WL) voltage fixed at 0 V. The body contact of split BL is seen to mitigate the storage voltage change for 1- state more effectively than the merged BL device. Also, the voltage change of 1- state is ~8x the 0- state for merged BL structures and ~3x for split BL structures. Hence, we focus on 1- state retention characteristics of the merged BL structure.

Correlation between retention characteristics and  $I_{OFF}$  was studied for VCT devices with different doping profiles and varying metal gate work function (WF). **Fig. 3** compares the 1- state retention characteristics and VCT  $I_{OFF}$ , at  $V_{DS} = 1.0$  V. It was found that  $I_{OFF}$  must be controlled below ~20 fA/um for the cell capacitance of 10 fF without the body contact.

Next, the impact of channel and LDD doping profiles, as well as metal gate WF, on GIDL was investigated. **Fig. 4** shows the process window of LDD profiles for three channel doping types: p-type ( $5 \times 10^{18} \text{ cm}^{-3}$ ), intrinsic, and n-type ( $5 \times 10^{18} \text{ cm}^{-3}$ ). For GIDL evaluation,  $I_D < 20 \text{ fA/um}$  at  $V_G = -0.4 \text{ V}$  was used, instead of  $I_{OFF}$  at  $V_G = 0 \text{ V}$ .

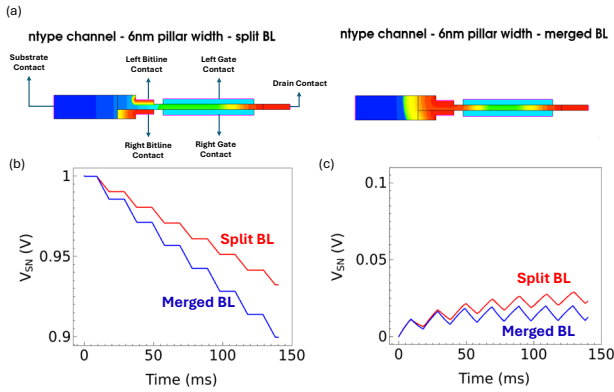


Fig 2: (a) Split bit-line (BL) and merged BL devices shown. The split BL creates a body contact connection to the substrate using p-type doping to split the n-type doping near the bitline contacts; Effect of both designs on retention voltage for (b) 1- state and (c) 0- state.

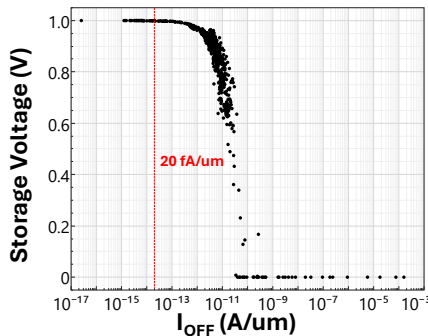


Fig 3: Correlation between  $I_{OFF}$  and storage node voltage programmed at 1 V after 140 ms for a 10 fF capacitor with no body contact.

When the LDD doping concentration is set to  $1 \times 10^{20} \text{ cm}^{-3}$ , the retention characteristics exhibit sensitivity to the metal gate WF (see inset of Fig. 4). A higher WF leads to the degradation of retention due to an increased vertical electric field [7]. However, when the LDD region is defined more than 12 nm away from the gate edge with phosphorus concentration between  $3 \times 10^{17} \text{ cm}^{-3}$  to  $1 \times 10^{19} \text{ cm}^{-3}$ , a high-WF metal gate was found to satisfy the GIDL criterion. Furthermore, within this LDD process window, the sensitivity to the channel doping type is relatively weak. A junctionless nFET [8] with n-type doped channel without the body contact can meet the retention requirements for the 4F<sup>2</sup> DRAM cell. Precise control of LDD doping profile is therefore critical for suppressing FBE.

**Fig. 5** compares  $I_{ON}$ - $I_{OFF}$  characteristics for back gate (BG) vs. gate-all-around (GAA) structures with no LDD. BG needs to pay penalty of about 1.5x~4x  $I_{ON}$  reduction compared to GAA, due to subthreshold swing degradation associated

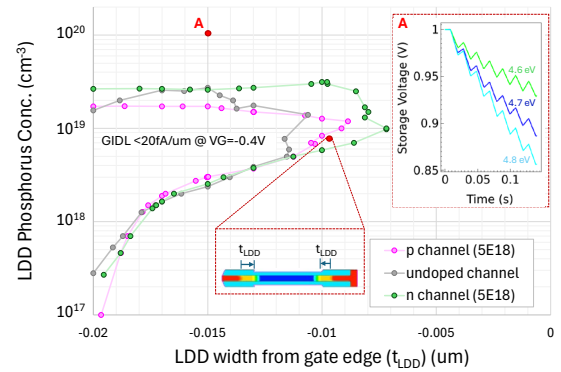


Fig 4: Process window of LDD profiles for  $I_D < 20 \text{ fA/um}$  at  $V_G = -0.4 \text{ V}$ . LDD of  $>12 \text{ nm}$  from gate edge and between  $3 \times 10^{17} \text{ cm}^{-3}$  and  $1 \times 10^{19} \text{ cm}^{-3}$  results in the lowest  $I_{OFF}$  at  $V_G = -0.4 \text{ V}$ . When outside this range (point A), higher WF leads to retention degradation due to GIDL.

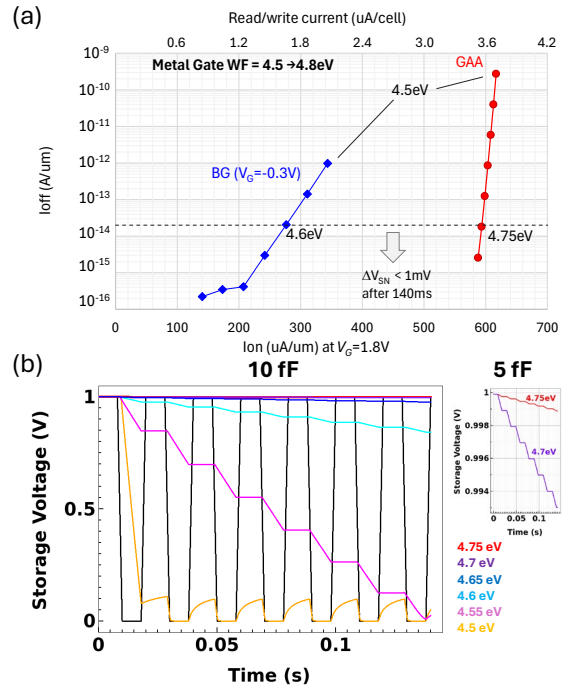


Fig 5: (a)  $I_{ON}$ - $I_{OFF}$  characteristics for BG and GAA structures; (b) For the GAA structure, the retention voltage through time is shown for the various metal gate WF shown in (a) for both 10 fF and 5 fF capacitors.

with weaker gate electrostatic control (**Fig. 6**) as well as reduction of the effective channel width. On the other hand, while mid-gap WF of  $\sim 4.6$  eV can meet  $I_{OFF} < \sim 20$  fA/ $\mu\text{m}$  for BG with  $V_{BG} = -0.3$  V, GAA requires high WF  $> 4.75$  eV. A molybdenum metal gate [9] or an ultra-thin ( $\leq 5$  nm) TiAlC film is reported to exhibit high WF  $> 4.75$  eV [10] and thus is suitable for the metal gate in the GAA VCT.

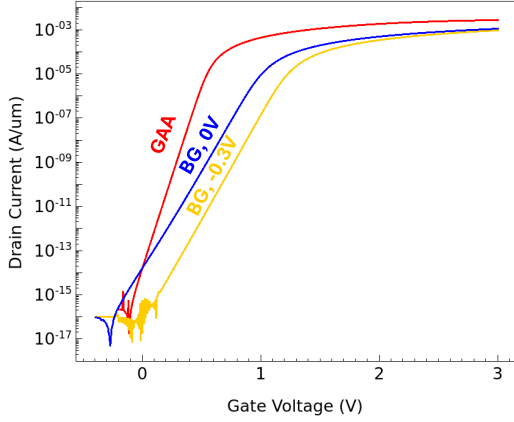


Fig 6: Transfer characteristics for GAA and BG ( $V_{DS} = 1.0$  V). BG shows degraded subthreshold swing compared to GAA.

### III. 2D PROCESS/DEVICE SIMULATION FOR VCT FABRICATION ON OI-Si STARTING SUBSTRATES

Due to the stringent requirements for gate leakage suppression and interface states control, a thermal oxide is required as the gate dielectric for the nano Si pillar VCT. In addition, the thermal budgets of the capacitor module and the S/D activation anneal impose significant constraints in doping profile control for the VCT fabrication. As a result, a low-temperature S/D doping process after capacitor formation [11] using selective epitaxy [3] along with a wafer bonding process [12] is required. To simplify the process complexities, we investigated a new approach in which the optimal VCT doping profile identified in the previous section

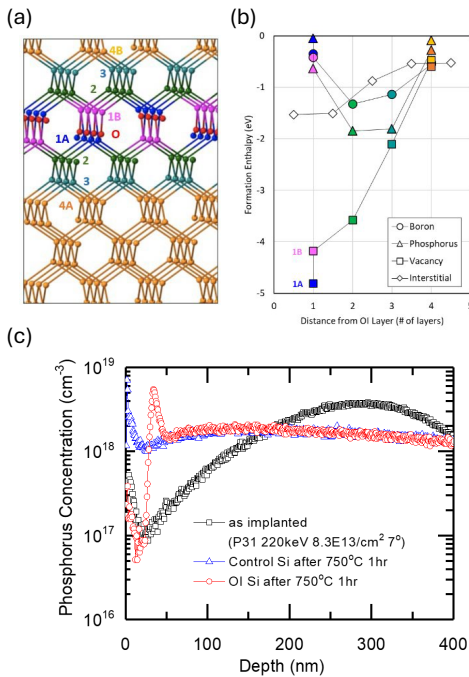


Fig 7: (a) atomistic model of OI-Si; (b) formation enthalpy change near the OI layer [14]; (c) comparison of phosphorus SIMS profiles after implantation and 750 C 1 hr anneal for Ctrl and OI-Si [15].

is predefined in the starting Si substrates by incorporating OI-Si in LDD and SD regions, using experimentally calibrated MSTcad<sup>TM</sup> [13]. In the OI-Si (**Fig. 7 (a)**), charge transfer from Si to Oxygen atoms due to the difference in electronegativity creates a thermodynamically stable environment in the vicinity of the OI layer compared to the bulk Si, for dopant atoms and point defects (**Fig. 7 (b)**) [14]. As a result, phosphorus atoms in Si are attracted to the OI layer leading to the pile-up in the OI-Si region during thermal processing (**Fig. 7 (c)**) [15]. This unique pile-up feature can be utilized for retaining phosphorus dopants in the predefined LDD and SD regions of the starting substrate throughout the DRAM thermal budget. For process simplicity, undoped Si channel is used for the starting substrate. **Fig. 8** compares  $I_{ON}$ - $I_{OFF}$  characteristics of GAA with varying metal gate WF, for pre-defined doping profile in Si substrates with and without OI-Si. An 850 C 3 min. RTO ( $t_{ox} = 2.7$  nm), 950 C 5 s RTA, and 750 C 2 hr anneal were applied to emulate the DRAM process thermal budget. The phosphorus pile-up effect of the OI-Si substrate is projected to result in  $2.5\sim 3\times$  increase in  $I_{ON}$ , and thus read/write current, while meeting the  $I_{OFF} < \sim 20$  fA/ $\mu\text{m}$  requirement for retention. Notably, phosphorus diffusion from LDD into the channel region is acceptable since junctionless VCT with an n-type channel can be employed for GIDL suppression.

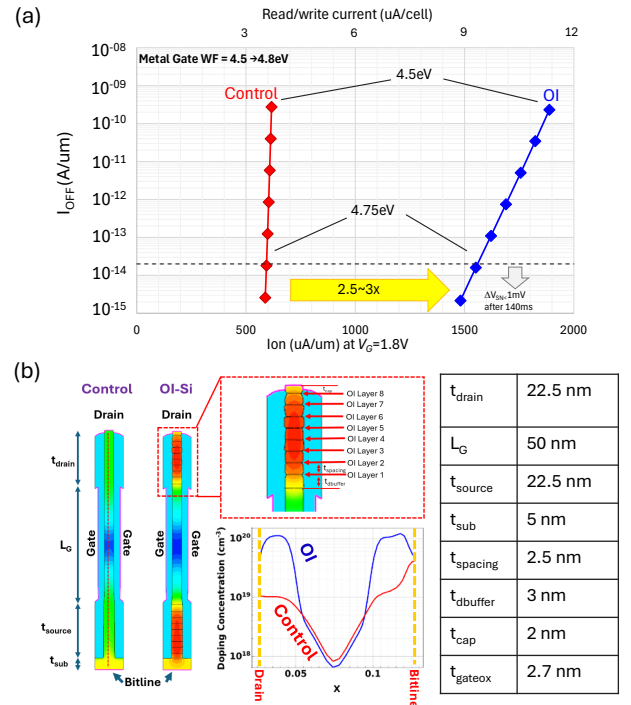


Fig 8: Comparison of VCT (a)  $I_{ON} - I_{OFF}$  characteristics and (b) phosphorus doping for control Si substrates vs. OI-Si substrates with pre-doped S/D, LDD, and channel profiles, after 850 C 3 min. RTO ( $t_{ox} = 2.7$  nm), 950 C 5 s RTA, and 750 C 2 hr anneals. OI-Si leads to  $2.5\sim 3\times$   $I_{ON}$  increase owing to phosphorus retention in the S/D regions through DRAM thermal cycles.

### IV. 3D TCAD SIMULATION FOR VCT ON OI-Si SUBSTRATE

The effectiveness of OI Si substrates with pre-defined optimal doping profile for GAA-type VCT was further evaluated via 3D TCAD, by importing 1D doping from 2D process simulations. **Fig. 9** shows that OI-Si substrates can

meet the  $I_{ON}$ – $I_{OFF}$  requirements under practical thermal process conditions.

The impact of contact resistance on  $I_{ON}$  with varying S/D doping profile and metal–nanopillar contact areas are further studied in a 4 nm pillar width device. Relatively high thermal budgets (850 C 3 min. RTO for gate oxide; 950 C 5 s S/D activation; 750 C 2 hrs. for capacitor process) were applied to predefined doping profile in starting substrates with and without the OI Si in the S/D regions. Two cases were investigated: 1) uniformly doped S/D with  $5 \times 10^{20} \text{ cm}^{-3}$  without LDD, and 2) graded S/D doping with LDD and  $1 \times 10^{21} \text{ cm}^{-3}$  doping in the contact region. The contact area was varied by changing the height of the side pillar exposed to the metal contact. A 50% deactivation of phosphorus during DRAM capacitor thermal cycle [16] was incorporated based on experimental measured contact resistivity as a function of phosphorus concentration [17]. **Fig. 10** shows the sensitivity of S/D doping and contact areas. Inclusion of contact resistance results in significant reduction of  $I_{ON}$  by ~87-92%. Notably, OI-Si starting substrates with uniformly doped S/D at  $5 \times 10^{20} \text{ cm}^{-3}$  are projected to yield appropriate LDD doping profile to achieve  $I_{OFF}$  spec due to phosphorus diffusion during the high thermal cycles while achieving write current of 6.14  $\mu\text{A}/\text{cell}$  (1.535  $\text{mA}/\mu\text{m}$ ) at  $V_G$  of 1.8 V for a 6 nm contact sidewall height. Increasing the exposed pillar sidewall height to 5~6 nm improves  $I_{ON}$  by 3~5x compared to contacting only the bottom of the pillar.

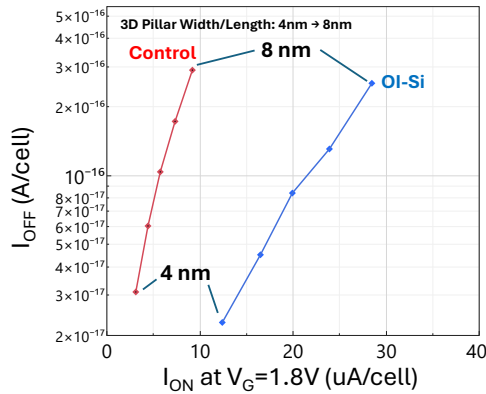


Fig 9: OI-Si substrates have low  $I_{OFF}$  and maintain higher  $I_{ON}$  than the control even in 3D TCAD. This repeats Fig. 8 for only  $WF = 4.75 \text{ eV}$  and different pillar cross-sectional area.

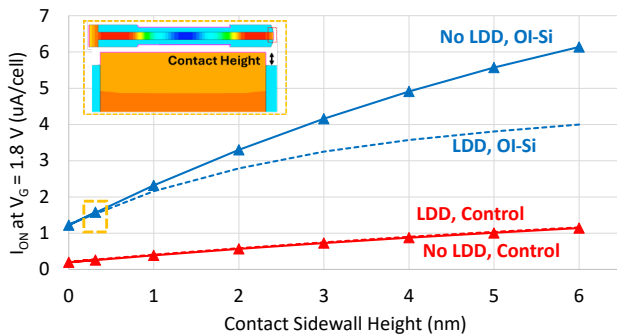


Fig 10:  $I_{ON}$  vs. contact sidewall height for (1) structure with no LDD and uniformly doped S/D of  $5 \times 10^{20} \text{ cm}^{-3}$  and (2) structure with LDD of  $1 \times 10^{19} \text{ cm}^{-3}$  within 12 nm of gate edge and  $1 \times 10^{21} \text{ cm}^{-3}$  within 0.2nm of contact. OI shows more improvement in  $I_{ON}$  with increasing contact sidewall height than control with 3~5x improvement for 5~6nm sidewall height compared to only the bottom of the pillar.

## V. CONCLUSIONS

OI-Si substrates enable the simplest process integration solutions by predefining ideal doping profile in the starting substrates, owing to its excellent phosphorus retention characteristics through DRAM thermal budgets. It also enables precise LDD doping profile control, requiring between  $3 \times 10^{17} \text{ cm}^{-3}$  to  $1 \times 10^{19} \text{ cm}^{-3}$  and greater than 12 nm from the gate edge in the 4 nm diameter Si pillar, to meet retention requirements for VCT in 4F<sup>2</sup> DRAM cells without body contact to manage the floating body effect. Along with gate work function control ( $WF > 4.75 \text{ eV}$ ) and a side pillar contact scheme, junctionless GAA nFET on OI-Si substrate can provide high read/write current.

## REFERENCES

- [1] K. -W. Song *et al.*, "A 31 ns Random Cycle VCAT-Based 4F DRAM With Manufacturability and Enhanced Cell Efficiency," in *IEEE J. Sol.-Stat. Cir.*, vol. 45, no. 4, pp. 880-888, April 2010.
- [2] Y. Cho *et al.*, "Suppression of the Floating-Body Effect of Vertical-Cell DRAM With the Buried Body Engineering Method," in *IEEE Trans. on Elect. Dev.*, vol. 65, no. 8, pp. 3237-3242, Aug. 2018.
- [3] P. Sahu, *et al.*, "SiP Epitaxial Growth for DRAM Bit Contact", *J. Elct. Mat.*, vol.54, pp.2390-2936 (2025)
- [4] S-Device Manual, ver. 2024.09 W, Synopsys (2024).
- [5] S-Process Manual, ver. 2024.09 W, Synopsys (2024).
- [6] M. Jeong *et al.*, "Effect of Back Gate on Word Line Disturb Immunity of a Vertical Channel DRAM Cell Array Transistor," *2024 IEEE IRPS*, Grapevine, TX, USA, 2024, pp. P23.MR-1-P23.MR-4.
- [7] I.A. Khan, *et al.*, "Work Function Engineering to Improve Data Retention Due to Floating Body in 3-D GAA Stacked Nanosheet Based DRAM", *IEEE Trans. on Elect. Dev.*, vol. 71, no. 12, pp.7412-7417, Dec. 2024.
- [8] A. Yoo, *et al.*, "High-Performance Gate-all-around Junctionless Vertical-Channel Transistors with the Ultra-low Sub-threshold Swing for Next-generation 4F2 DRAM," *IEEE IEDM* pp. 1-4 (2023), .
- [9] Q. Lu, *et al.*, "Molybdenum metal gate MOS technology for post-SiO<sub>2</sub> gate dielectrics," *IEEE IEDM*, pp. 641-644 (2000)
- [10] J. Xiang *et al.*, "Investigation of TiAlC by Atomic Layer Deposition as N Type Work Function Metal for FinFET," *ECS J. Solid State Sci. Technol.*, vol. 4, no. 12, p. P441, Oct. 2015, doi: 10.1149/2.0231512jss.
- [11] Z. Chen, *et al.*, "Structures and Methods for Forming 4F2 Dynamic Random-Access Devices," U.S. Patent 2025/0380398, A1, Dec. 11, (2025).
- [12] H. Yoon, *et al.*, "15.10 A Vertical-Cell-Transistor-Based 4F2 DRAM with Cell-on-Peripheral Architecture Using Wafer-to-Wafer Hybrid Copper Bonding," *2026 IEEE ISSCC* pp. 272-274 (2026).
- [13] D. Connelly, *et al.*, "Suppressing Oxidation-Enhanced Diffusion of Boron in Silicon With Oxygen-Inserted Layers," *IEEE J. Elect. Dev. Soc.*, vol. 6, pp. 1173-1178, (2018).
- [14] H. Takeuchi, *et al.*, "Remote Control of Doping Profile, Silicon Interface, and Gate Dielectric Reliability via Oxygen Insertion into Silicon Channel," *2022 IEEE IMFEDK*, pp. 1-4 (2022).
- [15] H. Takeuchi *et al.*, "Punch-Through Stop Doping Profile Control via Interstitial Trapping by Oxygen-Insertion Silicon Channel," *IEEE J. the Elect. Dev. Soc.*, vol. 6, pp. 481-486, (2018).
- [16] Y. Ueno, *et al.*, "High re-activation and precise diffusion control of epitaxial Si:P layers using flash lamp annealing," *MRS Advances*, vol. 10, pp. 238-243, (2025).
- [17] C. Porret *et al.*, "Low temperature source/drain epitaxy and functional silicides: essentials for ultimate contact scaling," *IEEE IEDM*, pp. 34.1.1-34.1.4 (2022).