

Vertical Channel-All-Around a-IGZO-FET Towards 2T1D DRAM Design with Self-Boosted Storage-Node Voltage

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Abstract—This work presents a 2T1D DRAM cell based on vertical channel-all-around a-InGaZnO field effect transistors (CAA-FETs). A calibrated simulation framework based on fabricated devices is employed to systematically investigate the capacitance characteristics of CAA-FETs. To mitigate the impact of parasitic coupling on the storage node in memory cells, an insulator-metal-insulator-metal (IMIM) structure with an additional top oxide layer is proposed, enabling linear tunability of the overlap capacitance. The asymmetric capacitance behavior of CAA-FETs is also analyzed to enhance the retention and stability of capacitorless DRAM gain cells. The proposed 2T1D DRAM employs a reconfigurable gated diode as a nonlinear capacitor to realize self-boosting of the storage-node voltage while maintaining a compact cell footprint of $4F^2$. A read current margin of 10^4 is achieved at an ultra-low operating voltage of 0.2 V. Furthermore, 3D array-level evaluation demonstrates that data integrity is maintained even after 2500 row hammer cycles.

Keywords—2T1D DRAM, channel-all-around, capacitance, IGZO, row hammer effect.

I. INTRODUCTION

Compared with conventional planar 2T0C DRAM cells, Vertical channel-all-around (CAA) architectures enable monolithic 3D integration and scaling of dynamic random-access memory (DRAM) beyond the $4F^2$ limit[1]. Capacitorless gain cells based on oxide semiconductors, such as IGZO, have attracted increasing attention due to their low leakage and compatibility with high-density integration[2]. However, at low voltage, capacitorless DRAM suffers from severe storage-node voltage (V_{SN}) degradation caused by parasitic capacitance coupling, limiting sensing margin and retention performance[3]. This issue is more pronounced in vertical CAA structures, where source-drain asymmetry and complex electrostatic coupling significantly affect memory performance. To address this, an insulator-metal-insulator-metal (IMIM) structure with an additional top oxide layer is introduced to suppress parasitic coupling and enable tunable capacitance. The capacitance variation induced by device asymmetry is systematically investigated. Furthermore, by exploiting the large gate overlap in the CAA structure, a reconfigurable gated diode is realized as a nonlinear capacitor, enabling self-boosting of the V_{SN} while maintaining a compact $4F^2$ cell footprint. The proposed 2T1D DRAM achieves a large sensing margin at ultra-low voltage and demonstrates strong robustness against array-level disturbances, providing a promising pathway for low-power and high-density memory applications.

II. EXPERIMENT AND MODEL CALIBRATION

To establish an accurate simulation model, CAA-FETs with $CD = 600$ nm and $L = 50$ nm were fabricated[4]. A

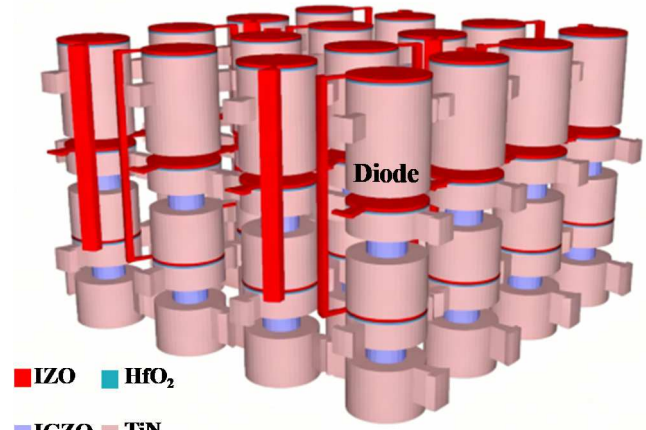
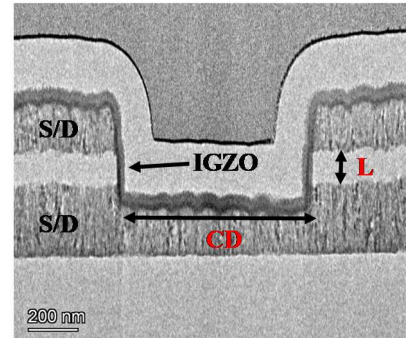
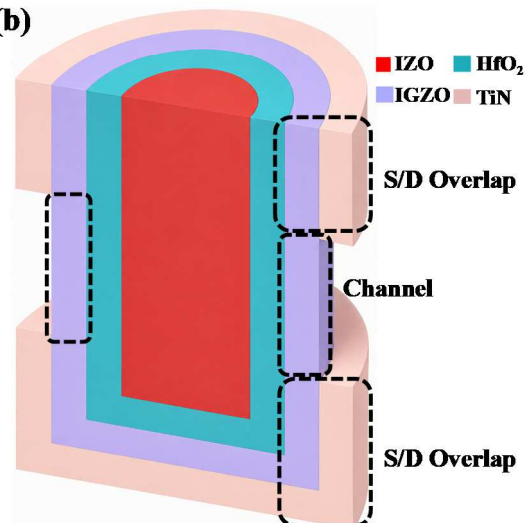


Fig. 1. Schematic of the 3D structure of a 2T1D DRAM array based on CAA-FETs.

(a)



(b)



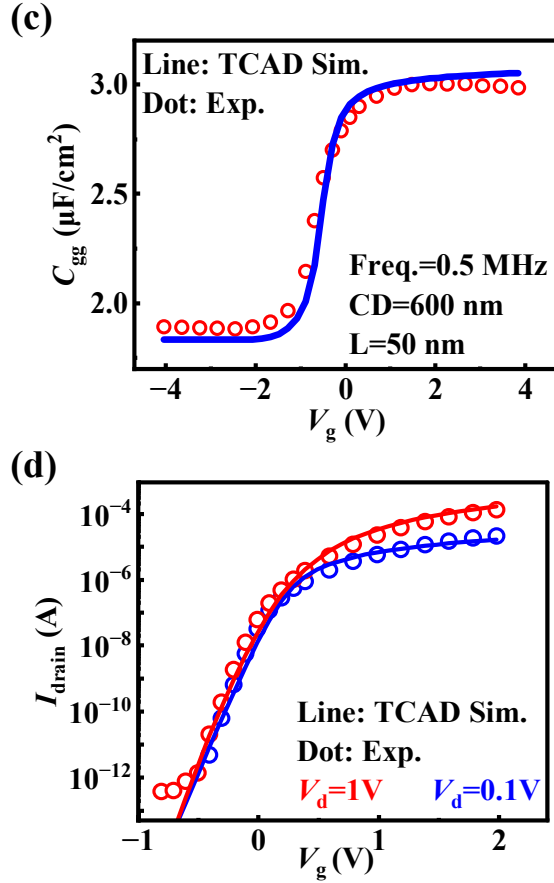


Fig. 2. (a) Cross-sectional TEM image of the fabricated CAA-FETs. (b) 2D cross-sectional schematic of the CAA-FETs structure. (c) Capacitance characteristics of the device and fitting with TCAD simulations. (d) The transfer characteristics of the device and their fitting with TCAD simulation results.

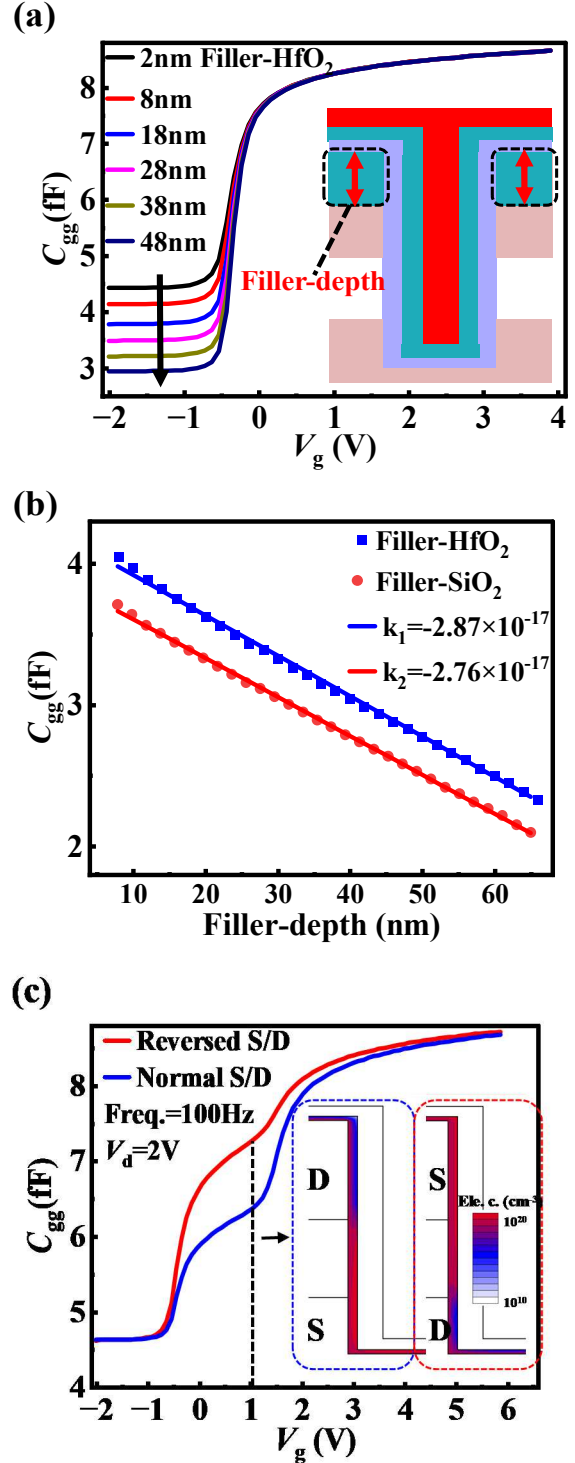
TiN/SiO₂/TiN (MIM) stack was formed to define the vertical source/drain electrodes, followed by via etching to create the vertical channel region. Plasma-enhanced atomic layer deposition (PEALD) was then used to conformally deposit the IGZO channel, the HfO₂ gate dielectric, and the In-Zn-O (IZO) metal gate along the via sidewalls. Oxygen plasma was employed during IGZO deposition to suppress hydrogen incorporation. The channel width is defined by the via perimeter, while the effective channel length is mainly determined by the SiO₂ thickness and etching profile. Fig. 2(a) shows a cross-sectional TEM image of the device. In the off-state, the capacitance of the CAA-FETs is dominated by the gate-source/drain overlap regions as indicated in Fig. 2(b). During turn-on, the capacitance is further influenced by the IGZO material properties and bias conditions. To analyze the capacitance characteristics more comprehensively, a TCAD model was established using the Victory Device simulator in SILVACO, as shown in Fig. 2(c), which shows good agreement with the measured capacitance data. Fig. 2(d) shows the transfer curves of the device, and the experimental results are in good agreement with the simulations.

III. RESULTS AND DISCUSSION

To reduce the overlap parasitic capacitance in CAA-FETs, an IMIM structure is proposed. An additional oxide layer is deposited as an isolation layer between the IGZO channel and the gate. As shown in Fig. 3(a), the C-V characteristics of the

improved device are presented. Increasing the isolation thickness reduces the electrode-channel overlap region, thereby decreasing the parasitic capacitance. Fig. 3(b) shows the variation of C_{gg} with filler-depth for two filling materials, HfO₂ and SiO₂. Using a filler with a lower dielectric constant further reduces the parasitic capacitance. As shown in Figs. 3(c, d), capacitance asymmetry in CAA-FETs, induced by different drain bias conditions, can be exploited to modulate coupling during the write operation, thereby improving storage-node stability.

Based on the capacitance analysis of CAA-FETs, a 2T1D



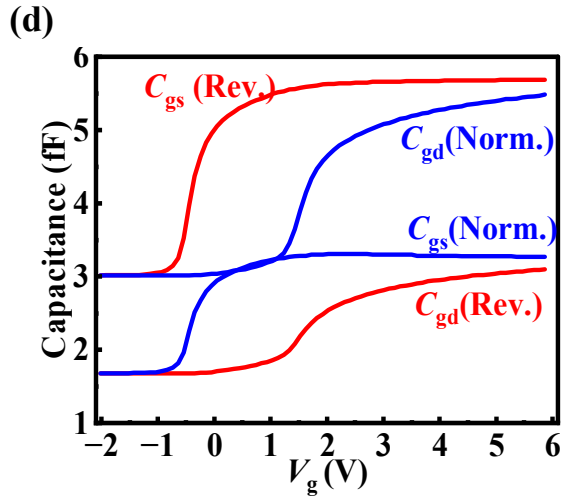


Fig. 3. (a) C - V characteristics after partially filling the drain side with oxide to isolate the IGZO channel. (b) Capacitance variation trends for different oxide-filled electrode configurations. (c) Asymmetric C_{gg} - V_g for the CAA-FETs after source/drain exchange. (d) Asymmetric C_{gd} - V_g and C_{gs} - V_g for the CAA-FETs after source/drain exchange.

structure with self-boosted V_{SN} is proposed. Fig. 4(a) shows the circuit schematic [5]. Fig. 4(b) compares V_{SN} in 2T0C and 2T1D when writing 1 V. By reducing the parasitic capacitance (C_{WWL-SN}), the coupling voltage drop is limited to 0.1 V. As V_S increases, V_{SN} rises from 0.9 V to 2.508 V, improving read accuracy and storage window. Fig. 4(c) analyzes the effect of overlap capacitances of the write transistor and the diode (1D). The intrinsic structural characteristics of the CAA diode give rise to a large overlap capacitance. As a result, enhanced charge transfer between

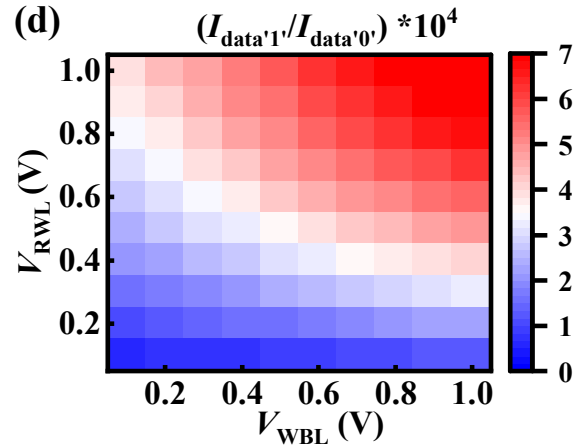
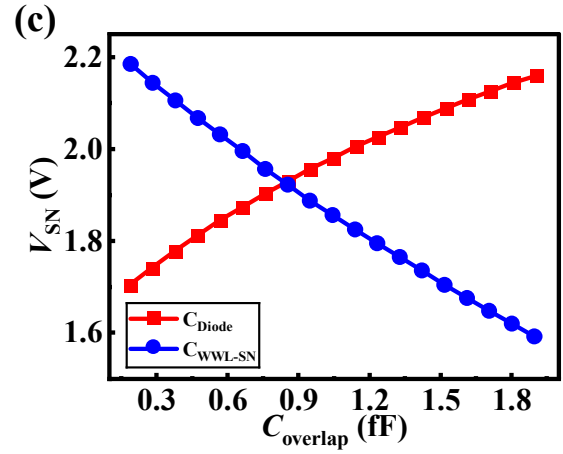
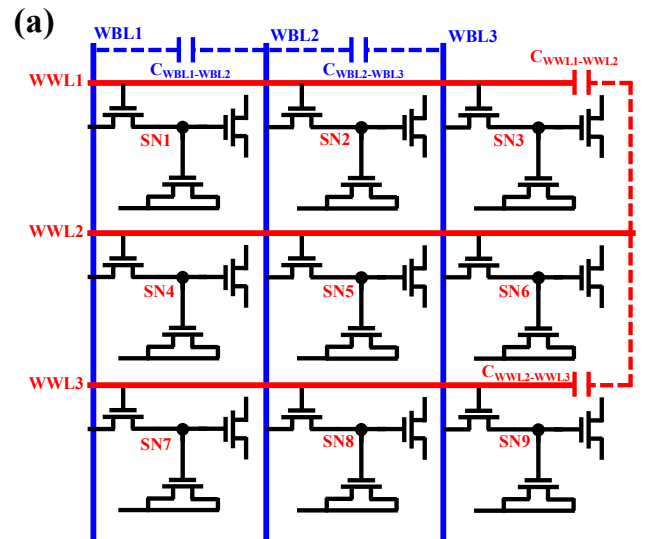
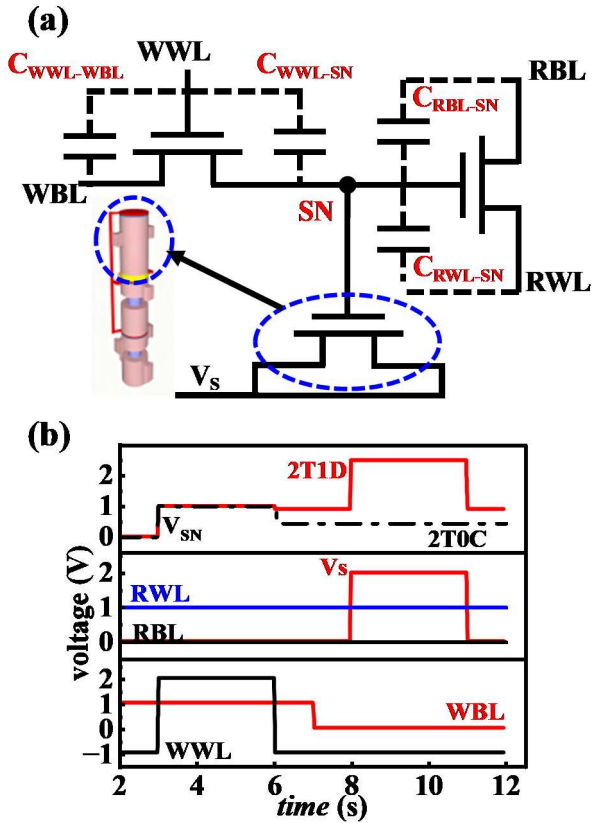


Fig. 4. (a) Schematic diagram of the 2T1D circuit. (b) Read and write operation waveforms of the 2T1D and 2T0C structures. (c) Dependence of the V_{SN} on parasitic capacitance. (d) Storage window under different operating voltages.

the off-state and on-state capacitances can effectively boost V_{SN} . Fig. 4(d) shows the storage current window of the CAA-based 2T1D varying write-bit-line (V_{WBL}) and read-word-line (V_{RWL}) voltages, achieving a large window of 10^4 at a low operating voltage of 0.2 V. Furthermore, by increasing the effective storage-node capacitance after introducing the diode, the retention time of the DRAM cell can be extended



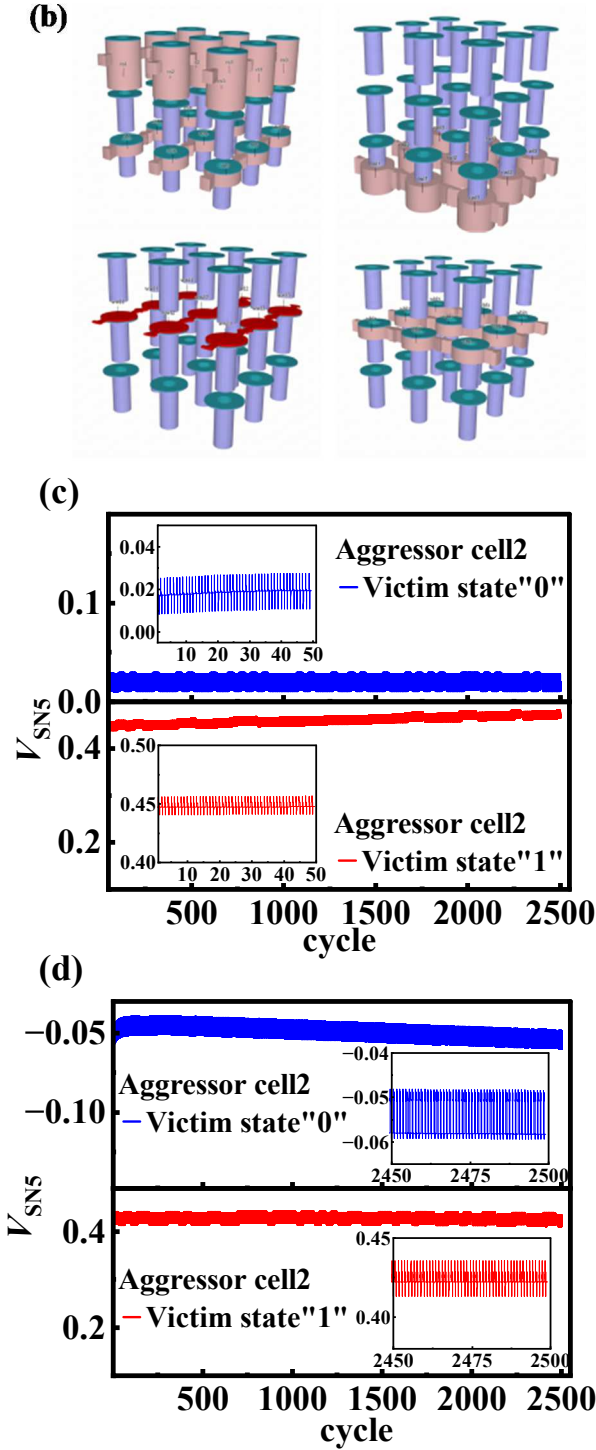


Fig. 5. (a) Circuit schematic of a 3×3 array. (b) 3D schematic of cell interconnections. (c) Row hammer attack with repeated "1" writes. (d) Row hammer attack with repeated "0" writes.

under the same leakage-current condition.

Capacitive coupling is an important factor contributing to the row hammer effect in conventional DRAM structures. As shown in Fig. 5(a), to evaluate the reliability of the 2T1D array, a 3×3 2T1D array is constructed and the parasitic capacitances between adjacent cells are extracted[6]. Fig. 5(b) shows the 3D schematic of the interconnections between neighboring cells, where adjacent cells are filled with SiO₂. Figs. 5(c, d) illustrate the impact on the V_{SN5} of a neighboring cell when SN₂ is repeatedly written with data "1" and data "0",

respectively, for 2500 hammering cycles. During this process, the charge-leakage path induced by the parasitic capacitance between adjacent read transistors was also taken into account[7]. The maximum voltage variation of the victim cell is only 0.02 V, with no bit flip observed, indicating that the 2T1D array exhibits good data retention under row hammer disturbance.

IV. CONCLUSION

This work proposes a 2T1D DRAM cell based on vertical CAA-FETs with self-boosted V_{SN} enabled by nonlinear capacitance. An IMIM structure suppresses parasitic coupling, while asymmetric capacitance is analyzed to mitigate coupling effects. The cell achieves a sensing margin of 10⁴ at 0.2 V with a compact 4F² footprint and shows strong robustness against row hammer disturbance. These results demonstrate the potential of capacitance engineering in CAA devices for low operation voltage, high-density DRAM.

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