Assessment of the Charge Trapping Behaviors in Ferroelectric Field-Effect Transistor Based Ternary Content Addressable Memory

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***Abstract*—Ternary content addressable memories (TCAMs) is vital in network routers, caches, and machine learning. Ferroelectric field effect transistor (FeFET) based TCAMs are promising for modern computing and data processing due to their high on-off ratio, non-volatility, and CMOS compatibility. However, the impact of charge trapping/detrapping behaviors in FeFET on TCAM performances has not been fully studied. We have established a compact FeFET device model that considers the complex couplings of charge trapping/detrapping behaviors and ferroelectric polarization dynamics. This model is used to simulate a TCAM based on two FeFET units, and the impact of trap density and pulse delay on TCAM performances is explored. The simulation results show that charge trapping has a significant impact on the search accuracy and functional reliability of FeFET-TCAM, which can provide a reference for ferroelectric memory design.**

***Keywords*—FeFET, TCAM, Compact modeling, Charge trapping, hafnium oxide ferroelectric.**

I. Introduction

The ternary content addressable memories (TCAMs) are associative memories that support fast parallel searches. They can directly match and query stored data in memory, outputting corresponding results and locations, thereby effectively alleviating the processor-memory bottleneck in traditional computing architectures [1],[2],[3]. As a highly promising core component of in-memory computing (IMC), TCAMs are not only widely used in traditional fields such as network routers and associative caches, but also play a key role in applications such as machine learning, neuromorphic computing, and bioinformatics [4],[5],[6].

The hafnium oxide (HfO_2) ferroelectric memories are promising candidates as emerging storage and computing technology, owing to their excellent compatibility, good scalability, low-power operation, and high-density integration [7]. The HfO_2 ferroelectric field effect transistors (FeFETs) have been used to implement TCAMs through two parallel FeFETs [8]. Compared with traditional SRAM-based TCAMs using 16 transistors, FeFET-based TCAMs have advantages in cell compactness, non-volatility, and energy efficiency, thanks to the high on/off ratio, three-terminal structure, and compatibility with CMOS processes of FeFETs [9].

However, the charge trapping/detrapping behaviors, originating from the intrinsic defects of the HfO_2 ferroelectric (FE) and the interfaces of HfO_2/interfacial layer (IL) and IL/Si, constitute a primary reliability challenge in FeFETs by introducing unstable device characteristics [10]. While the intricate coupling between these charge trapping phenomena and ferroelectric polarization switching dynamics has been thoroughly studied from both experimental characterization and theoretical modeling perspectives [11], their specific effects on the FeFET-based TCAM operation remain largely unexamined. Of particular concern is how the resulting threshold voltage (V_{TH}) instability could lead to erroneous search operations or complete matching failures in TCAM based arrays, potentially compromising their practical implementation in memory and computing systems.

In this work, a compact model of FeFET devices is established, which includes ferroelectric loop trajectories, switching dynamics, ferroelectric history effects, and charge trapping/detrapping, etc. Circuit simulations are performed on the FeFET-TCAM unit, and the effect of trapped charge/FE polarization coupling on the performance of FeFET-TCAM is revealed by matching the change of voltage drop on the line, which is a function of trap density and pulse delay.

II. Simulation Method

Fig. 1(a) shows a schematic of FeFET device, which consists of a ferroelectric capacitor integrated on a MOSFET. The complex couplings between the defect charge trapping/ detrapping processes and the ferroelectric polarization charges as well as the channel charges are also illustrated. Fig. 1(b) depicts the equivalent circuit diagram of FeFET gate stack, which can be regarded as a series connection of FE module, charge trapping (CT) module and MOSFET module. The electrostatics of the FeFET, particularly influenced by the polarization charges in ferroelectric layer and the defect distributions at the FE/IL interface, is governed by the charge balance and charge balance as seen in Fig. 1(a). The obtained electrostatics in turn determines both the polarization switching dynamics and the consequent charge trapping /detrapping behaviors in the device. The detailed simulation process is shown in Fig. 2.

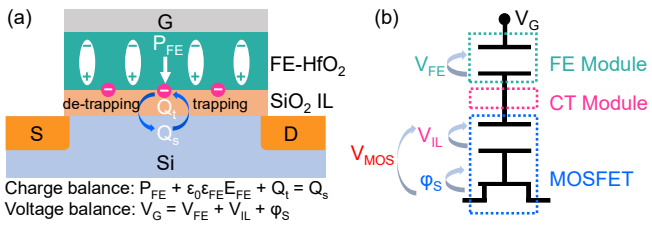

Fig. 1. (a) Schematic of FeFET, showing the coupled charge trapping/de-trapping and ferroelectric polarization switching dynamics. (b) Equivalatent circuit of the gate stack in FeFET, including three modules with FE module, CT module, and MOSFET in series connection.

For FE module, the Preisach model is used to calculate the ferroelectric polarization switching behaviors, and the time-dependent switching dynamics is considered by

introducing the RC delay model [12]. This model can accurately capture the major/minor loops and ferroelectric history effects. As shown in Fig. 3, the green curve represents the ferroelectric polarization direction downward, and the orange curve represents the upward one. The A-G point represents the turning point, which are used to calculate the scaling constants *m* and *b*. For a simple example, if we want to calculate the polarization curve from B to C, the scaling constants *m* and *b* are calculated from the stored polarization values of points A and B, and are substituted into the saturation hysteresis curve.

For CT module, the two-state nonradiative multiphonon (NMP) model can effectively characterize the underlying mechanisms that governs the charge trapping and detrapping behaviors in the system. The tunneling coefficient is calculated by the Wentzel-Kramers-Brillouin (WKB) approximation model [14]. The occupancy probability (P_{occ}) is evaluated at each time based on the carrier capture and emission constants (k_{21} and k_{12}).

Then the FE and CT modules are coupled into the MOSFET module which is described by the BSIM-BULK106.2 model [13]. For each time step, the FE module, CT module and MOSFET module are coupled for self-consistent solution through the charge balance equation and the voltage balance equation. Finally, a FeFET SPICE model based on the Verilog-A language is established, and the HSPICE platform is embedded to realize the collaborative simulation of FeFET devices and TCAM circuits.

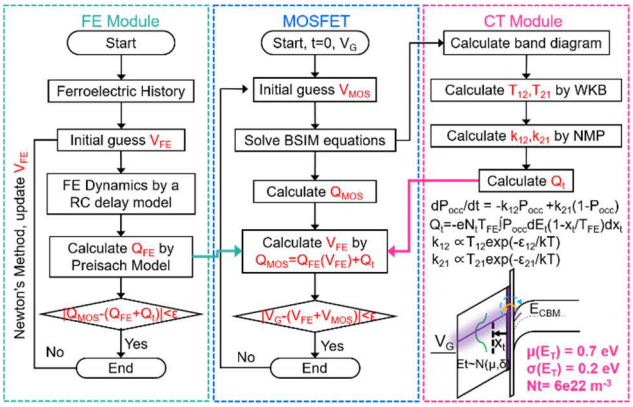

Fig. 2. A dynamic compact model of FeFET, where the FE dynamics are modeled by Preisach model using a RC delay function as seen in Fig.3, and the CT dynamics is modeled by the NMP model, both of which are coupled into the MOSFET module for a self-consistent calculation.

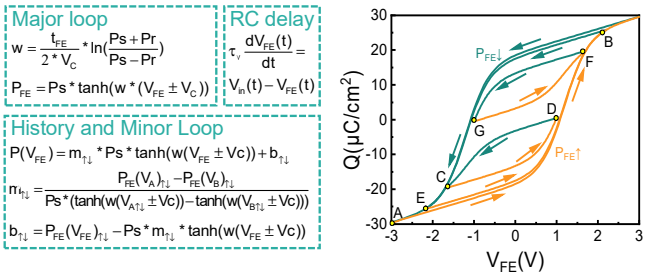

Fig. 3. The Preisach model that well captures the FE history and minor loops.

III. Results and Discussion

A. *FeFET Model Validation and CT Behaviors*

The comparison between simulated and experimental I-V curves for FeFET is shown in Fig. 4(a) and (b), where the experimental data are taken from [15]. For the calibrated FeFET, the thickness of the HfO_2 ferroelectric layer is 10 nm, the thickness of the SiO_2 interfacial layer is 3 nm, the gate length and width are both 10 μm, the remnant polarization and coercive field are 18.5 μC/cm² and 1.2 MV/cm, the program and erase voltages V_{PRO}/V_{ERS} are ±4V, respectively. The good agreement in the memory window (MW) characteristics verifies our compact FeFET model, which can be reliably used to predict the key electrical characteristics of FeFET devices and circuits.

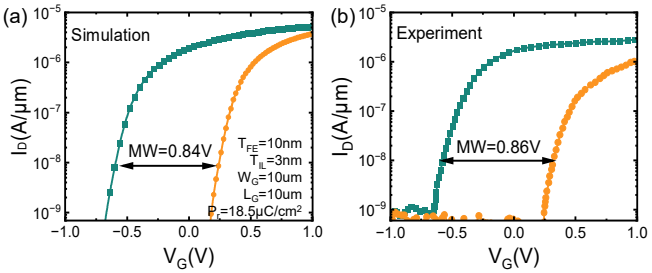

Fig. 4. (a) Simulated and (b) experimental I-V curves from [15] of the FeFET.

Fig. 5(a) shows the read I-V characteristic curves obtained by adjusting the amplitude of V_{PRO}/V_{ERS} under the fixed pulse width (PW). The simulation results clearly capture the shift of the V_{TH} under the high threshold voltage (HVT) and low threshold voltage (LVT) states. This shift originates from the partial polarization switching process of the ferroelectric material, resulting in a reduction in the memory window. In addition, Fig. 5(b) characterizes the MW changing with PW under different V_{PRO}/V_{ERS} conditions, which is consistent with the experimental results. When the PW is fixed, the MW shows a monotonically increasing trend with the increase of voltage amplitude, while under the condition of fixed voltage amplitude, the MW initially rises rapidly with the increase of the PW, which reflects the transient response process of polarization reversal, but when the PW exceeds a certain critical value, the MW gradually tends to saturation, indicating that the polarization reversal process reaches saturation.

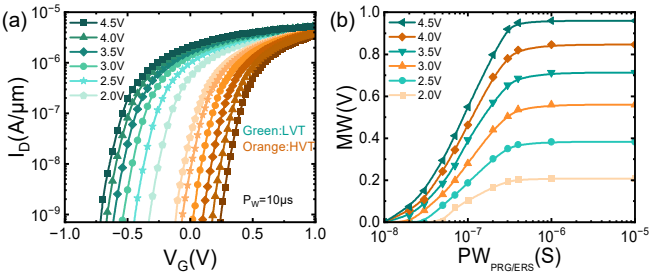

Fig. 5. (a) I-V curves under different V_{PRO}/V_{ERS} with a fixed P_W. (b) MW as a function of PW under different V_{PRO}/V_{ERS}.

To further investigate the threshold voltage relaxation process caused by charge trapping/detrapping dynamics, we calculate the I-V curves with the defect model at different delay stress times (T_{delay}), from 700 μs to 10 ms, with applied waveform as shown in Fig. 6(a). The defect energy levels E_T follow a normal distribution, with $\mu(E_T)$ = 0.7 eV and $\sigma(E_T)$ = 0.2 eV, and the defect density N_t is 6×10^{22} m^{-3}, as shown in the CT module of Fig. 2. Then Fig. 6(b) shows the CT behaviors on the I-V characteristic curves of FeFET. The V_{TH} shift in the LVT state is very significant, especially in the short T_{delay} condition, which is caused by the rapid charge capture within a very short T_{delay}. As T_{delay} gradually increases, the charge is decaptured and the V_{TH} gradually approaches a stable state. In contrast, the V_{TH} in the HVT

state is almost unaffected. The V_{TH} in LVT and HVT versus T_{delay} are derived in Fig. 6(c).

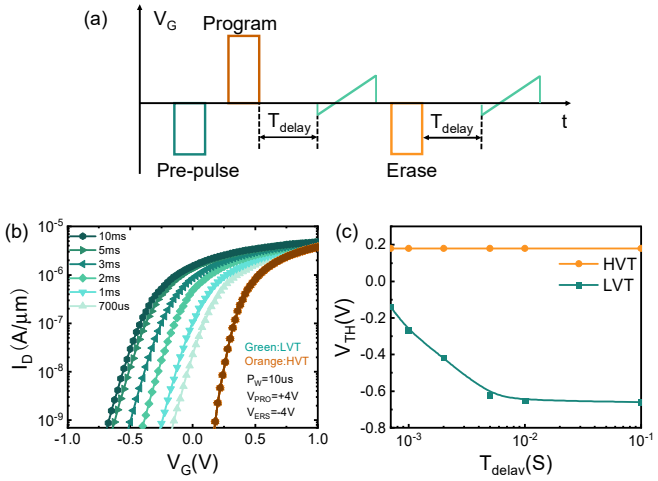

Fig. 6. (a) Applied waveform to consider the T_{delay}. CT effect on the (b) I-V curve, and (c) V_{TH} as a function of T_{delay}.

B. *CT Effects on FeFET-TCAM Performance*

We investigate a 2FeFET based TCAM cell, which adopts a complementary write scheme with CLK as the enable signal, where the matching line (ML) is precharged to V_{DD} before the search operation, and an external sense amplifier (SA) circuit is used to amplify the output match line signal, as shown in Fig. 7 [16]. The gates of the two FeFETs serve as the write port (WP) and the read port (RP). To write a logic "1" to a TCAM cell, a positive voltage pulse (+4 V) is applied to the node WP/RP to set M1 to the LVT state, and a negative voltage pulse (-4 V) is applied to the node WP/RP to set M2 to the HVT state. Similarly, a logic "0" can be written to the cell by setting M1 and M2 to HVT and LVT, respectively. To write a don't care into a TCAM cell, a -4V voltage needs to be applied to both FeFETs. At this time, the FeFETs are in HVT state, and M1 and M2 will not be turned on no matter how the search voltage is applied.

The ML is precharged to V_{DD} through a p-type transistor, and then a read voltage is applied to nodes WP/RP and WP/RP to read the state of the TCAM cell. If in the matching state, such as storing logic "1" and searching logic "1", M1 is in the LVT state and M2 is in the HVT state. The search lines apply -1V and 0V respectively, and M1 and M2 cannot be turned on. Similarly, if in the mismatching state, storing logic "1" and searching logic "0", the 0V search voltage will turn on M1 in the LVT state, causing the voltage drop on the ML to change, as shown in Fig. 8.

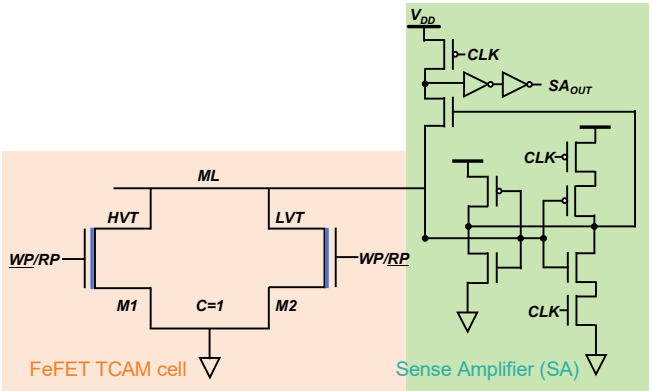

Fig. 7. Schematics of 2FeFET based TCAM cell with external SA circuits.

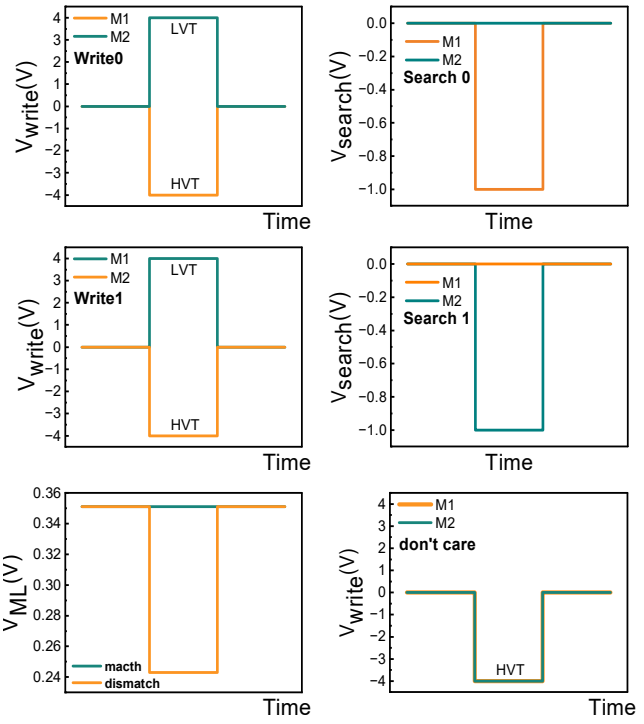

Fig. 8. Simulated "write 0", "write 1", "don't care", "search 0", "search 1", "match", "dismatch".

In order to systematically study the effect of defect density in FeFET on the defect behavior of TCAM circuit and its performance degradation, we applied a constant stress time of 1 μs to the device. As shown in Fig. 9(a) and (b), when the storage cell is in a mismatch condition (storing the logic "1" state), the defect charge accumulation inside the FeFET will gradually increase with the increase of defect density. This charge accumulation process causes the LVT characteristics of the device to shift significantly to the right, and its shift eventually exceeds the 0 V search voltage threshold preset by the circuits. The V_{TH} shift will have serious circuit-level consequence as follows.

Firstly, it may cause the transistor M1, which should be in the on state, to turn off, thereby destroying the normal current path. This state transition further causes the abnormal rise of the match line voltage (V_{ML}). When the V_{ML} exceeds the critical value of 0.32 V, it will trigger the subsequent circuit to produce an incorrect logic judgment. Specifically, the output state of the SA abnormally jumps from the correct low logic level to the high logic level, thereby mistakenly identifying the actual mismatch state as the match state.

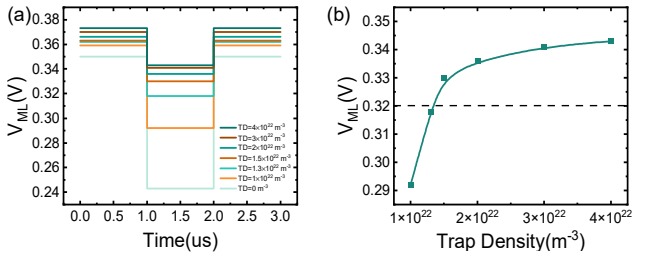

Fig. 9. (a) In "dismatch" state, the V_{ML} drop decreases with trap density N_t increasing. (b) Derived V_{ML} level versus N_t. When the V_{ML} is less than 0.32 V, the SA output flips, putting a trap density limit to make TCAM work right.

Secondly, Fig. 10(a) and (b) show the effect of stress time T_{delay} on TCAM. Shortening the stress time causes an

increase in defect charge, which causes the LVT voltage to shift to the right above the search voltage (1V). This transition also forces the SA output to change from low to high, falsely indicating a mismatch state.

Both abovementioned phenomena can cause erroneous state transitions during the TCAM operation, significantly reducing the matching accuracy of the content-addressable search function and ultimately affecting the overall reliability.

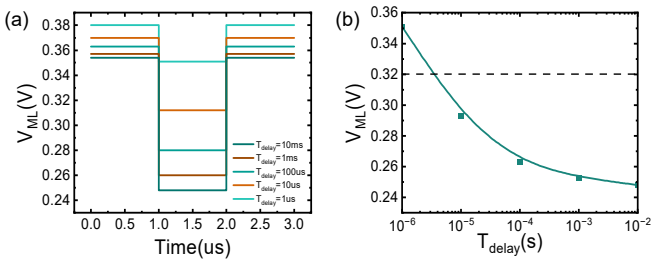

Fig. 10. (a) In the "mismatched" state, the V_{ML} voltage drop decreases as T_{delay} decreases. (b) The derived V_{ML} level, considering that the SA output flips when V_{ML} is less than 0.32V, so the hold time cannot be too short.

IV. Conclusions

This work provides insights into the mechanisms by which the internal trap behaviors of FeFET affects the reliability of search operations in TCAM. The results show that the defect density and the search delay time of FeFET are two key parameters that significantly modulate the V_{TH} shift characteristics of the FeFET device. The increase of defect density and the decrease of search delay time can cause significant V_{TH} shift characteristics of FeFET device. This modulation effect of V_{TH} directly alters the conductive properties of the TCAM cell during the search operation, which may flip an otherwise correct match/mismatch state. The state misclassification caused by the charge trapping/ detrapping behaviors can significantly degrade the search accuracy of the TCAM array, leading to an increase in the mis-match rate and ultimately affecting the functional reliability of the entire TCAM circuit.

Acknowledgements

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