Investigation of Reverse Recovery Failure Mechanism in SJ MOSFET with Increasing R_g

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***Abstract*— We investigated the reverse recovery failure mechanisms in a 650V-class Si superjunction (SJ) MOSFET with increasing gate resistance (R_g) by experiments and TCAD simulations. We analyzed that physical failure occurs when two phenomena take place simultaneously: voltage overshoot exceeding a critical value and non-uniform reverse recovery operation, meaning that reverse recovery at the edge termination is not completed even after reverse recovery at the active has terminated. As R_g increases, the magnitude of overshoot increases due to the current imbalance between the drain-source capacitance, the parasitic inductance and a large gate delay of the device under test. This large overshoot eventually leads to device failures. This study confirms that the magnitude of overshoot depends on the electrical characteristics of the active rather than the edge termination, while the physical failure occurs on the edge termination area because the large current density and the voltage overshoot are applied due to the non-uniformity. Finally, we proposed strategies to develop the edge termination with improved resilience against physical failures in conditions with similar overshoot events.**

***Keywords*— Superjunction MOSFET, Reverse Recovery, Gate Resistance, Failure Mechanism, TCAD Simulation**

I. Introduction

The SJ MOSFET is widely used in power applications because of a significantly lower specific ON-resistance (or conduction loss) than conventional power MOSFETs, owing to its charge-balanced p-/n-pillars structure [1-5].

In half-bridge or full-bridge circuit applications, the intrinsic body diode of the SJ MOSFET, formed by the p-/n-pillars, can function as a freewheeling diode. It can reduce the overall system size but, at the same time, imposes the necessity for the robustness of the body diode for the reliability of SJ-MOSFETs as well as the entire system. Generally, the body diode of the SJ MOSFET exhibits a higher reverse recovery charge (Q_{rr}) than that of the conventional power MOSFET due to the increased PN junction area resulting from its inherent pillar structure. This substantial Q_{rr} can lead to considerable voltage and current spikes caused by the rapid variations in voltage (dv/dt) and current (di/dt) in high-speed switching applications. The inadequate reverse recovery performance leads to increased power consumption and significant oscillations, which can result in serious reliability issues for the system [6-8]. Many studies have been conducted to improve reverse recovery characteristics by optimizing processes or designs at the device level [9-13]. Since the performance of the body diode depends not only on silicon design but also on package inductance in applications such as synchronous rectification, however, previous studies may have limitations in clarifying the actual body diode behavior. Therefore, it is necessary to consider parasitic components in the analysis not only at the device level but also from the package and equipment perspective [14].

On the other hand, in modern power electronics applications, there is a growing need for high efficiency combined with high power density, which represents a key trade-off issues in the design of power converters. One way to improve trade-off relation is to use soft switching topologies as known as the zero voltage/current switching. The main benefit of these topologies is to minimize the losses generated by the power devices during switching transitions. One of the key point in a design of soft switching topologies is to determine the optimal external gate resistance, considering its impact on the commutation behavior in order to set the delay or dead-time between the conduction of the switches [15-16].

We found the physical failures during the reverse recovery period with increasing R_g as shown in Fig. 1 and also found that the failure mechanism was not clearly understood based on the previous studies since the relation between the failures in the process of body diode reverse recovery and the physical parameters of SJ-MOSFET with changing R_g has not been sufficiently discussed. Therefore, in this study, we investigated the reverse recovery failure mechanisms in a 650V-class Si SJ MOSFET as R_g increased, using TCAD simulation with well-calibrated both device model and parasitic RLC.

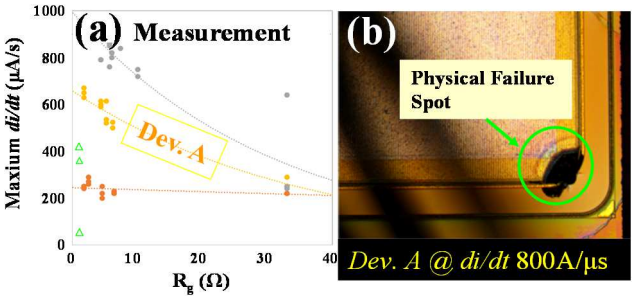


Fig. 1. (a) Measurement results show the maximum di/dt level is degraded with increasing R_g (Different colored dot = different device type). (b) Photo image of one of the SJ MOSFET that has experienced physical failure in device group A (Dev. A).

II. Simulation Method

Synopsys TCAD [17], a device simulator with mixed-signal mode and a thermodynamic model, was used for the simulations. The model used in this study was calibrated to within a 10% error range for the static characteristics of DBH's 650V-class SJ MOSFET, particularly demonstrating good prediction of the breakdown hot spot [18]. Also, the predictive accuracy for dynamic and ruggedness characteristics such as short-circuit withstand time and un-clamped inductive switching exhibits an error margin of approximately 15%. This indicates that the models used in the process and device simulations are suitable for evaluating reliability issues. Simulations were conducted with considering the parasitic RLC components proposed for the reverse recovery test circuit shown in Fig. 2.

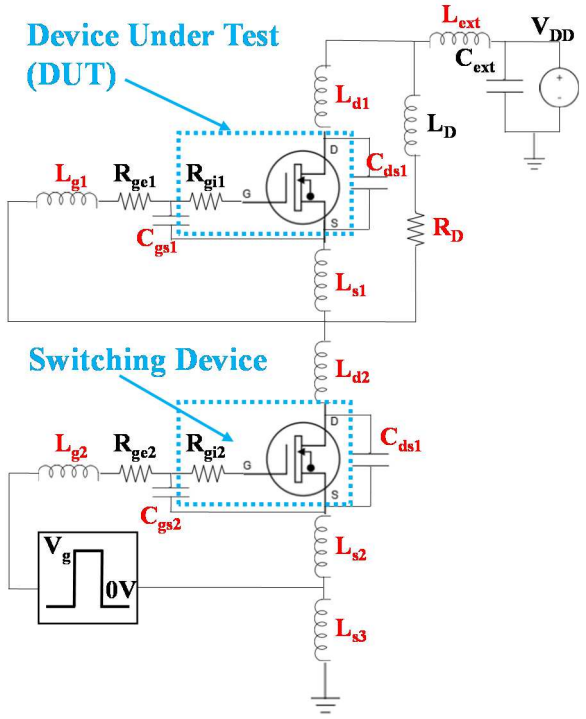
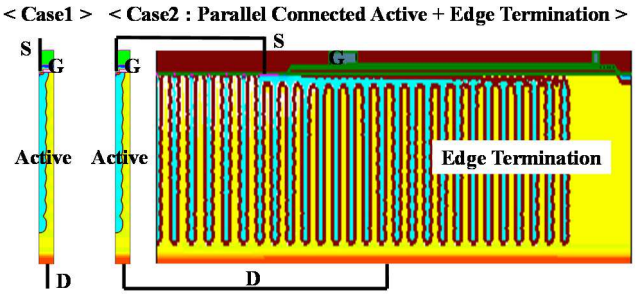


Fig. 2. Circuit diagram of the reverse recovery test with parasitic RLC used in the mixed-mode TCAD simulation (R_{gi1}=R_{gi2}, L_{d1}=L_{d2}, L_{s1}=L_{s2}, C_{ds1}=C_{ds2}, L_{g1}=L_{g2}, R_{ge1}=R_{ge2}, R_g=R_{gi}+R_{ge} (R_{gi}= intrinsic gate resistance, R_{ge}= external gate resistance)). Red-colored components indicate parasitics arising from packages and/or equipment that were not considered in previous studies. The values are not presented in this paper.



Device under test (DUT) has two configurations: (Case 1) Active only and (Case 2) parallel-connected active and edge termination in this simulation work. The switching device utilizes the active area only, where more than 90% of the gate charge is affected.

In this study, the device under test (DUT) employs two configurations: an active-only case and a parallel structure that includes both the active area and the edge termination area, as shown in Fig. 3. This simulation setup is used to assess the influence of each region during the reverse recovery period.

III. Results and Discussions

Fig. 4 shows that as R_g increases, the slope of *dv/dt* between the drain-to-source voltage (V_{DS}) of the DUT exhibits similar values under similar *di/dt* conditions; however, the tendency for overshoot voltage ($V_{overshoot}$) also increases. The inset of the Fig. 4 shows the case where parasitic RLC is not included in the simulation, and in this case, there is no increase in $V_{overshoot}$ with respect to R_g. Also, the overshoot characteristics and their voltage levels were observed to be similar for both the active-only case and the DUT configured with various designs of edge termination connected in parallel, as long as the cell design remained the same (not shown here). Since the active area occupies more than 95% of the total chip area, this indicates that the characteristics of the body diodes in the active pillars are significantly influenced by the total current shape (*di/dt*, *dir/dt*) during the reverse recovery period. In other words, the magnitude of the voltage overshoot does not significantly affect the edge termination itself; rather, it can be attributed to the reverse recovery softness of the active region and the influence of parasitic RLC.

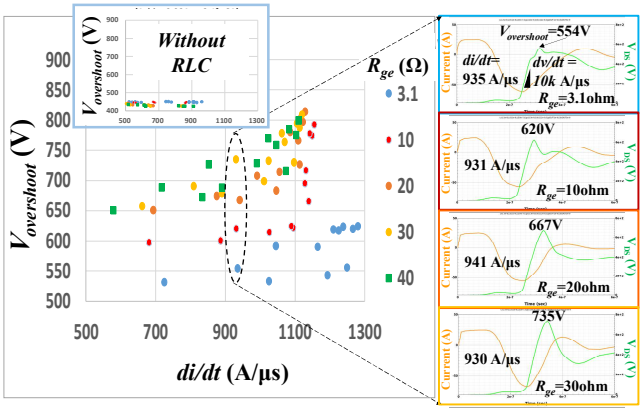


Fig. 3. Maximum magnitude of V_{DS} (=$V_{overshoot}$) of DUT (Case1) during reverse recovery operation as a function of R_g. The right insets display the current and V_{DS} (range of 0 to 800V) of the DUT under each R_g condition during reverse recovery operation, indicating that the border colors of the graph correspond to the colors of the data points. The left inset presents the simulation results under conditions without parasitic RLC components.

To provide a detailed understanding of the mechanism by which R_g affects overshoot, we compared the voltage and current behaviors of the DUT and SW devices during the reverse recovery operation time interval, as illustrated in Fig. 5, for varying values of R_g. Since the same chip is used for both the DUT and SW devices, their internal capacitances are identical, and the delay in the gate turn-on time of the SW device during the reverse recovery period occurs solely due to the large R_g. During the period from t_1 to t_2, all of body diode reverse recovery charge (Q_{rr}) of the DUT is consumed to respond to *di/dt*. After that, since the parasitic inductance,

especially the large L_{ext}, cannot respond to the large *dir/dt* which changes the sign of the current slope over time, the drain-source capacitance (C_{DS}) current of the package responds while the V_{DS} of the DUT switches to V_{DD}. At this point, when R_g is small, the V_{GS} of the DUT responds quickly, allowing the channel current of the DUT by V_{GS} to reach the threshold voltage (V_t) of DUT at t_3, and the current of C_{DS} alternately responds to the current required after t_2. Accordingly, the V_{DS} of the DUT settles to V_{DD} without large overshoot. However, for DUTs with large R_g, since the turn-on response of V_{GS} is delayed, the channel current of the DUT does not respond to the current required after t_2, so the voltage at the drain node of the DUT increases as it continues to respond to *dir/dt* with the charge of the C_{DS}. A large voltage overshoot due to the increase in R_g is interpreted by the above mechanism.

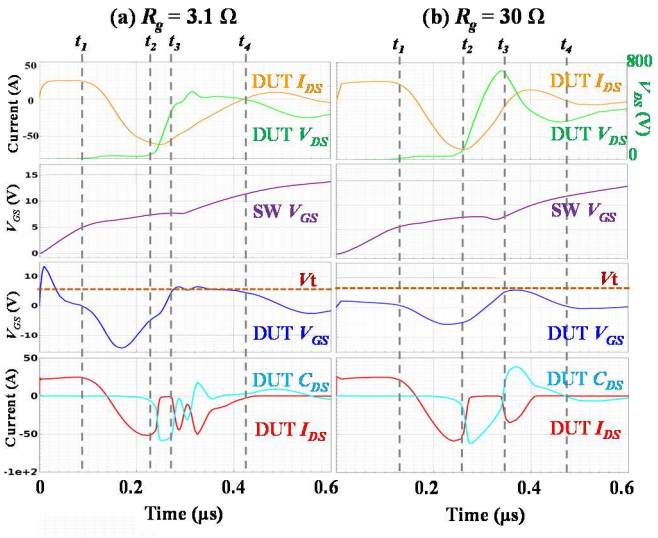


Fig. 4. Timing diagrams of the reverse recovery operation with varying R_g ((a) R_g = 3.1 Ω, (b) R_g = 30Ω). (t_1 = SW reaches V_t, t_2 = Q_{rr} in DUT consumes all, t_3 = DUT reaches V_t, t_4=V_{DS} in DUT settles to V_{DD}.)

In contrast, it remains difficult to determine the causes of physical failures by analyzing only the active region, as demonstrated in Case 1 of Fig. 3, despite the increase in R_g resulting in a rise in $V_{overshoot}$. Because, as shown at t_3 of Fig. 5(b), the occurrence of $V_{overshoot}$ corresponds to the state when no current is flowing through the DUT channel; specifically, this refers to the normal off-state operation of the SJ-MOSFET. Therefore, when considering only the active region, as shown in Fig. 6, although a significant $V_{overshoot}$ occurs, the rise in lattice temperature is not monitored within the active area. Alternatively, Case 2 of the DUT indicates that the maximum lattice temperature during the reverse recovery process can change based on the specific type of edge termination used. In this case, a smaller R_g with smaller $V_{overshoot}$ results in a reduced increase in the maximum lattice temperature for Case 2.

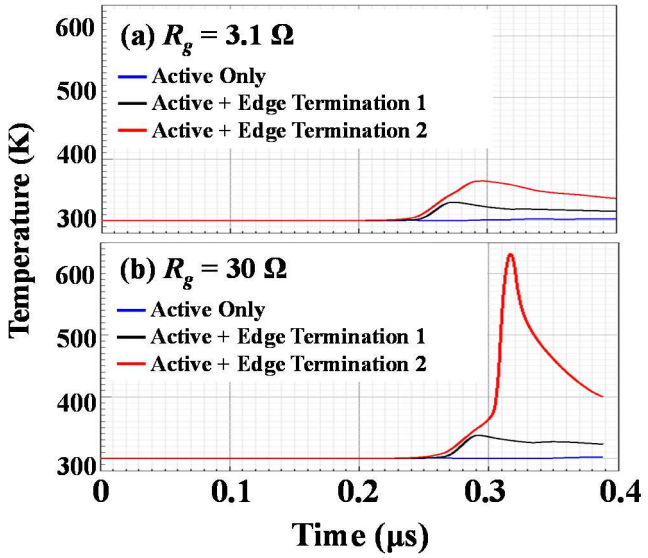


Fig. 5. Simulation results of the maximum lattice temperature for each DUT condition with varing R_g. (a) R_g = 3.1Ω with $V_{overshoot}$ = 554 V and (b) R_g = 30 with $V_{overshoot}$ = 735 V that it is the same for the different DUTs when R_g is set to the same value.

In Fig. 7, we investigate how edge termination affects the increase in lattice temperature during the reverse recovery operation. For the case where R_g is 30 Ω, the figures show the current density, electric field, and lattice temperature contours at V_{DS} = $V_{overshoot}$. At this time, edge termination 2 exhibits a lighter p-type doping concentration near the source contact compared to edge termination 1. This results in a slower recombination rate of holes generated at the edge termination relative to the active region, leading to sustained current flow. Consequently, a substantial amount of current becomes concentrated near the source contact of the edge termination. Due to the inability to eliminate the generated holes, as is done in the active region, the pillars of the edge termination are not fully depleted. The voltage overshoot becomes concentrated in the upper region, resulting in a high electric field strength in that area, which reaches approximately 0.3 MV/cm, exceeding the critical electric field of silicon. Unfortunately, as the areas of current flow and high electric field overlap in this region, as shown in the insets of Fig. 7, they experience increased electrical stress. This electrical stress may lead to the generation of a large number of excess carriers, which could ultimately result in physical failure due to thermal runaway. In conclusion, when a significant overshoot occurs due to the characteristics of the active region and parasitic RLC elements, a greater difference in the excess hole removal speed between the edge termination and the active region increases the probability of physical failure. Furthermore, it can be interpreted that physical failures are more likely to occur near the source contact of the edge termination rather than in the active region. Therefore, designing the edge termination to achieve a similar excess hole removal rate as that in the active region implies that the probability of avoiding physical failure, even under identical overshoot conditions, is significantly increased.

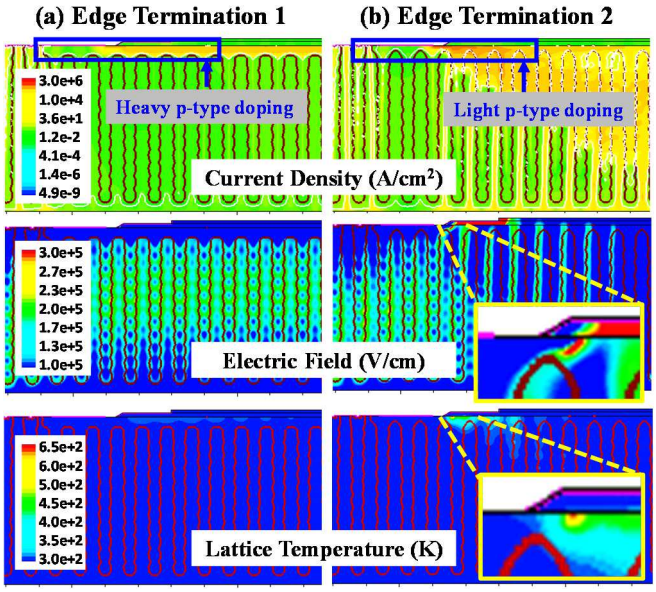


Fig. 6. Comparison of the current density, electric field, and lattice temperature for two different edge termination designs in the Case 2 with R_g =30Ω at $V_{overshoot}$ = 735V. The inset shows an enlargement of the area where the lattice temperature exceeds 600 K in edge termination design 2. Each edge termination has a different doping profile near the source contact, as shown in Fig. 7(a). Edge termination design 1 includes a higher concentration of p-type doping compared to edge termination 2.

IV. Conclusion

In this study, we investigated the reverse recovery failure mechanisms in a 650V-class Si SJ MOSFET as R_g increases, utilizing both experimental methods and TCAD simulations with the proposed circuit scheme with parasitic components. Our analysis shows that physical failure occurs when a voltage overshoot due to the active region and parasitic RLC and a non-uniform reverse recovery process in edge termination take place at the same time. This indicates that the immunity to the physical failure can be achieved by optimizing the pillar design in the active region for soft recovery or by sufficiently reducing parasitic RLCs. And, regardless of whether these optimization are satisfied, it is crucial to design the edge termination to have the closely matched reverse recovery performance to that of the active region. These results and analytical methods regarding reverse recovery failures can be applied to not only other V-class SJ MOSFETs but also devices where the different semiconductor material are used.

Acknowledgment

This work was supported by the Industrial Strategic Technology Development Program (00144306) funded by the Ministry of Trade, Industry & Energy (MOTIE), South Korea and Eco-friendly & High-efficiency 1200V SiC MOSFET Development for Commercialization in Energy Industry (00431820), South Korea.

References

[1] D. J. Coe, “High voltage semiconductor device,” U.S. Patent 4 754 310, Jun. 28, 1988.

[2] X. Chen, “Semiconductor power devices with alternating conductivitytype high-voltage breakdown regions,” U.S. Patent 5 216 275, Jun. 1, 1993.

[3] F. Udrea, G. Deboy, and T. Fujihira, “Superjunction power devices, history, development, and future prospects,” *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 713–727, Mar. 2017.

[4] G. Deboy, N. Marz, J. P. Stengl, H. Strack, J. Tihanyi, and H. Weber, “A new generation of high voltage MOSFETs breaks the limit line of silicon,” *in IEDM Tech. Dig.*, Dec. 1998.

[5] T. Fujihira, “Theory of semiconductor superjunction devices,” *Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes*, vol. 36, no. 10, pp. 6254–6262, Oct. 1997.

[6] G. Yao, M, Qiao, Z, Shi, J. Li, and B. Zhang, “Fabrication and Optimization of a High-Reliability 700V Super-Junction MOSFET with Segmented P-Buried RESURF Termiantion,” *in Proc. IEEE Int. Symp. Power Semiconductor Devices IC’s (ISPSD)*, June 2024.

[7] Z, Yang, J, Zhu, X. Tong, W. Sun, F. Bian, Y. Tian, Y. Zhu, P. Ye, Z. Li, and B. Hou , “Investigations of Inhomogeneous Reverse Recovery Behavior of the Body Diode in Super Junction MOSFET,” *in Proc. IEEE Int. Symp. Power Semiconductor Devices IC’s (ISPSD)*, May 2017.

[8] M. Ren, M. Yang, S. Zhong, C. Xie, Z. Li, W. Gao, J. Zhang, and Bo. Zhang, “Failure Analysis and Improvement of the Body Diode in Superjunction Power MOSFET,” *in Proc. IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, July 2018.

[9] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, “Investigation on the self-sustained oscillation of superjunction MOSFET intrinsic diode,” *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 605–612, Jan. 2019.

[10] Z. Lin, Q. Yuan, S. Hu, X, Xhou, J. Zjou, and F. Tang, “A Simulation Study of Novel Superjunction MOSFET Embedded With an Ultrasoft Reverse-Recovery Body Diode,” *IEEE Trans. Electron Devices*, Vol. 66, No. 5, 2019.

[11] M. Huang, R. Li, Z. Yang, Y. Ma, Y. Li, X. Zhang, and M. Gong, “A Multiepi Superjunction MOSFET With a Lightly Doped MOS-Channel Diode for Improving Reverse Recovery,” *IEEE Trans. Electron Devices*, Vol. 68, No. 5, 2021.

[12] P. Li, R. Ma, Z. Yang, J. Guo, Z. Lin, and S. Hu, “A Novel Approach to Suppress the Inhomogeneous Reverse Recovery Behavior of the Body Diode in Superjunction MOSFET,” *in Proc. IEEE Int. Conf.Solid-State Integr. Circuit Technol. (ICSICT)*, 2022.

[13] P. Li, R. Ma, Z. Yang, C. Li, J. Shen, Z. Lin and S. Hu, “Superjuction MOSFET with an N-dot region in the P-pillar for Soft Reverse Recovery,” *in Proc. IEEE Int. Symp. Power Semiconductor Devices IC’s (ISPSD)*, June 2024.

[14] R. Jagannathan, H.-P. Hoenes, and T. Duggal, “Impacts of package, layout and freewheeling diode on switching characteristics of super junction MOSFET in automotive DC-DC applications,” *in Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst. (PEDES)*, Dec. 2016, pp. 1–6.

[15] F. D. Domenico, and M. Rene, ZVS Phase Shift Full Brridge : CFD2 Optimized Design, Infineon, March 2013.

[16] W. Yang, P. Geng, Y. Wang, P. Zhang, and Z. Xu, “The Affect of Dead-time to ZVS Phase-Shift Full-bridge Converter,” *in Proc. IEEE Int. Conf. Elect. Machine and Systems (ICEMS),* Oct, 2015.

[17] Sentaurus TCAD Tools Suite. V-2023.12. Synopsys.

[18] J. Lee, J. M. Kim, M. B. Pyun, W. K. Cho, K. Y. Ko, and H. Nah, “3D Simulation Method to Predict Breakdown Voltage of Complex Large-Scale Ring Corner in SJ MOSFET,” in Proc. IEEE Int. Conf. Simulation of Semiconductor Processes and Devices (SISPAD), Sep. 2023.