A Comprehensive Assessment of Scattering and Ballistic Effects on Sub-3nm Nanosheet FET: A Quantum Transport Simulation

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***Abstract* -- The scaled geometry of vertically stacked Nanosheet FET (NSFET) is now in adaptable stage. However, the device geometry and inherent physical charge transport phenomenon is not yet well captured by the simulation studies. In some sense, the conventional drift-diffusion transport is not adequate and requires the inclusion of coupled Boltzmann transport equation (BTE). Further, at some instant, the ballistic model needs to be incorporated to capture the transport mechanism, where the mean-free path of the carrier is larger. To overcome this dilemma, in this work, we extensively analyzed the scattering effect on NSFET by employing different models viz (*i*) phonon scattering (PH); (*ii*) surface roughness (SR); (*iii*) coulomb scattering (CO). Further, we simulated the same baseline device considering the ballistic model using *Sentaurs*-QTX simulations. All the models are well-mapped with different geometrical dimensions and found that the cumulative effects of scattering events are rightly capturing the carrier transport, instead considering the ballistic model.**

Keywords: *Nanosheet field-effect transistor, Scattering, surface roughness, Ballistic transport.*

I. INTRODUCTION

Nanosheet Field-Effect Transistors (NSFETs) offer several critical advantages, particularly in the context of advanced technology nodes where electrostatic control, cell-area, and short-channel effects become major concerns [1]. In contrast, the vertical stacking of the sheets/channels forms a more complex device resistance/capacitance framework, unlike the conventional planar devices. Therefore, the charge transport mechanism is not simply governed by the conventional drift-diffusion transport mechanism. In general, the transport is governed by various scattering events, where the charge carrier movement (e.g., mobility) gets affected by geometrical and bias conditions. As in NSFET, the sheet thickness is ~50 Å, which generates multi/sub band valleys in the conduction band. Under these conditions, carrier transport is strongly affected not only by sub-band occupation but also by various scattering mechanisms that degrade mobility and limit drive current [2,3]. Among them, the dominant scattering is surface roughness (SR) scattering, which intensifies at the channel-dielectric interface due to enhanced confinement. On the other hand, phonon scattering, particularly through interactions with both acoustic and optical phonons; and Coulomb scattering from charged impurities and interface traps [4] are less dominant because most the current carrying charges are lying near the surface. These mechanisms collectively impacted on the transport characteristics. In contrast, the ballistic transport mechanism, governs the charges of larger mean-free path and sometimes inadequately predicted the actual electrostatics. Thus, in this paper, we comprehensively explored the various scattering mechanisms in NSFET under <110> orientation.

II. DEVICE STRUCTURE AND TCAD SETUP

A three-stack NSFET is considered as a baseline device for this simulation study as shown in fig. 1(a) whereas fig.1(b) depicting the geomatric dimension of individual nanosheet. Sentaurus TCAD is used for device simulation to capture the scattering phenomenon governing the actual carrier transport.

The baseline device is well-calibrated in fig.2 against the experimental data [5]. During the structural design, the channel transport direction was aligned along the ⟨110⟩ crystallographic orientation, while the top surface orientation was set to ⟨100⟩ to exploit enhanced carrier mobility and other favorable device characteristics, as reported in [6]. The source/drain regions are uniformly doped, whereas the extension regions are equipped with Gaussian doping to mimic the realistic scenario. All other geometrical dimensions are listed in Table I.

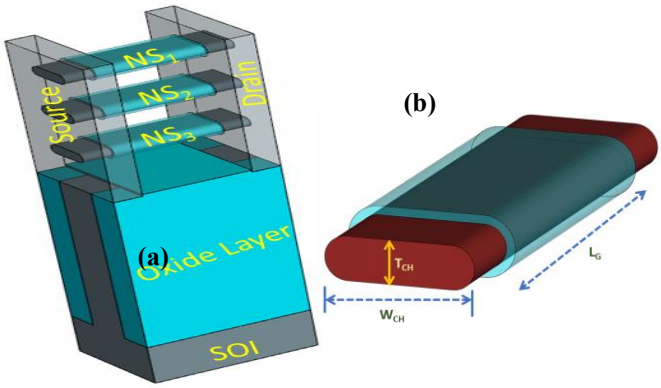

Fig.1 (a) Schematic of three stack nanosheet transistor; and (b) cross section of nanosheet illustrating geometry- parameters.

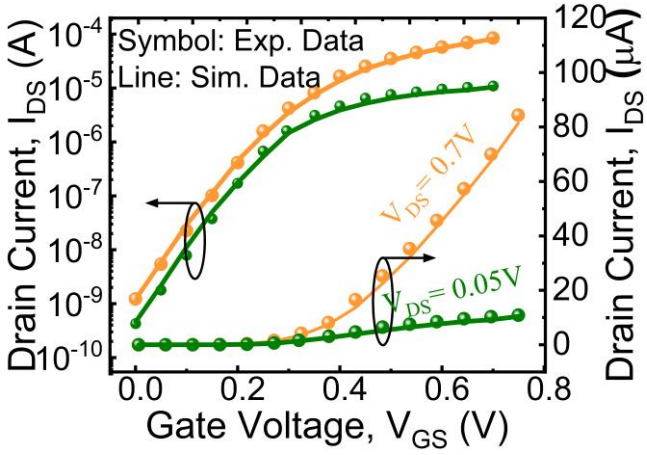

Fig. 2 The calibrated transfer characteristics against the experimental data [5].

For the electrical simulations, quasi-ballistic carrier transport and quantum confinement effects were incorporated by coupling the drift-diffusion (DD) model with the sub-band-based Boltzmann transport equation (sub-band-BTE) using the Sentaurus–QTX module. Each nanosheet is treated as a nonlocal simulation domain. To capture the overall device behavior, three parallel simulations were performed—one for each nanosheet—and the total current was obtained as the

TABLE I

DEVICE PARAMETERS OF THE REFERENCE DEVICE AND THEIR RANGE FOR DATASET GENERATION

Parameter	Symbol	Value/Range
No. of Nanosheet	N	3
Thickness of SiO_2	t_{ox}	0.6nm
Thickness of HfO2	t_{hfo2}	1.5nm
Channel Direction	<abc>	110
Channel Length	L_G	16
Chennel Widht	W_{CH}	10-15nm
Channel Thichness	T_{CH}	3-5nm
Gate Workfunction	WF	4.624 ev

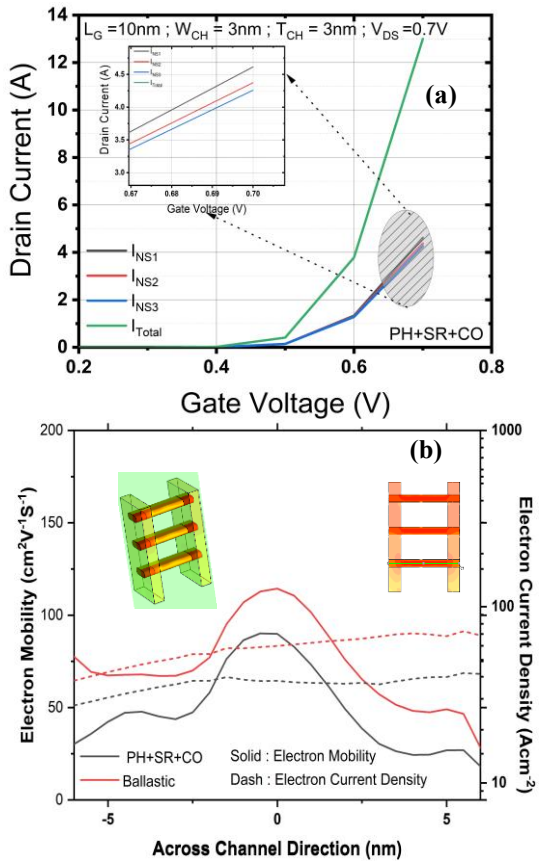

Fig. 3 (a) impact of individual nanosheet on the total current of transistor. (b) cutline profile of the electron mobility and electron current density for the lower sheet measured across the channel direction.

summation of individual sheet currents. This approach also contributed to improved convergence and reduced computation time, as demonstrated in Fig. 3(a). To solve the BTE, a total of 10 sub-bands were considered, while six sub-bands were included when accounting for scattering mechanisms. Incorporating scattering in the simulation

revealed a degradation in effective mobility across the channel, leading to a reduction in current density. This impact is illustrated in Fig. 3(b), which compares the output characteristics under ballistic and scattering-limited transport regime.

III. RESULAT AND DISCUSSION

In this paper, we extensively analyzed the significance of various scattering models over ballistic models used in TCAD simulations. Fig. 4(top) illustrates the influence of nanosheet thickness (T_{CH}) on the transfer characteristics, under both ballistic and scattering-limited transport regimes. The simulations were performed for constant channel length mechanisms exacerbates this degradation, resulting in a further reduction in drive current and an increase in the required threshold voltage. Similar trends were observed in the behavior of drain-induced barrier lowering (DIBL) and to achieve the iso-OFF current of 10pA, the equivalent gate work function is observed (Fig.4 (bottom-right)). Subsequently, the impact of gate length (L_G) scaling on

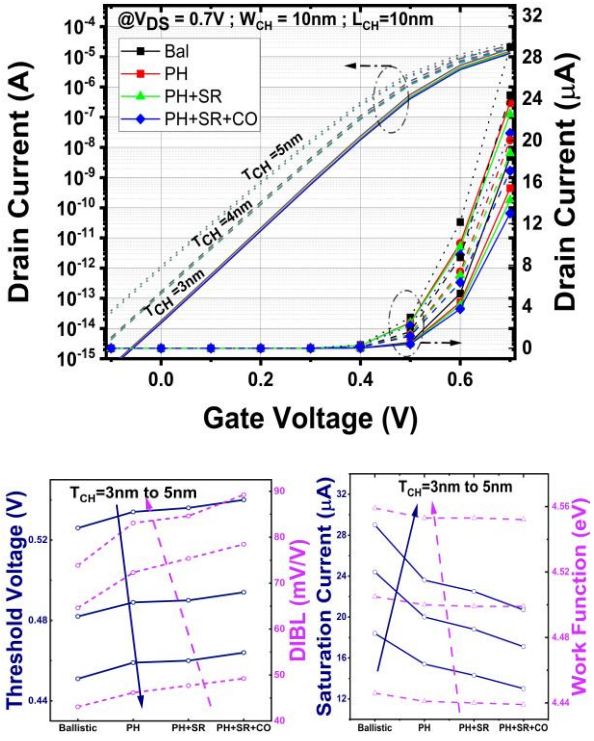

Fig.4 (top) Impact of the channel thickness of nanosheets on the transfer characteristics of the transistor on log (left) and linear (right) scale. (bottom) Illustrate the variation on different figure of merits such as threshold voltage, DIBL, Saturation current and work function DIBL due the different scattering mechanism for W_{CH} =10nm, L_{CH} =10nm and V_{DS} of 0.7V.

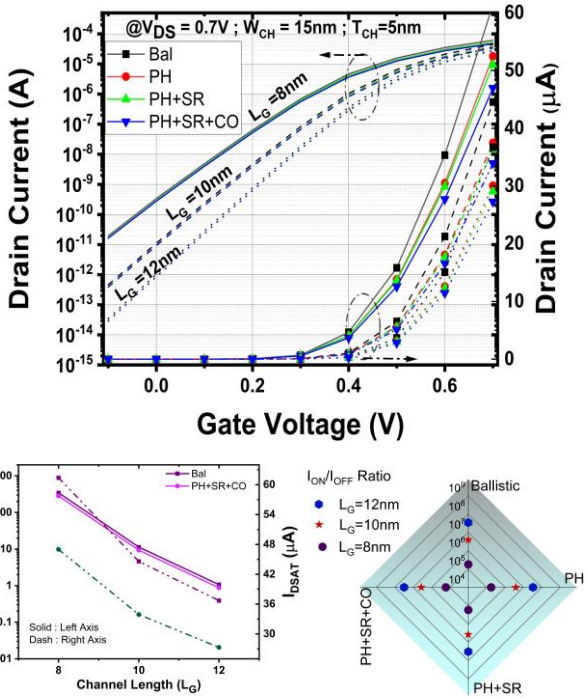

Fig.5: (top) Impact of the channel length of nanosheets on the transfer characteristics of the transistor on log (left) and linear (right) scale at V_{DS} of 0.7V (bottom-left) impact on the OFF and ON state current, (bottom-right) Radar representation of current ratio as a function of different scattering events and TABLE II: Illustrate the impact on different figure of merits of transfer characteristics due the ballistic and scattering mechanism as a function of L_G.

device performance is investigated with the transfer characteristics, for a fixed sheet thickness and width (Fig.5). As the gate length decreases, the device exhibits a lower threshold voltage. However, it shows an increase in DIBL. This results in an increased off-state current and thereby reducing the ON/OFF current ratio (Fig. 5(bottom-right)). The key performance metrics under both ballistic and scattering-influenced conditions (PH, SR, and CO) are summarized in Table II. Another critical design parameter is the channel width, which directly affects the current drive capability of the device. As depicted in Fig. 6 (top), where wider channels result in higher saturation current and reduced threshold voltage. However, the inclusion of scattering mechanisms leads to increased DIBL and a positive shift in the threshold voltage compared to the ballistic case, as shown in Fig. 6 (bottom).

IV. CONCLUSION

Using well-calibrated TCAD models, we extensively analyzed the various scattering models (PH, SR, CO) and ballistic models for capturing carrier transport in Nanosheet

FET. The results reveal that the ballistic model over-estimates the results to some extent owing to the influence of pinch-off condition. Thus, the proposed work provides a reliable simulation guideline for capturing the scattering phenomenon at sub-3nm node.

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TABLE II

THE KEY PERFORMANCE METRICS UNDER BOTH BALLISTIC AND SCATTERING-INFLUENCED CONDITIONS (PH, SR, AND CO)

@V_{DS} =0.7V T_{CH} = 5 nm W_{CH} =15nm	L_G (nm)	V_{TH} (V)	I_{DSAT} (μA)	I_{DOFF} (PA)	CR (X 10^6)	DIBL (mV/V)	SS (mV/dec)
Ballistic	12	0.436	36.7	1.06	34.40	63.07	68.6
	10	0.398	44.6	11.32	3.94	110.76	73.7
	8	0.331	61.4	343.3	0.18	189.23	83.5
PH+SR+CO	12	0.447	27.3	0.87	31.26	64.61	68.7
	10	0.411	33.9	9.34	3.63	110.76	73.8
	8	0.343	47	281.30	0.17	193.84	83.7

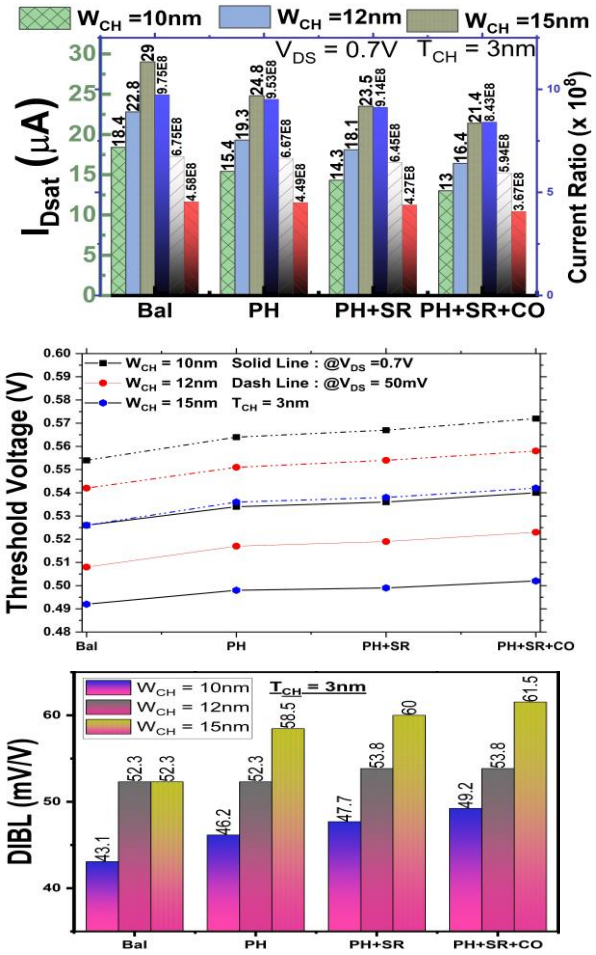

Fig.6: Illustrate the impact of ballistic and different scattering mechanisms on various figures of merit derived from the transfer characteristics, due to the width of channel for constant TCH of 3nm and WCH of 10nm at VDS of 0.7V.

REFERENCES

[1] A. Veloso et al., "Vertical Nanowire and Nanosheet FETs: Device Features, Novel Schemes for Improved Process Control and Enhanced Mobility, Potential for Faster & More Energy Efficient Circuits," 2019 *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2019, doi:10.1109/IEDM19573.2019.8993602.

[2] A. Dixit, et al. "Mobility and intrinsic performance of silicon-based nanosheet FETs at 3 nm CMOS and beyond." *Solid-State Electronics* (2025): 109172, doi:10.1016/j.sse.2025.109172.

[3] T Dutta et al. "Predictive Simulation of Nanosheet Transistors Including the Impact of Access Resistance." *2024 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*. IEEE, 2024.

[4] R. Kaur and N. R. Mohapatra, "Comprehensive Analysis of Sheet Thickness Scaling on the Performance of Nanosheet nFETs," in *IEEE Transactions on Electron Devices*, vol. 71, no. 5, pp. 2856-2862, May 2024, doi: 10.1109/TED.2024.3377606

[5] N. Loubet *et al*., "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," *2017 Symposium on VLSI Technology*, Kyoto, Japan, 2017, pp. T230-T231, doi: 10.23919/VLSIT.2017.7998183.

[6] A. Dixit *et al*., "Unravelling the Impact of Random Dopant Fluctuations on Si-Based 3nm NSFET: A NEGF Analysis," *2024 IEEE 24th International Conference on Nanotechnology (NANO)*, Gijon, Spain, 2024, pp. 5-8, doi: 10.1109/NANO61778.2024.10628880.

[7] T. Liu et al. "The study of electron mobility on ultra-scaled silicon nanosheet FET." *Physica Scripta* 99.7 (2024): 075410.