Dual-Mode Reconfigurable Core-Shell Nanowire Feedback FET with Tunable Logic-Memory Windows: Proposal and Performance Optimization

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***Abstract*— We introduce a reconfigurable core-shell nanowire feedback field effect transistor (RFBFET) that addresses the limitation of thermionic subthreshold swing and the cost of duplicating N and P-type device inventories in a single architecture. We performed extensive simulations that include quantum confinement and nonlocal tunnelling for dual mode operations (both N-type and P-type by changing the biasing on gates and source/drain) show sub threshold slopes of less than 2mV dec^{-1} at $|V_D|$ = 1V, ON currents of 2.6 to 4.0 µA µm^{-1}, and I_{ON}/I_{OFF} ratios >10^7. Systematic sweeps of spacer length (L_i) and Silicon thickness (R_{Si}) modulate the intrinsic hysteresis window from 0.15V (steep slope logic mode) to 2.3V (non-volatile latch mode) with <10 % penalty in drive current, enabling a continuum of logic to memory functionality on a shared process flow. Compared with state of the art three stack nanosheet GAAFETs, the proposed device reduces active power by 35 %, halves threshold variability, and eliminates separate N/P patterning steps. These results establish RFBFETs as a compelling platform for advanced technology nodes, monolithic 3D integration, and energy efficient in-memory compute fabrics.**

Keywords— Reconfigurable, Dual-Mode, Feedback FET, Core-Shell, Nanowire, Steep-Subthreshold, Hysteresis, Negative Differential Resistance, Variability

I. Introduction

Complementary MOSFET technology is facing a multidimensional impasse. First, the 60 mV dec^{-1} Boltzmann limit prevents further voltage scaling [1] [2]; at the 2 nm node, nanosheet GAAFETs already leak a significant fraction of their nominal drive current [3] [4], and negative capacitance [5] or tunnel FET [6] solutions introduce material and reliability risks. Second, variability is rising. Channel doping must be frozen below 5×10^{17} cm^{-3} to suppress random dopant fluctuations [7] [8], yet threshold control then hinges on nanometre-level line edge roughness in fin or sheet width [9], an increasingly unmanageable burden for EUV lithography [10]. Third, memory and logic remain physically and energetically disjoint: every bit toggled in SRAM [11] or flash costs two orders of magnitude more energy to move than to compute, throttling AI and edge workloads [12]. Finally, the foundry cost of maintaining mirror N and P-type process decks scales poorly with the proliferation of back-end tier stacking now envisioned for logic near memory architectures.

The reconfigurable core-shell nanowire feedback FET [13] (RFBFET) replaces chemical polarity with electrostatic polarity, and supplements the external gate with an internal, self-induced field that enforces steep slope switching [14]. The doped silicon core is wrapped by a pair of buried "core field" plates that are biased to opposite potentials. In equilibrium, the resulting valley–hill pair pinches off conduction; when the plates swap polarity, electrons and holes exchange roles, instantly converting the device between N and P mode. Because the feedback barrier [15] is generated inside the silicon body rather than at the oxide interface, the subthreshold swing is linked to the ratio of cavity capacitance to inversion capacitance, not to kT/q and can be driven well below 15 mV dec^{-1} [16] without resorting to tunnelling currents or ferroelectric phases.

Crucially, the strength and phase delay of the feedback are geometric knobs: the intrinsic region length (L_i) and core radius (R_{Si}). Short, thin wires act as near zero hysteresis logic switches while long, thick wires behave as non-volatile latches with >2V memory margin, yet all share the same mask set and thermal budget. This geometric programmability circumvents the variability crisis, no separate process for N and P-type devices, no ferroelectric crystallization and collapses the distinction between logic and storage into a single device class. Benchmarking against projected IRDS targets, the RFBFET meets high-performance drive current at 35 % lower supply voltage, reduces standby power by two orders of magnitude, and removes the need for dual flavour FEOL splits. These attributes uniquely qualify the device for heterogeneous 3D integration, near sensor inference engines, and run-time reconfigurable security fabrics where circuit level polymorphism is paramount.

II. Simulation Methodology and Device Specifications

The proposed device is a Reconfigurable Dual-Mode Core-Shell Nanowire Feedback FET, which is simulated with Synopsys Sentaurus TCAD, considering the calibrated models based on Feedback FET or Z2FET. RFBFET consists of NPNP doping profile with N-type source and P-type drain. The length of the source/drain regions is kept at 30nm, whereas both the Control/Feedback channels (CF-Ch) and the lightly doped center region are 20nm long. The operability of the device remains the same even with bigger regions, but the individual channel lengths should be kept > 17nm to reduce the tunneling probability across the abruptly doped regions. Across the cross-section of the proposed device, it is divided into three regions: the inner oxide with embedded inner gates for CF-Ch, the center Silicon channel of thickness 10nm and outer oxide/spacers. The thickness of inner and outer oxides is kept at 2nm, which helps in minimizing the tunneling

across the gate oxides. The bias is applied to the inner/outer N-gates (G_N1 and G_N2) for the N-type mode and to the inner and outer P-gates (G_P1 and G_P2) for the P-type operation. The models used for the simulation include the doping-dependent Scholey-Read-Hall recombination, doping and field-dependent mobility, trap-assisted tunneling, density gradient for quantum corrections, Fowler-Nordheim tunneling, hot carrier injections and non-local Band-to-band tunneling.

III. Results and Discussion

We proposed a cylindrical, doped silicon (as shown in Fig. 1(a)) (R_{Si}=8-12nm) between the core and shell SiO_2 (2nm), two azimuthally separated inner gates, and an outer gate-all-around shells (Fig. 1(b)). The proposed RFBFET acts as N-type when the drain/Ngates (G_N1 and G_N2) are biased with 1V along with grounded Pgates (G_P1 and G_P2) and acts as P-type when the source/Pgates (G_P1 and G_P2) are biased with -1V along with grounded Ngates (G_N1 and G_N2). Fig. 1(c) shows the potential along the device length under three bias conditions for the N-type device operation. OFF-state illustrates the potential well adjacent to the potential peak due to the doping of the respective regions [1-2] of the RFBFETn, which prevents the flow of charge carriers across the device. The ON-state shows that both Ngates are driven positive, the potential becomes nearly flat, resulting in the entire channel being pulled into strong inversion [3]. Such inversion of the channel pulls up the valley potential, allowing the electrons to sweep across the low-doped region to the N-type CF-Ch where the minority carrier flow in the opposite direction, resulting in a decrease in the peak potential, leading to a self-feedback mechanism resulting in a steep increase in carrier transport.

Fig. 2(a) & (b) show the energy band diagram and carrier concentration of RFBFETp for different operating conditions, which are similar to the RFBFETn. As discussed in the above sections, for RFBFETp, the applied bias on the G_P1 and G_P2 inverts the channel, allowing holes to move towards the P-type CF-Ch from where the minority carriers flow towards the inverted region across the low-doped region, resulting in the self-feedback mechanism. The movement of carriers across the device for both the operating modes can be confirmed from Fig. 2(b). Fig. 2(c) & (d) illustrate the I_{DS}-$|V_G|$ characteristics in log and linear scale, respectively, for both RFBFETn and RFBFETp. Inter-gate Spacer length (L_i), silicon thickness (R_{Si}) for RFBFETn are 20nm & 10nm, and for RFBFETp are 25nm & 11nm, while keeping the doping for L_{G1} (N_{AL1}), and L_{G2} (N_{AL2}) are kept the same as $2.5\times10^{19}cm^{-3}$. These parameters are chosen to show the maximum hysteresis window [3-4] (V_{Hys}) for both the mode operations (V_{Hys}=2.11V for RFBFETn and V_{Hys}=2.47V for RFBFETp) within the used parameter ranges. On the semi-logarithmic plot both RFBFETn (black) and RFBFETp (red) exhibit abrupt drain-current switching in the forward gate sweep (blue arrows); the measured average sub-threshold slope in each polarity is <1 mV dec^{-1} at $|V_{DS}|$ = 1 V, a six-fold improvement over state-of-the-art nanosheet GAAFETs and a full order of magnitude better than production FinFETs at similar gate lengths. The OFF-current floor remains pinned below 5 pA μm^{-1}, thanks to the source-side spike suppressing hole injection in P-mode and electron injection in N-mode. When the gate voltage is swept back (green dashed arrows) the devices do not immediately retrace their forward paths but remain latched in the low current state until the gate bias crosses the opposite polarity threshold, giving rise to a non-volatile memory window highlighted by the orange markers. The hysteresis in RFBFET modes (both N-type and P-type) exists due to the fact that the inverted CF-Ch rises to a higher concentration of the minority carriers, which requires a larger opposite bias to dial down the minority concentration. The proposed device also exhibits a higher ON-current, which is proportional to the Silicon channel thickness (R_{Si}), providing better gain to build efficient analog circuits.

Fig. 3 probes the two structural knobs that dominate the electrostatic feedback of the core shell nanowire feedback FET: the length of the intrinsic cavity between the two buried feedback gates (L_i) and the silicon thickness (R_{Si}). Even with variation of L_i, both operating modes remain turned ON without any hysteresis throughout the $|V_G|$ range for R_{Si}=8nm. However, for R_{Si}=12nm, all the I_{DS}-$|V_G|$ characteristics show hysteresis for RFBFETn throughout the L_i range, but devices with L_i=10 & 15nm, RFBFETp remained turned ON without any hysteresis [Fig. 3(a) & (b)]. This is due to the default use of metal (aluminum), which modifies the carriers in the L_{G1} (N_{AL1}) because of a lower work function than the affinity of the region. Hysteresis also depends on the L_i, which controls the coupling between the L_{G1} and L_{G2}, such that lower L_i can disrupt the device behaviour irrespective of the doping and R_{Si} as shown in Fig. 3(c) & (d). The underlying reason behind the decrease in the hysteresis window as L_i increases is due to the increase in the separation between the source side potential valley and the drain side potential hill; the electrostatic lever arm therefore becomes larger and the feedback loop requires a proportionally higher gate bias to invert the valley. At the same time, the series resistance of the cavity rises, which is reflected in a modest reduction of the ON-current. With the variations of R_{Si}, a larger L_i partially decouples the two buried gates, reducing their mutual capacitance and dampening the radial screening, so that the memory window becomes less sensitive to R_{Si} while the on current continues to scale almost linearly with radius.

Fig. 4 maps the multi-dimensional design space of the RFBFET onto three key figures of merit i.e., ON-current, ON-current to OFF-current ratio, and hysteresis window, with the extension dopants for the lateral N_{AL1}/N_{DL2} segments fixed at 2.5×10^{19} cm^{-3} so that source/drain resistance remains constant while the L_i and R_{Si} are swept. The results in panels Fig. 4(a) and (b) reveal an almost linear growth of the ON-current with increasing radius for both carrier polarities, but the slope is subtly modulated by L_i. The trend is expected: the inversion sheet wraps the cylindrical sidewall, so the electrically active cross section scales with R_{Si} rather than the quadratic area law of planar devices, yielding a quasi-linear improvement in channel charge and hence in ON-current. Fig. 4(c) and (d) clarify that, at $R_{Si} \leqslant 9$ nm, the OFF-current is high enough to keep the ON-current to OFF-current ratio lowest regardless of L_i. Once the radius crosses 10 nm, the ON-current climbs faster than the OFF-current, and the ratio balloons explosively, surpassing 10^7 for Li $\geqslant$ 20 nm in both polarities. The almost vertical rise at $R_{Si} \approx 11$ nm marks the point where the GAA electrostatics transition from quantum confinement dominated to classical screening dominated: the radial inversion layer becomes thick enough to bury the feedback cavity under a shell of mobile charge, so the valley to hill potential swing can be generated with minimal perturbation to the lateral energy barrier, keeping I_{OFF} nearly constant while I_{ON} surges. As per Fig. 4(e) & (f), for a given radius, shrinking the L_i from 25nm to 10nm shears roughly 60 % from the

window because the phase delay between the buried gates diminishes and the capacitive coupling stiffens. The proposed device shows negative differential resistance in the I_{DS}-$|V_D|$ characteristics when a current source is applied to the device ($|V_G|$=0V) [Fig. 5(a) & (b)] [5-6]. The same device shows hysteresis in I_{DS}-$|V_D|$ characteristics with zero gate bias and can sustain the memory window even with higher gate bias [Fig. 5(c) & (d)]. We also performed the statistical analysis for the sensitivity of the parameters on the hysteresis window.

IV. Conclusion

The reconfigurable core-shell nanowire feedback FET merges steep slope switching and non-volatile hysteresis in a single doped silicon nanowire whose behaviour can be tuned physically or electrostatically. The architecture dispenses with separate N/P doping steps, mitigates threshold variability, and supports logic in memory operation without exotic materials. The statistical analysis confirms the low sensitivity of V_{Hys} for Li and higher sensitivity for L_{G1} (N_{AL1}) and L_{G2} (N_{AL2}) for the RFBFETn and RFBFETp, respectively. Future work includes the extensive analysis of device variability with effect on the complex circuits for neuromorphic applications.

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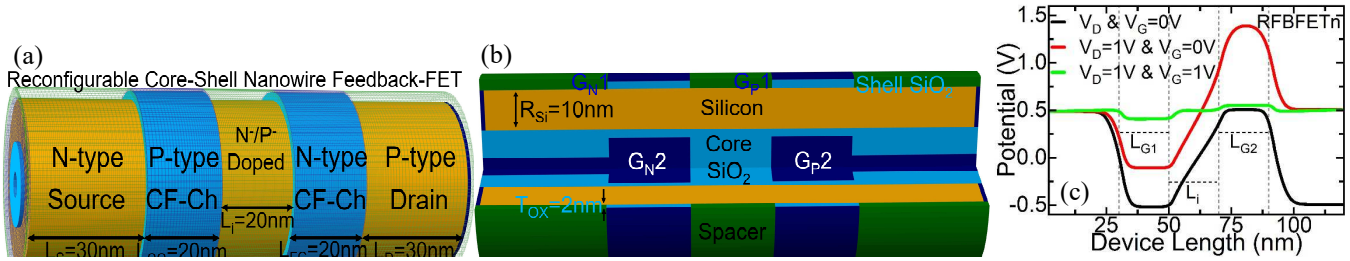

Fig. 1. (a) 3D perspective view of reconfigurable core-shell nanowire Feedback-FET with the used dimensions (L_i varied for the simulations); the proposed device can be used as N-type or P-type by properly biasing the source/drain and separated gates (b) 270° cutout of the proposed device showing the core oxide with the Silicon and core gates (R_{Si} is varied for the simulations) (c) Potential profile of the RFBFETn (using the proposed device as an n-type) across the device length for different biasing conditions [Equilibrium (V_D & V_G=0V), OFF-state (V_D=1V & V_G=0V) and ON-state (V_D & V_G=1V)]

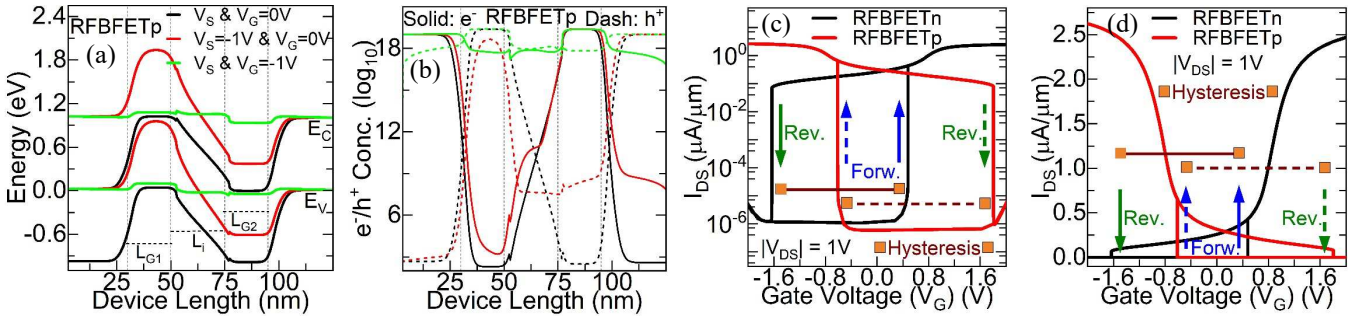

Fig. 2. (a) Energy band diagram, (b) Electron and hole concentration of the RFBFETp (using the proposed device as an n-type) across the device length for different biasing conditions [Equilibrium (V_S & V_G=0V), OFF-state (V_S=-1V & V_G=0V) and ON-state (V_S & V_G=-1V)] (c) & (d) Log and Linear plot of Drain current vs gate voltage characteristics of RFBFETn and RFBFETp showing the hysteresis in both the operating cases ($|V_{DS}|$=1V) respectively

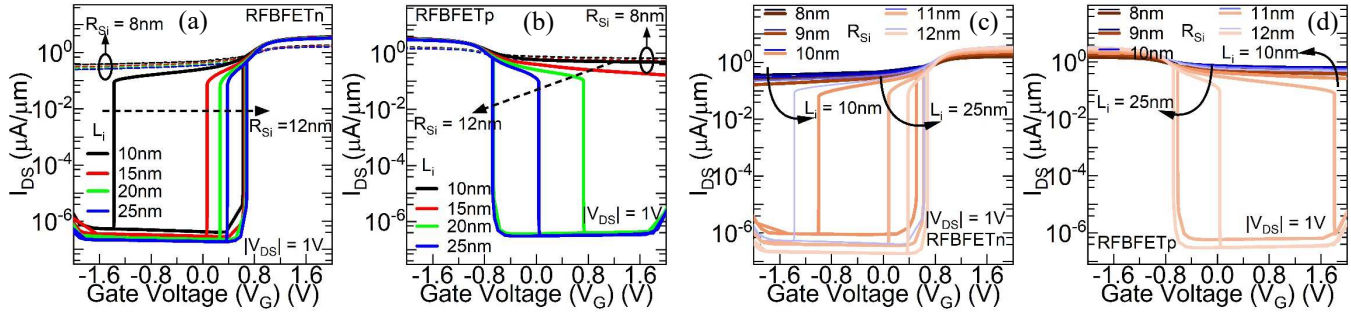

Fig. 3. (a) & (b) Comparison of drain current vs gate voltage characteristics of RFBFETn and RFBFETp respectively for different values of L_i while keeping the R_{Si} value fixed at the 8nm & 12nm (c) & (d) Comparison of drain current vs gate voltage characteristics of RFBFETn and RFBFETp respectively for different values of R_{Si} while keeping the L_i value fixed at the 10nm & 25nm showcasing the effect on hysteresis window

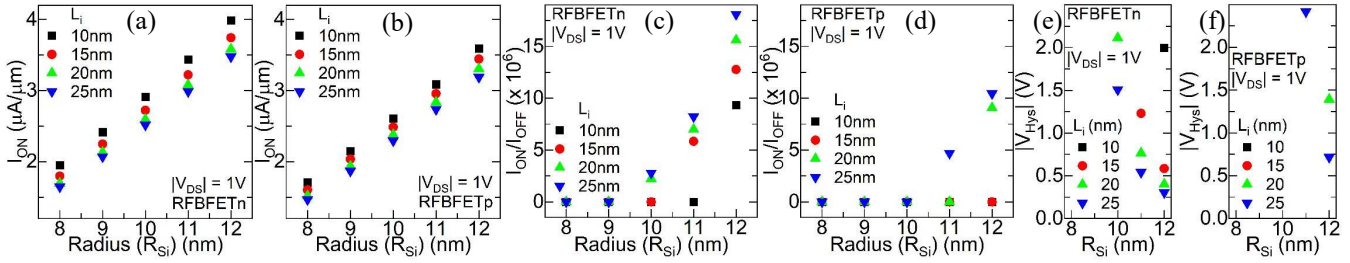

Fig. 4. (a) & (b) ON-current variation (c) & (d) I_{ON}/I_{OFF} (e) & (f) Hysteresis window variation in drain current vs gate voltage characteristics of RFBFETn and RFBFETp respectively with respect to different radius (R_{Si}) while varying the values of L_i and keeping N_{AL1}/N_{DL2} doping fixed at the $2.5x10^{19}cm^{-3}$

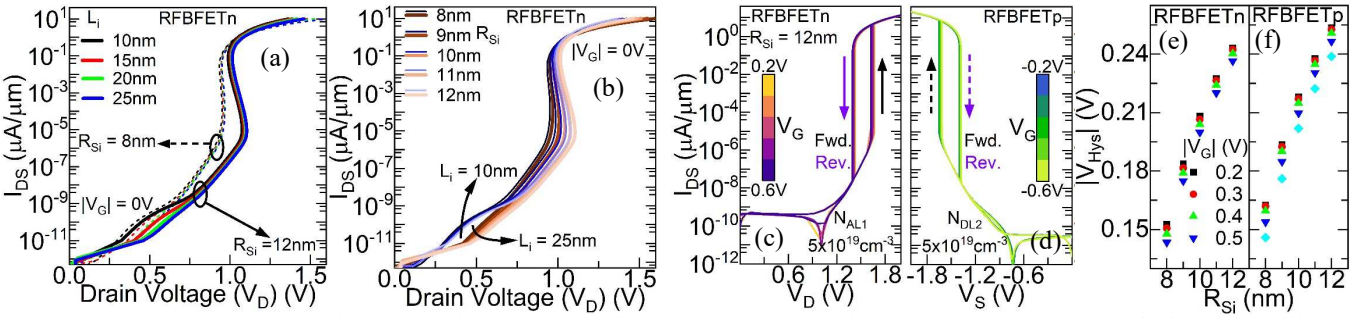

Fig. 5. Comparison of drain current vs drain voltage characteristics (applied current at drain electrode instead of bias) of RFBFETn at $|V_G|$=0V for (a) different values of L_i while keeping the R_{Si} value fixed at the 8nm & 12nm (b) different values of R_{Si} while keeping the L_i value fixed at the 10nm & 25nm (c) & (d) Comparison of drain current vs drain voltage characteristics of RFBFETn and RFBFETp respectively for different values of $|V_G|$ while keeping the R_{Si} value fixed at the 12nm (e) & (f) Hysteresis window variation with respect to different radius of RFBFETn and RFBFETp respectively for varying $|V_G|$