Stress Simulation of CFET Inverters with Unmerged SiGe S/D and Wrap-Around Contact

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***Abstract*—Stress profiles inside CFET inverters are analyzed with our in-house process emulator equipped with a newly developed stress module. In the conventional structure, the PMOS channel exhibits a peak compressive stress of -1.9 GPa, whereas the NMOS channel exhibits only +0.3 GPa tensile stress. In the PMOS, the horizontal defects lead to a 19% reduction in channel stress and vertical defects induce tensile stress in the channel. Employing the unmerged SiGe S/D, the peak stress of NMOS is enhanced to +1.2 GPa. Adopting the wrap-around contact in the PMOS lowers its channel stress by 19% compared to the conventional contact structure. These findings offer clear guidelines for stress-engineering optimized CFET architectures.**

***Keywords*—CFET, process emulation, stress simulation, wrap-around contact**

I. Introduction

The complementary field-effect transistor (CFET) is being explored as the next-generation technology beyond gate-all-around (GAA) transistors. In the FinFET technology, the main surface orientation was (110), resulting in similar levels of hole mobility and electron mobility. However, in GAA and CFET devices, the surface orientation is changed to (100), leading to lower hole mobility compared to electron mobility. Therefore, it is necessary to revisit the stress engineering technique to boost carrier mobilities. Since the presence of bulk silicon can significantly affect the quality of the SiGe source/drain (S/D), the PMOS is placed on the bottom tier [1].

When the S/D epitaxy process is conducted, defects may be generated because the S/D is grown on the channels and bulk silicon, which serve as seed layers. Studies are underway to investigate the impact of defects on channel stress [2]. The impact of defects on stress is being utilized to study unmerged SiGe S/D technology, which enables the formation of wrap-around contacts [3]. This reduces contact resistance and offers advantages from a device simulation perspective. In this work, we numerically analyze the changes in stress profiles during CFET process. Special attention is paid to the effects of unmerged SiGe S/D structures and the implementation of wrap-around contacts on the resultant channel stress profile.

II. Simulation Methodology

Our in-house process emulator, G-Process is based on the level-set method, and research utilizing it has been reported [4]–[6]. In this work, the stress module is newly implemented.

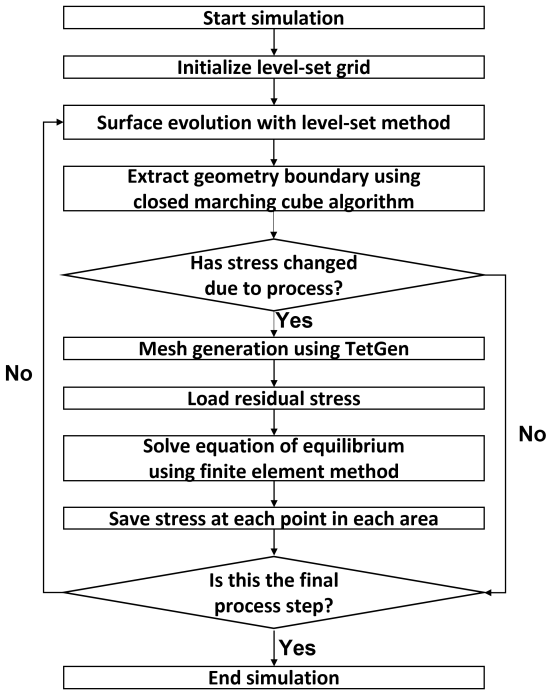

Fig. 1. Flowchart of the simulation which integrates level-set method-based process emulation and FEM-based stress simulation

The simulation flow of G-Process is shown as Fig. 1. When the process emulation starts, a three-dimensional (3D) tensor grid is made for the level-set. The process emulator tracks surface evolution throughout the process steps implicitly. When the process that affects the stress of structure is conducted, the boundaries are extracted using the closed marching cube algorithm. Form the extracted boundaries, a tetrahedral volume mesh is generated by TetGen [7]. Then the stress is calculated by solving the equation of equilibrium, expressed as

$$\nabla \cdot \tilde{\sigma} = 0, \tag{1}$$

where $\tilde{\sigma}$ denotes the Cauchy stress tensor. The equation is discretized via the finite element method (FEM). The relationships between stress and strain, and between strain and

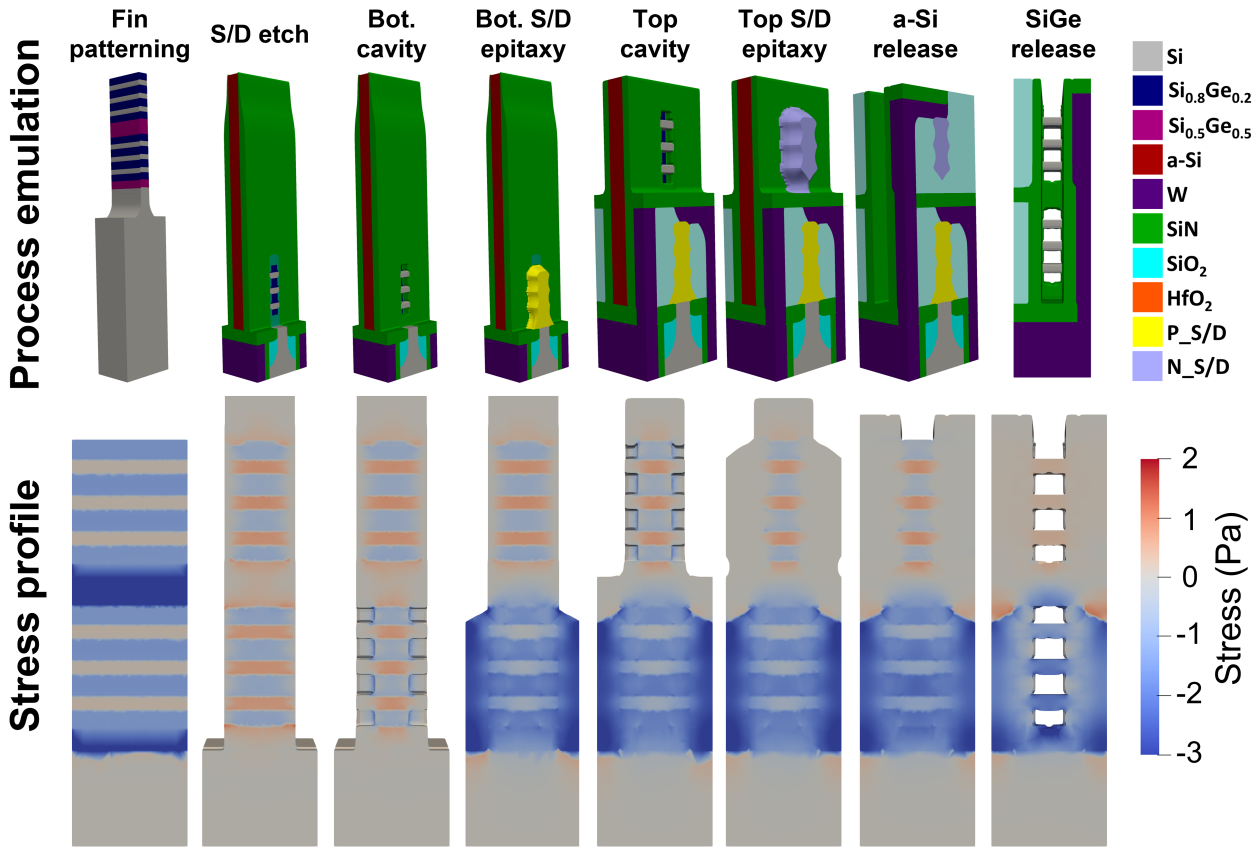

Fig. 2. Results of the process emulation and stress simulation. The conventional structure with buried power rail is considered. Only some selected process steps, where stress profiles are affected, are shown.

displacement, within a single element are given as follows:

$$\hat{\sigma} = C\hat{\epsilon} + \hat{\sigma}_0, \tag{2}$$

$$\hat{\epsilon} = B\vec{u}, \tag{3}$$

where $\hat{\sigma}$ and $\hat{\epsilon}$ represent the stress and strain vectors in the Voigt notation, respectively. $\hat{\sigma}_0$ is the residual stress, C is the fourth-order material matrix. $\vec{u}$ represents the displacement vector of the single element and B is the strain-displacement matrix. Substituting these relationships into (1) and applying the FEM, the followings are obtained.

$$K\vec{U} = \vec{F}, \tag{4}$$

where $\vec{U}$ represents the global displacement field vector. K is the global stiffness matrix of system and $\vec{F}$ is the force vector of system. They are defined as

$$K = \int_V B^T C B \; dV, \tag{5}$$

$$\vec{F} = -\int_V B^T \hat{\sigma}_0 \; dV. \tag{6}$$

By solving the linear system, $\vec{U}$ is obtained, and the corresponding stress is induced by (2) and (3). This step is repeated until the simulation is complete.

III. Simulation Result

The process emulation and stress calculation of the CFET inverter with buried power rail (BPR) is conducted using G-Process. The contacted poly pitch is 42 nm, with a gate length of 12 nm and a channel width of 12 nm.

Fig. 2 shows the results of the process emulation and stress simulation. $Si_{0.5}Ge_{0.5}$ source/drain (S/D) is grown by epitaxy to induce compressive stress in the bottom channels. For the top channel, stress cannot be applied in the same manner since there is no bulk Si. Instead, Si S/D is employed. In Fig. 3, the stress cutline graphs along the channel direction can be seen for (a) the PMOS and (b) NMOS. In the Si-SiGe stack structure, the compressive stress is initially applied only to the SiGe layer to the SiGe layer due to lattice mismatch. When the fin structure is formed, the SiGe layer undergoes lateral relaxation, which induces tensile stress in the channel direction through the Poisson effect [8]. In the case of PMOS, the compressive stress is induced by SiGe S/D epitaxy, whereas the Si S/D of the NMOS does not apply stress to the channel. The channel release process shifts the stress of both PMOS and NMOS toward negative values. As a result, the peak of channel stress is -1.9 GPa for the PMOS and +0.3 GPa for

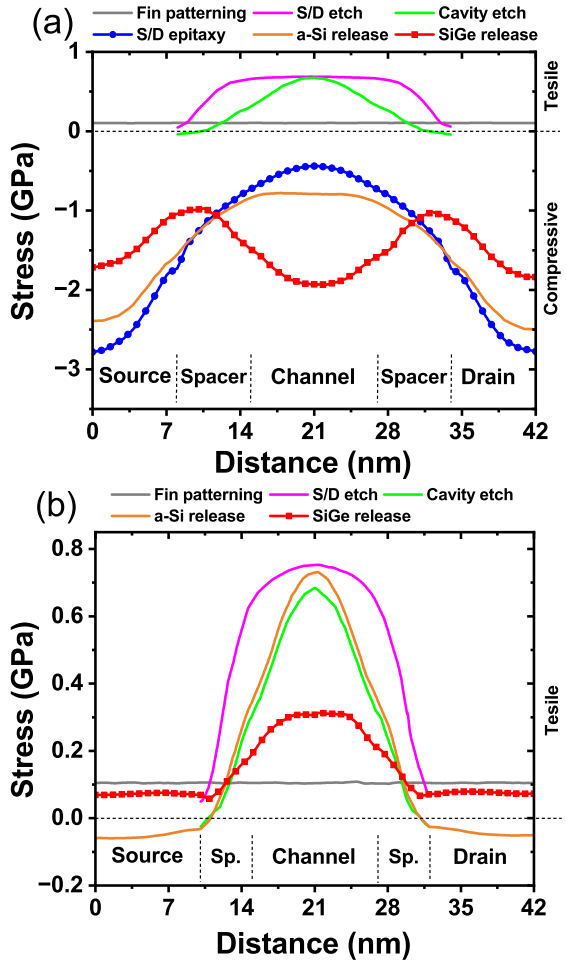

Fig. 3. Stress profile of middle channel according to the process with conventional contact: (a) PMOS (b) NMOS.

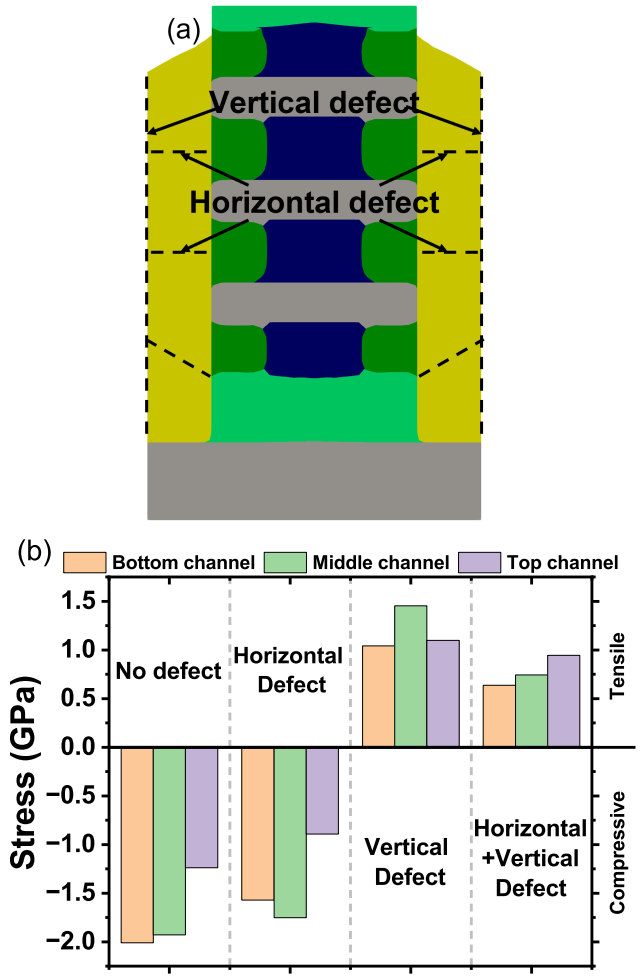

Fig. 4. (a) Location of defects induced by S/D epitaxy (b) the peak channel stress of each channel according to defects.

the NMOS.

The defect analysis during S/D epitaxy growth for the PMOS device can be seen in Fig. 4. In the S/D epitaxy process, when a defect occurs, a region where the defect is identified and treated as a void [2]. In the case of horizontal defects, a 19% reduction in stress is observed, whereas a vertical defect causes a change in the sign of stress. It can be utilized as a method to apply tensile stress to the top NMOS channel. The SiGe S/D, which is not merged with that of adjacent devices applies tensile stress to the channel, which facilitates the formation of wrap-around contacts. The wrap-around contact and unmerged $Si_{0.5}Ge_{0.5}$ S/D are introduced as shown in Fig. 5. The stress profiles of three cases (the structure in Fig. 2, the structure in Fig. 5, and the structure in Fig. 5 with defects in the S/D) are compared in Fig. 6. The unmerged SiGe S/D induces the tensile stress, and it is consistent with the previous report [3]. For the unmerged SiGe S/D with defects, the horizontal defects lead to a decrease in tensile stress, consistent with the results observed in Fig. 4.

Fig. 7 shows the impact of contact shape on stress in the PMOS. In the case of the wrap-around contact shown in Fig. 5, the stress profile appears asymmetric because the metal completely surrounds the drain side but only partially covers the source side. The S/D in the conventional contact structure is more extensively covered with low-k material compared to the wrap-around contact structure. Since the modulus of the low-k material is lower than that of the metal, greater stress changes occur during the channel release process. As a result, the wrap-around contact structure reduces the channel stress of PMOS by 19% in comparison to the conventional contact. From the perspective of the device simulation, the wrap-around contact is superior, so additional studies incorporating the deice simulation are needed.

IV. Conclusions

In order to boost the device performance of the CFET device, the stress calculation is important. Therefore, the stress module has been newly introduced in our in-house process emulator, G-Process. Using this tool, the emulation of the CFET inverter and the stress simulation has been carried out.

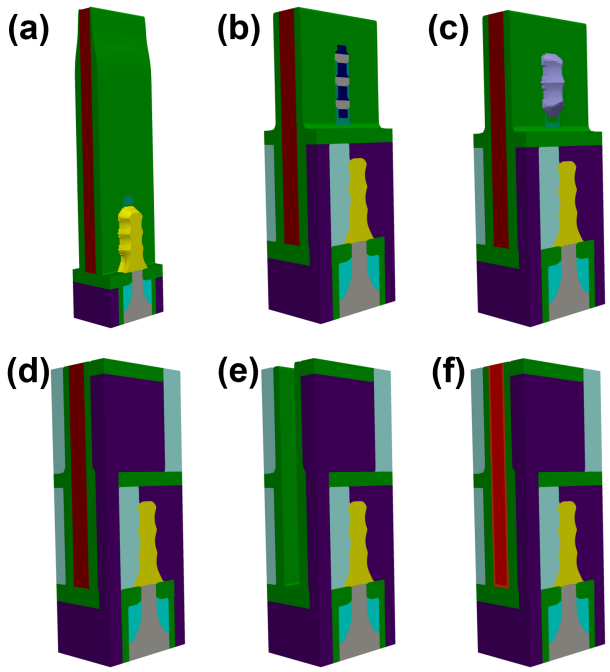

Fig. 5. CFET inverter process flow with unmerged SiGe S/D and wrap-around contact: (a) Bottom S/D epitaxy (b) Bottom S/D contact (c) Top S/D epitaxy (d) Top S/D contact (e) Channel release (f) HKMG.

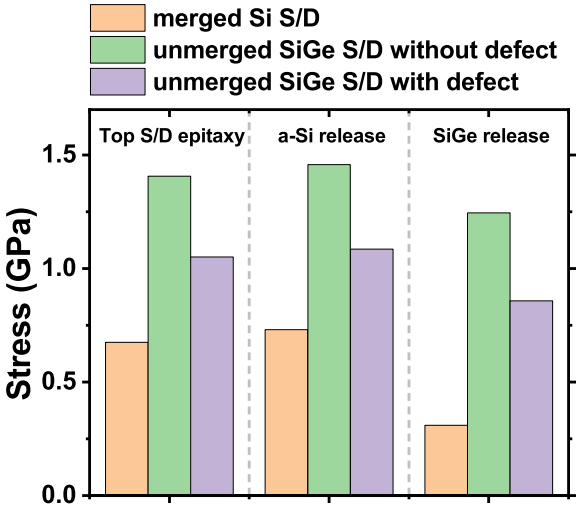

Fig. 6. Stress comparison between Si S/D, unmerged SiGe S/D, and defect-induced structures in NMOS.

The effects of process variations such as defects, unmerged S/D, and wrap-around contact on the channel stress have been investigated.

V. Acknowledgement

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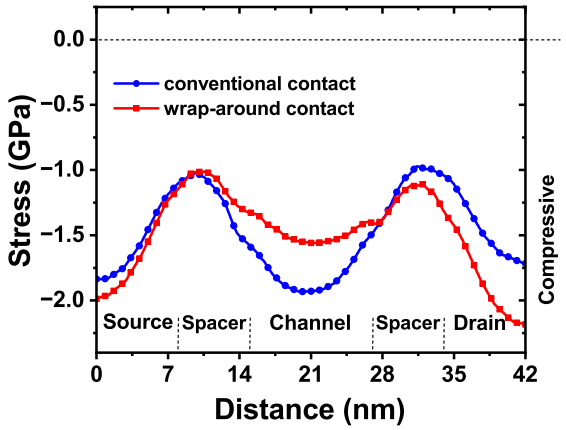

Fig. 7. Stress comparison between conventional contact (Fig. 2) and wrap-around contact (Fig. 5) in PMOS.

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