Modelling the Impact of Lateral Electrode Offset in Vertical Memristors for Neuromorphic Applications

Abin Varghese and Bipin Rajendran
Centre for Intelligent Information Processing Systems (CIIPS),
Department of Engineering, King's College London, London, United Kingdom
{abin.varghese, bipin.rajendran}@kcl.ac.uk

***Abstract*—We investigate the effects of lateral electrode shifting (skewing) in vertical metal-insulator-metal (MIM) resistive switching (RS) devices made of thin film oxides using a multiscale simulation platform. Incorporating relevant defect dynamics and electronic and thermal transport models, we compare the forming, set/reset, and voltage pulse-based conductance programming of skewed electrode devices and standard vertical memristor. Our simulations indicate that lateral electrode shift enables filament confinement during forming, reset and set processes, and influences RS behaviour due to prominent edge electric fields and introduces multi-level resistance states, making them promising for neuromorphic device applications.**

***Index Terms*—resistive switching, multiphysics simulations, HfOx, oxide memristors, neuromorphic devices.**

I. Introduction

Resistive switching devices, specifically memristors, are promising for neuromorphic computing due to their conductance programmability, which mimics synaptic plasticity [1]. Conventional vertical MIM RS devices typically rely on filamentary or interface switching mechanisms, mediated by ion migration or electrochemical reactions when an electric field is applied between the top and bottom electrodes [2]. While some filamentary memristors have experimental validation, their switching is stochastic, with oxygen vacancy filaments forming/rupturing in an uncontrolled and random (spatially) manner, leading to significant device-to-device and cycle-to-cycle variability and reliability concerns [3]. On the other hand, interface-type switching exhibits more complex interfacial electrochemical dynamics that lack a reliable microscopic picture [2], [3]. The ability to control the switching behaviour spatially and temporally is necessary for implementing synaptic plasticity mechanisms for neuromorphic learning rules, such as spike-timing-dependent plasticity (STDP) and stochastic weight updates [4]. Therefore, it is crucial to analyse the resistive switching behaviour in these types of devices using technology computer-aided design (TCAD) tools that include the relevant physics.

In this work, we propose a resistive switching memory (RRAM) with a skewed electrode MIM architecture, where the top and bottom electrodes are laterally offset to isolate the volume of the thin film that participates in resistance switching. While material, stack, and geometry (lateral or horizontal)-level approaches have been demonstrated to reduce variability and improve synaptic functionality [5], engineering the spatial distribution of conductive filaments via structural modifications has not been explored much. Our device configuration aims to guide filament formation through localized conductive paths, and introduce analogue resistance states, offering a new approach to modulating resistive states more predictably. Using the multiscale and multiphysics simulation software Ginestra™ [6], we investigate the impact of electrode position on electronic transport, oxygen vacancy filament formation and evolution, and stability of multi-level resistance states.

II. Simulation Setup

We employ a multiscale modeling approach using the Ginestra™ platform that provides a self-consistent solution of charge transport, defect (ion) generation/recombination and migration, along with power dissipation and temperature effects through the solution of Poisson, drift-diffusion, and Fourier's heat equations [7]. The device structure consists of (i) a switching layer (thin film HfOx, 5 nm) with an oxygen vacancy density (V^+) of 10^{19} cm^{-3} uniformly distributed in the dielectric (before forming), (ii) an ideal bottom electrode (TiN), and (iii) an ideal top electrode (TiN) which is laterally offset to define a skew distance (s_d). A thin layer (0.5 nm) of TiOx separates the top electrode from the HfOx switching layer, and functions as an oxygen ion (O^-) reservoir region. The dimensions of the devices are X = 3 nm, Y = 9 nm, and Z = 5.5 nm and the surface area of both electrodes is kept the same. The skewed device structure as well as the standard device configuration (control) are shown in Figure 1. The geometric asymmetry in the device structure (skew) introduces an electric field component in the plane of the switching material, in addition to the standard vertical component.

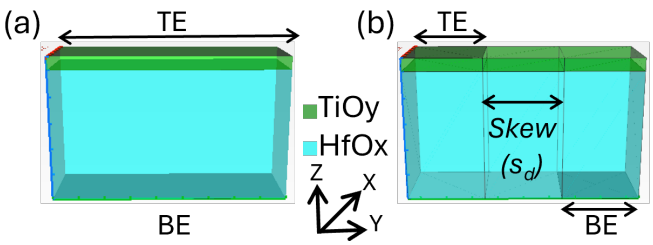

Fig. 1: Device representations of (a) standard vertical MIM, and (b) MIM with top and bottom electrodes laterally separated to define a skew length (using Ginestra™ simulation software).

III. Results and Discussion

We perform forming, reset, and set simulations to evaluate the impact of the skewed electrodes and compare the programming and conductance characteristics with the standard vertical memristor. For the HfOx-based filamentary switching RRAM device, the forming is simulated by applying a positive voltage ramp signal to the top electrode (TE), with a preset current compliance (CC). The current-voltage (I-V) characteristics of skewed devices, for a low CC of 1 μA (Figure 2), show multiple abrupt steps that increase with increasing skew distance, s_d. For a higher CC of 0.1 mA, the current values increase gradually post the sharp transitions (inset). For the control sample, D_C, the forming is marked by a prominent sharp increase in device current due to the conductive filaments that bridge the top and bottom electrodes at the voltage (V_{form}) at which CC is reached.

The 'formed' filaments are stochastically distributed in the switching layer, which is responsible for the significant variability observed in metal oxide-based RS devices [3]. However, in the skewed structure, during forming, oxygen vacancies are generated and closely distributed along the shortest path from the bottom to the top electrode. The electric field shows a graded nature across the electrodes, which promotes filament confinement. Along the 9 nm y-direction, the standard deviation of oxygen vacancies increases from 0.96 nm to 1.24 nm for s_d increasing from 0 (electrodes just misaligned) to 3 nm (large offset), whereas for D_C the value is 1.55 nm, highlighting better filament localization in the skewed structure. V_{form} can be modulated with the skew distance. Thus, s_d can be another parameter to optimize forming voltages (in addition to current compliance), which is critical for reducing power consumption during the initialization stage.

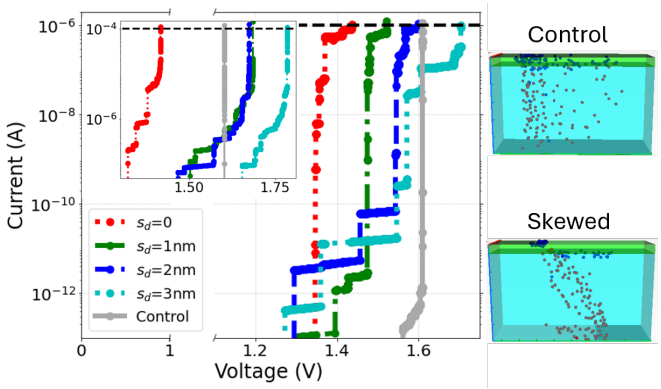

Fig. 2: A comparison of the forming I-V characteristics of devices with varying skew lengths and a vertical MIM control device for a low current compliance of 1 μA (inset shows the zoomed-in part for a higher compliance of 0.1 mA). On the right side, device plots show the nature of filaments in the control and skewed structures (using Ginestra™ simulation software). The red and blue spheres represent oxygen vacancies and oxygen ions, respectively.

Post forming, we studied the breakdown of the filaments under negative bias through reset simulations that were performed for a ramped negative voltage. As depicted in the negative voltage region in Figure 3(a), for s_d = 3 nm, reset occurs through multiple discrete drops in current due to fragmented dissolution of the conductive filaments, resulting in the high resistance state (HRS). Further, the set process for positive voltages (without CC) is also characterized by a stepwise increase in current to reach the low resistance state (LRS) at around 1.5 V. The ratio of forward to reverse sweep currents at V = 1 V increases significantly from 25 for s_d = 0 to ∼1000 for s_d = 1 nm. The distribution of oxygen vacancies and oxygen ions from the initial forming simulation forms the basis of the reset and set simulations, which further take into account the recombination and generation of the vacancies and ions, respectively. From Figures 3(b) and (c), it can be seen that both set and reset simulations lead to the respective formation and dissolution of the oxygen vacancy filament along the path traced by the initial forming stage. For the 3 nm skewed device, the standard deviation of the oxygen vacancies reduces to 0.91 nm (along the y-direction) after the set process. Thus, the filament path remains confined and partially intact (even at reset), which could improve endurance and reduce the device programming energy.

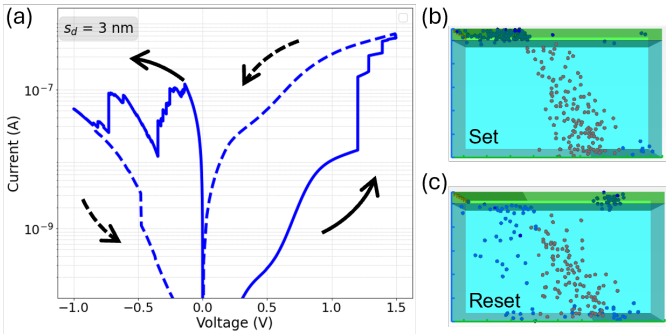

Fig. 3: (a) Current-voltage characteristics for a single reset-set cycle of the device with a 3 nm lateral skew of the electrodes. The direction of voltage sweeps for the simulations are indicated by arrows – solid for the increasing (in magnitude) voltages and dashed for completing the voltage loops. (b, c) show the difference in the nature of the oxygen vacancy filaments (represented by red spheres) under set and reset conditions, respectively (using Ginestra™ simulation software). The blue spheres represent oxygen ions.

The step-like features in the I-V characteristics hint at the possibility of multiple conductance states in the skewed devices. The ability to modulate conductance levels in a controlled and discrete manner is central to in-memory computing schemes where weight updates must be precise and repeatable. Potentiation simulations using constant-amplitude voltage pulses are used to probe the existence of discrete states. In a conventional RRAM with MIM structure, the first voltage pulse is usually enough to form a strong conductive filament, which results in a significant current increase followed by saturation [8]. This abrupt current increase does not enable a linear or controlled increase in conductance. For the skewed devices, the current increases steadily with pulses during potentiation along with good separability between levels, for programming and read pulses of magnitude 1.75 V and 0.2 V, respectively, and pulse width of 1 ms. Figure 4a presents the increasing read current response across multiple devices, all starting at the same initial configuration (at low conductance), to highlight the stochastic nature of devices that is captured

in these simulations. These devices are 'formed' at a low CC, hence only a few filaments can take part in the transport.

Similar to constant-amplitude potentiation, we apply negative voltage pulses to reduce the conductance from the potentiated state. For this, the programming and read pulses have a pulse width of 1 ms with magnitudes of -0.5 V and -0.05 V, respectively. The read current is controllably reduced, albeit stochastically, over multiple pulses (Figure 4b). We also compare the current modulation in the control device for similar simulations in Figure 4c. The skewed device shows better linearity in conductance programming in comparison to the control device. A confined and repeatable filament path enables a more reliable implementation of analogue weight updates, since the abrupt current jumps due to unpredictable filament growth can be minimized. Thus, the controlled potentiation and depression of conductance levels is uniquely made possible in the skewed structure.

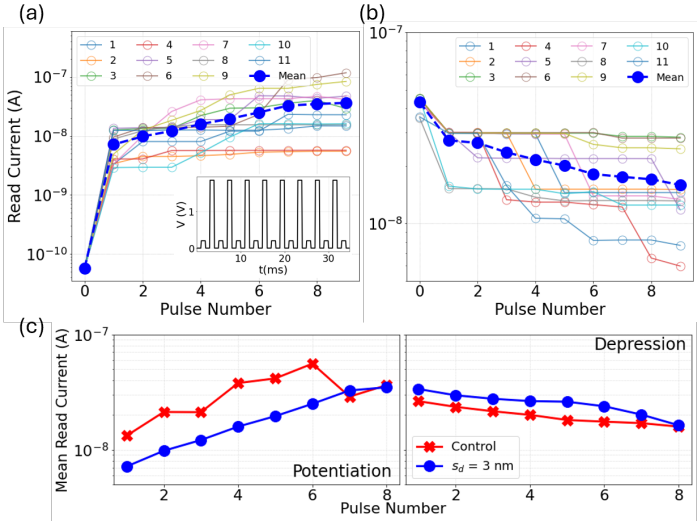

Fig. 4: Tuning the read current with constant amplitude voltage pulses across multiple devices. Positive (1.85 V) pulses (a) can potentiate the device current whereas negative (-0.5 V) pulses (b) can lead to depression. (c) shows a comparison of the mean read currents with pulsing for the control and skewed devices. A more controllable programming is seen in the skewed structure.

IV. Conclusions

In the proposed skewed RRAM device with MIM structure, the step-like (low compliance) and more-gradual (high compliance) current responses lead to a controlled increase/decrease in conductance levels with state-independent constant amplitude voltage pulses. This architecture offers the potential for reproducible resistive switching and multilevel operation without relying on complex material stack, doping or multilayer designs. Future work will focus on experimental validation of these structures. The use of industry-compatible materials such as TiN and HfOx for a crossbar array implementation of this structure could be promising for accelerating matrix vector multiplication. Our study offers an alternative pathway for designing more reliable memristive devices for non-volatile memory and neuromorphic computing applications.

V. Acknowledgement

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