Device process and architecture aware physical TCAD model for ultra-thin film a-IGZO transistors

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***Abstract*—Performance of amorphous IGZO thin film transistors is strongly linked to their device architecture and processing. We identify the critical parameters determining device performance across bias ranges through experiments and TCAD simulations. Based on this, we present a process-aware TCAD model describing transfer characteristics of three device architectures. Insights from this modeling work are used to understand the impact of various process steps on the device operation and propose design guidelines for performance optimization.**

Keywords— IGZO, thin film transistors, TCAD, device architecture, process-aware models

I. Introduction

Indium-Gallium-Zinc-Oxide (IGZO) thin film transistors (TFTs) are being researched for a wide range of applications, including 3D DRAM, RF circuits, displays, flexible electronics, neuromorphic computing [1]. For amorphous IGZO (a-IGZO) TFTs, the device characteristics are highly sensitive to architecture and fabrication process [2-5]. In [2], we demonstrated that moving from gate-first process to a gate-last integration scheme lowered channel doping in as-processed devices. A similar effect on doping was achieved on introducing raised contacts in [3]. We showed in [4] that even changes in the buffer layer on which a-IGZO is deposited can impact the performance. Further, in [5], we reported on the increase in subthreshold slope (SS) and sub-gap density of states (DoS) in a-IGZO TFTs on switching from back-gated to top-gated device configuration.

Physical models are necessary to understand and predict the performance of these devices for target applications. Though TCAD models for IGZO devices have been reported, they are usually tailored towards understanding a single device configuration and there is a lack of models exploring process induced device characteristics [6-9]. In this work, we present a TCAD model using Sentaurus^{TM} for three different a-IGZO TFTs architectures, with only a few process-related input parameters to capture the impact of fabrication steps on device characteristics.

II. Device and Model Definition

Figure 1 shows the three device architectures modeled in this work, back-gated device (BG), back-gated device with the top gate processed (BGTG), and top-gated device with oxygen tunnel module (TGOT) [3], with their transfer characteristics. Oxygen vacancies (V_O) and hydrogen (H) act as dopants in a-IGZO. Oxygen scavenging by TiN contact metal and H from W metal fill increase doping, reducing threshold voltage (V_t) [3]. Raised contacts move these sources of doping away from the channel. Annealing in oxygen ambient passivates V_O and increases V_t, but the oxygen pathways depend on device

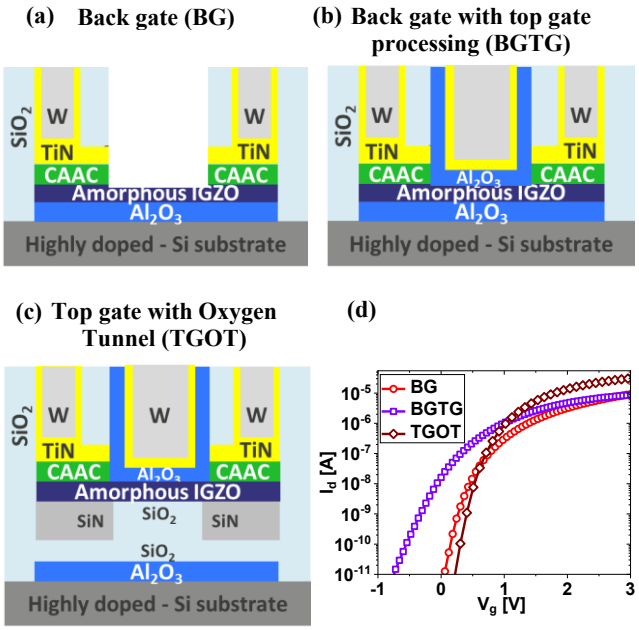

Fig. 1. Schematics of the modeled device architectures (a) back gate, (b) back gate device with top gate processed, and (c) top gate device with oxygen tunnel. Raised contacts help move sources of doping (TiN scavenging oxygen from channel, hydrogen from W-fill in the contacts) away from the channel. C-axis aligned crystalline (CAAC) IGZO raised contacts offers a good balance between doping due to scavenging and formation of thick interfacial layer. (d) Changes in the transfer characteristics across entire operating range underscore multiple effects of processing to be considered for process-aware modeling.

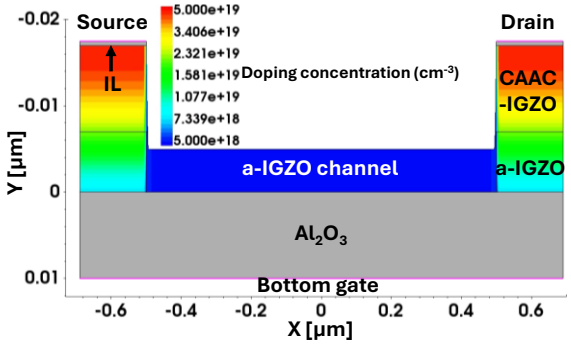

Fig. 2. Simulated device structure of BG is shown as an example. Etch-related recess into a-IGZO channel and rounded profile of the gate trench, are accounted in the device structure . To account for oxygen scavenging at contacts, a thin interfacial layer (IL) is added. Doping gradient from contact to channel is included to mimic the impact of scavenging and H from W fill in the contacts. (V_d = 1 V, W/L = 1 µm/1 µm)

architecture. A doping gradient is added to account for this in device simulations as exemplified for BG in Fig. 2. Doping under contacts is fixed at 5e19 cm^{-3}, while channel doping is

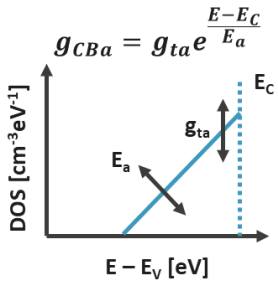

Fig. 3. Illustration of tail states close to conduction band defined as exponentially distributed acceptor states.

estimated from measured V_t. A thin interfacial layer is added at TiN-IGZO interface to emulate the contact oxidation. Further, a small over-etch and rounded corners are implemented to mimic the physical device [3]. We use W/L = 1 µm/1 µm devices to minimize short channel effects.

For a-IGZO, conduction (CB) and valence bands (VB) are assumed to be fully delocalized, with localized tail states attributed to the amorphous nature. Exponentially distributed tail states are defined as acceptor traps near CB (g_{CBa}) (Fig. 3) and donor traps near VB (g_{VBd}). A constant electron mobility in the channel is used as no significant difference was observed between drain current with constant mobility and percolation mobility models (not shown). Schottky barriers are added at interface of contact metal/raised contact (CAAC-IGZO) as well as a-IGZO ($\chi_{a\text{-}IGZO}$ = 4.16 eV [10])/CAAC-IGZO ($\chi_{CAAC\text{-}IGZO}$ = 4.6 eV [11]).

III. Modeling Device Operation

Key parameters in determining the transfer characteristics were identified from experiments [5,12] and parameter sensitivity simulations. Simplified anatomy of transfer characteristics with the identified parameters impacting various operation regimes is illustrated in Fig. 4(a). Here, we describe parameter extraction and fitting for the BG device (Fig. 4(b)-(f)). Non-ideal SS of 98 mV/dec (taken at minimum reliable current level) indicates presence of trap states. Subthreshold characteristics are impacted only by donor states at IGZO/gate oxide interface (D_{it}) and in IGZO channel. The ultrathin channel hinders separating the contribution of donor states in a-IGZO from those of interface states. However, in light-assisted studies, only deep donors were identified in a-IGZO which do not impact our operating bias range [13]. Therefore, these donors are included only at the interface.

In the moderate accumulation region, Fermi level (E_f) sweeps across g_{CBa} states, making their impact dominant. Total number of states increases on increasing either of the slope (E_a) and the peak of the exponential distribution (g_{ta}), and slows the rate of change of E_f with bias. Note that the extracted SS from experimentally detectable current ranges may still be impacted by tail states. Next, we vary mobility to model the on-state. With these, we achieve excellent fit across entire operating bias range for BG device (Fig. 5). Similar parametrization was used to achieve fits for BGTG and TGOT devices with fitting values listed in Table 1.

IV. Discussion

We utilize experimentally extracted V_t, mobility, SS, and D_t (D_{it} + g_{CBa}·$t_{channel}$) and the TCAD model parameters for different devices to elucidate the impact of processing. Top gate dielectric deposition on BG device increases D_t, degrading SS, as D_{it} at opposite interface of the back gate has a stronger impact. Gate metal TiN/W deposition increases channel doping, inducing a negative V_t shift. Counteracting this with oxygen anneals passivates V_O, thus reducing g_{CBa}, and hence D_t. As a result, current and SS decrease along with change in the moderate accumulation region. Conversely, forming gas anneals increase doping and g_{CBa} [5]. In the TGOT structure, presence of the oxygen tunnel module changes D_t due to different interface and anneal efficiency.

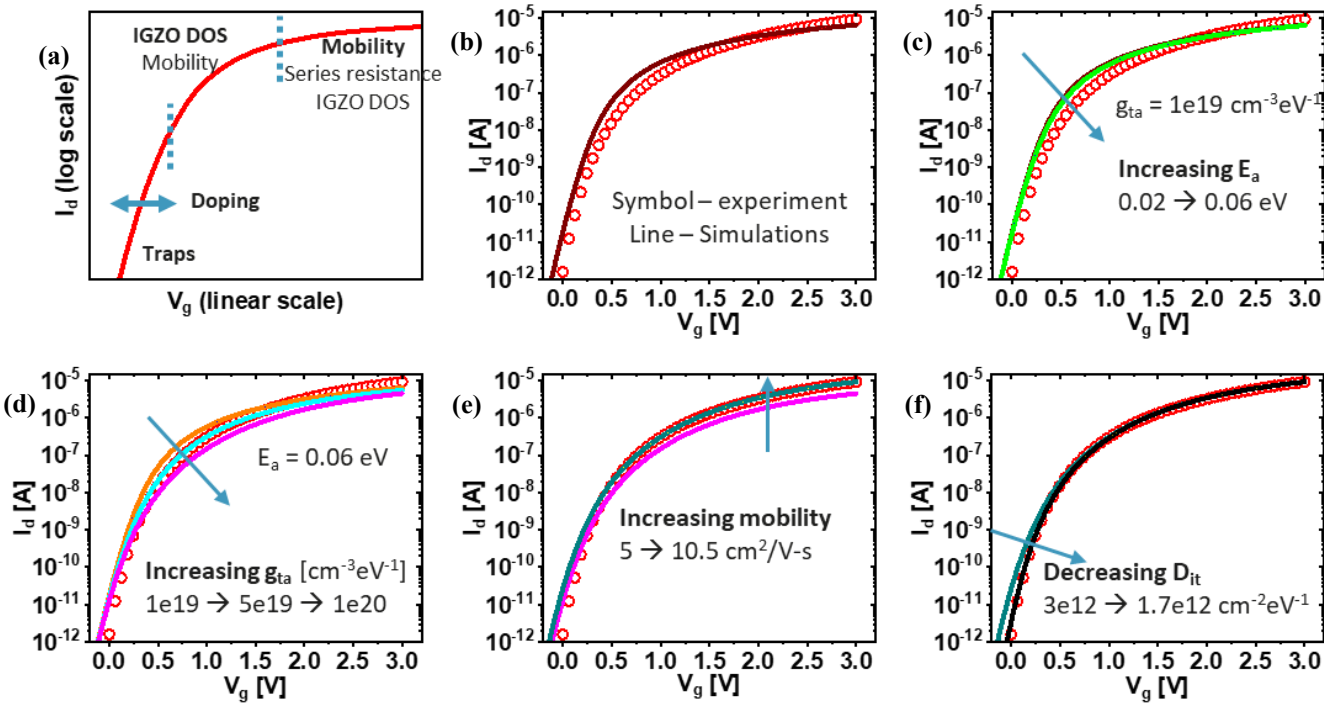

Fig. 4. (a) Based on sensitivity study, the dominant parameters in each operating regime is identified. (b) Transfer characteristics based on initial parameters from experiments and literature. (c)-(f) validate the impact of critical process dependent parameters seen in (a). They also showcase the calibration procedure.

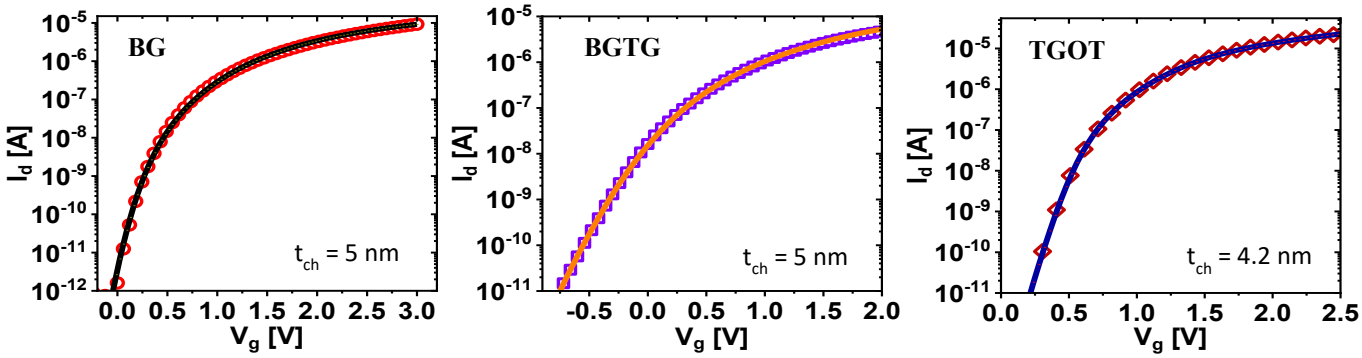

Fig. 5. Excellent fits are achieved for the three device architectures with the process-aware TCAD model, the parameters are listed in Table 1.

These insights further highlight the importance of considering process induced variations during physical model development. Moreover, they can be used to define guidelines for device optimization. For example, for better on/off current ratio, SS improvement is needed which requires consideration of both top and bottom interfaces with IGZO. Another is reducing the tail states, such as with oxygen anneals. This would enable a smaller V_g range for the moderate accumulation regime reducing voltage swing needed in applications.

V. Conclusions

A TCAD model for three device architectures of a-IGZO TFTs was presented, identifying the critical process related parameters. We reveal the impact of different process steps on the device characteristics, and highlight the importance of process dependent parameters in the model. This process-aware model can be used further for design optimization and variability aware simulations.

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TABLE I. Fitting parameters for different devices. This process-aware model provides insights into impact of the process on the device performance and helps define guidelines of device optimization.

Model parameter	**BG**	**BGTG**	**TGOT**
Channel doping [cm^{-3}]	5e18	7.8e18	1e17
Bottom D_{it} [$cm^{-2}eV^{-1}$]	1.7e12	1.7e12	1.7e12
Top D_{it} [$cm^{-2}eV^{-1}$]		7e12	1.7e12
Mobility [cm^2/V-s]	10.5	10.5	20
g_{ta} [$cm^{-3}eV^{-1}$] (Tail DOS)	1e20	1e20	6e19
E_a [eV] (Slope of tail DOS)	0.06	0.06	0.065

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