Compact Modeling of GAA-FET Applicable down to the T_{Si} = 5 nm Generation

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Abstract—**The reported compact model HiSIM_GAA, developed for circuit simulation, provides accurate reproduction of the 3-dimensional scaling characteristics of the Gate-All-Around (GAA) FET by capturing the complete potential distributions within the device under inclusion of the field confinements in three dimensions. The model scaling has been verified not only for the potential distributions within the device, but also by the reproducibility of V_{th} variations. While the channel-length reduction causes a V_{th} reduction, the reductions of the channel width or the silicon-substrate thickness cause a V_{th} increase, all of which is well reproduced. The observed complete V_{th} shift is modeled by the sum of these three modifications. Further, V_{th} is determined not only by the surface charge, but by the complete charge distribution of the GAA-FET due to the volume-inversion effect. Consequently, accurate circuit-performance prediction can be achieved only by efficient inclusion of the whole potential distribution in the compact model.**

Keywords—GAA-FET, compact modeling, whole potential distribution, field confinement in three dimensions, V_{th} prediction

I. Introduction

Thin-layer MOSFETs have been considered as suitable for down-scaling of device sizes, without the sacrifice of device-performance degradation. Especially, the GAA-FET has been investigated as one of the candidates for an ultimate FET structure [1]. Accordingly, aggressive down-scaling has been intensively investigated from a fabrication as well as a device-physics point of view, where a substrate-layer thickness T_{Si} down 5nm is the goal for the next years [2].

Compact models have been developed to realize accurate circuit-performance prediction in parallel with the device development [3, 4]. Nevertheless, many tasks are still remaining to fulfil the demands for accurate circuit simulation, such as modeling the small-size effects in the three structure dimensions. Our focus is the modeling of 3-dimensional scaling effects (L, W, T_{Si}), based on potential-distribution changes induced by the electric-field confinements in each direction. It is demonstrated, that our newly developed compact model accurately describes the potential distribution within the whole device, which enables accurate determination of V_{th} modifications.

II. Modeling of Field Confinements

The studied GAA-FET with an impurity concentration N_{Si} of 1×10^{15} cm^{-3} is configured as a 3D structure, schematically shown in Fig. 1 with dimensions for channel length L, channel width W and Si-substrate thickness T_{Si}, where nMOSFET is assumed. The studied target structure and additional structural variations are summarized in Table 1. The different sizes are selected to allow independent analysis of the down scaling in the three dimensions. 3D device simulations are studied instead of measurements, to characterize the features of the scaling microscopically [5]. For the simulation, number of mesh is increased up to the maximum so that small size change cannot be missed. Quantum-mechanical effects can be recognized as T_{Si} is reduced down to 7 nm (Fig. 2a), where the contribution is

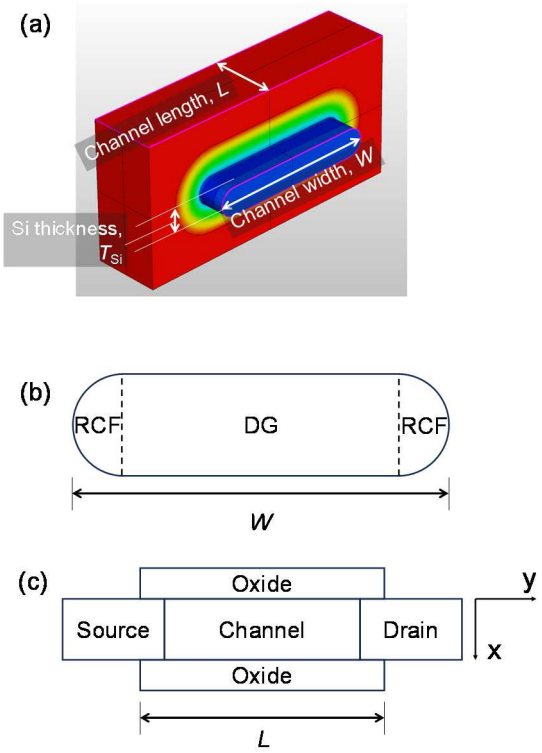

Fig. 1. (a) Studied GAA-FET structure with 3D device simulation, where $N_{si} = 1\times10^{15}$ cm^{-3} with EOT of 0.89 nm. Dimensions are given in Table 1. (b) A cross section of the structure along the width direction, where DG is the double-gate and RCF is the round circumference, modeled independently. (c) A cross section along the channel length direction, where the channel overlap length is fixed to 1.2 nm.

Table 1. Studied GAA-FET dimensions.

Device	L	W	T_{Si}	
#1	12 nm	30 nm	5.0 nm	: target
#2	3.0 µm	30 nm	5.0 nm	: long
#3	12 nm	1.0 µm	5.0 nm	: wide
#4	12 nm	30 nm	9.0 nm	: thick

most obvious under the strong-inversion condition, as expected [6]. For the investigation, a symmetrical structure (see Fig. 1c) is considered.

Modeling is done based on the Poisson equation, where all charges induced within the semiconductor are included as

$$\frac{d\phi}{dx} = -\frac{\rho(x)}{\varepsilon_s} \quad (1)$$

$$\rho(x) = N_D^+ - N_A^- + p - n \quad (2)$$

where N_D^+, N_A^-, p, n are densities of the ionized donors, the ionized acceptors, the holes, and electrons, respectively. The potential distribution is approximated by a quadratic function, and conventional boundary conditions are applied [7]. The quantum-mechanical effect is modeled as the oxide-thickness increase, which is a function of the carrier density [8]. The carrier distribution along the vertical direction is integrated analytically, once the carrier density distribution is calculated as a function of the potential distribution, the solution of the Poisson equation. The round-circumferences at the ends of the width direction are modeled separately from the double-gate control part due to different magnitude of field induced by V_{gs}.

The main focus of the present investigation is given on the subthreshold characteristics up to the moderate inversion condition, to investigate the volume-inversion effect, for which the modification of V_{th} by down scaling is mostly observed. A difficulty in compact modeling is that the middle potential ϕ_m (see Fig. 2b) is floating, and a boundary condition to determine the value is that the potential gradient at the position is zero. Therefore, the potential values (ϕ_s and ϕ_m) are calculated only by the Poisson equation, providing a consistent solution to preserve the Poisson equation together with the Gauss law. Here the Poisson equation is based on the charges induced within the device, and the charges are a function of ϕ. The final solution provides the potential distribution as a function of position. Since two unknown valuables (ϕ_s and ϕ_m) exist, thus, the Poisson equation is solved iteratively with use of two variable Newton method. The potential distribution along the channel direction is depicted in Fig 2c, a 3D-device simulation result as an example.

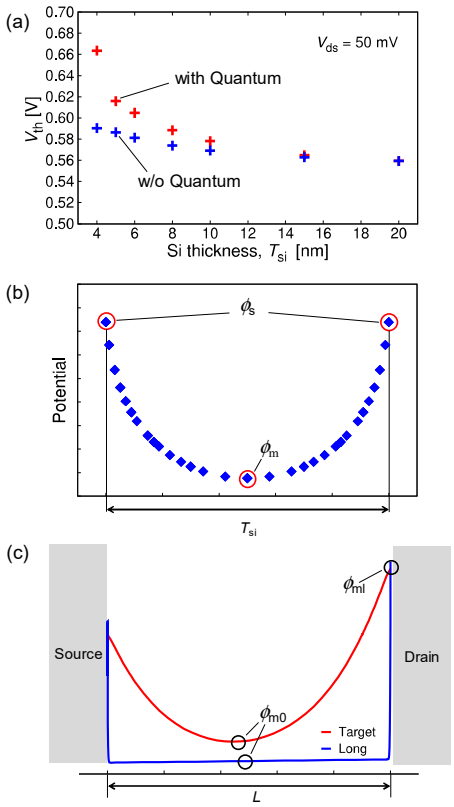

Fig. 2 3D-device simulation results (a) Quantum effect on V_{th} as a function of T_{Si} for the target device; (b) Potential distribution along the vertical direction (x direction) in the channel middle at V_{gs}=V_{th} and V_{ds}=50mV; (c) Potential distribution for the target device (#1) and the long device (#2) along the channel direction (y direction) at channel middle, where the bias condition is the same as (b).

The scaling in three dimensions causes three different potential-distribution changes: I. L reduction increases the electric-field overlapping into the channel region, which increases the potential ϕ_m; II. W reduction increases the round-circumference (RCF) contribution, which results in a higher vertical-electric-field confinement increase, namely a stronger gate control; and III. T_{Si} reduction causes a larger potential overlap along the depth direction, resulting in a flatter-potential distribution, origin of the volume inversion. All these effects are modeled as a modification of the gate control in HiSIM_GAA, and the Poisson equation is solved with the modification iteratively.

III. Compact-Model Results

3D-device simulation is applied for measurements so that microscopic features of macroscopic transistor characteristics can be analyzed [5]. The 3D-device simulation results are depicted in Fig. 3 for the L dependency. Fig. 3a demonstrates that the channel length reduction causes drastic subthreshold degradation. Fig. 3b depicts the derivatives of I_{ds} with respect to V_{gs}. Two peaks are observed in the second derivatives with reduced L length. Fig. 3c compares the calculated two potential values as a function of V_{gs}. It is seen that ϕ_m, the middle potential value, is higher than that of the surface. It can be concluded that ϕ_m controls the device characteristics under the subthreshold region. However, the potential values are completely identical for $V_{gs} > V_{th}$. This confirms that the inversion charge is completely independent of the structural variations but controlled only by V_{gs}. The V_{th} is extracted with the GMLE (g_m Linear Extrapolation [9]) method, which has been verified for its accurate extraction, even for nano-scale transistors [10]. W and T_{Si} dependencies are investigated in the same way as that for L. Fig. 4 depicts the same plots as Fig. 3 for the width W variation. Fig. 5 plots also the same characteristics for the thickness T_{Si} variation. It is seen that the increase of W and T_{Si} causes the reduction of V_{th}, which is opposite to the L variation. The V_{th} increase for the W increase is due to the reduced RCF effect, where the increased W results in the reduction of the RCF effect. Whereas, the T_{Si} increase causes the obvious enhancement of the short-channel effect.

Fig. 6 compares the extracted V_{th} dependencies for the 3-dimensional variations. It is observed, that the W and T_{Si} dependencies contribute to an increased V_{th} as sizes are scaled down. The reason for the V_{th} increase with reduced W is attributed to the delay of the starting of the volume-inversion effect in the RCF region. The reason for the V_{th} increase with reduced T_{Si} is attributed to the increase of the volume charge,

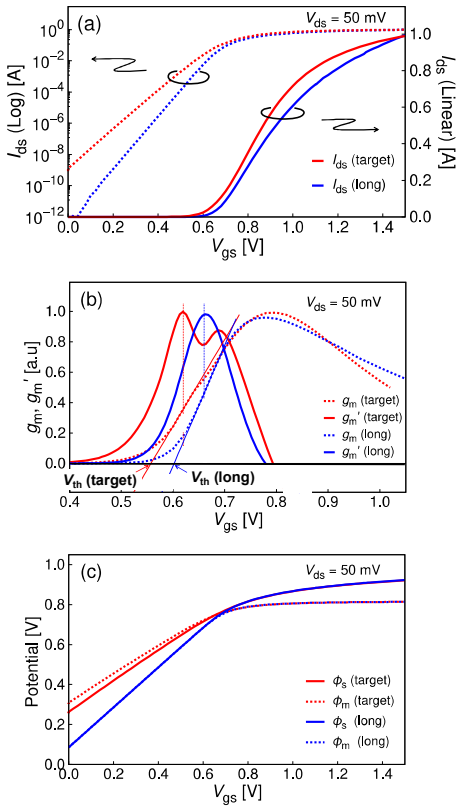

Fig. 3. 3D-device simulation results for (a) I_{ds} vs. V_{gs} characteristics for two different L (Devices #1 and #2); (b) g_m and g_m' depicting the V_{th} extraction by the GLME method; and (c) Surface potential ϕ_s and middle potential ϕ_m at the source side a function of V_{gs}. Maximum values of currents and derivatives are set to unity for comparison.

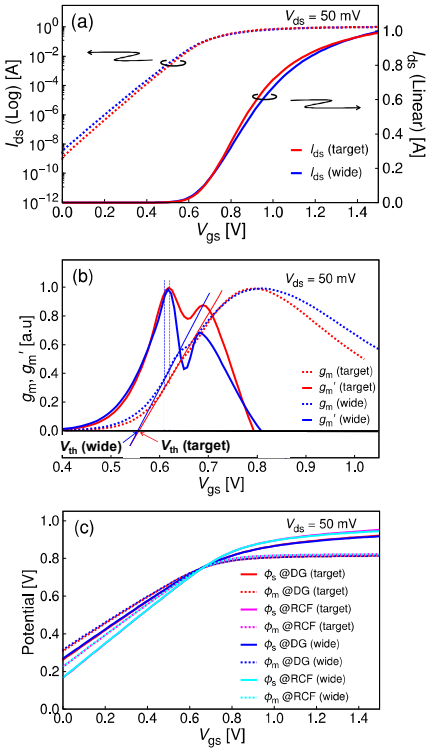

Fig. 4. 3D-device simulation results for two different W (Devices #1 and #3); (a) I_{ds} vs. V_{gs} characteristics; (b) g_m and g_m' depicting the V_{th} extraction; (c) Surface potential ϕ_s and middle potential ϕ_m. The wider device shows stronger short-channel effect due to the RCF effect.

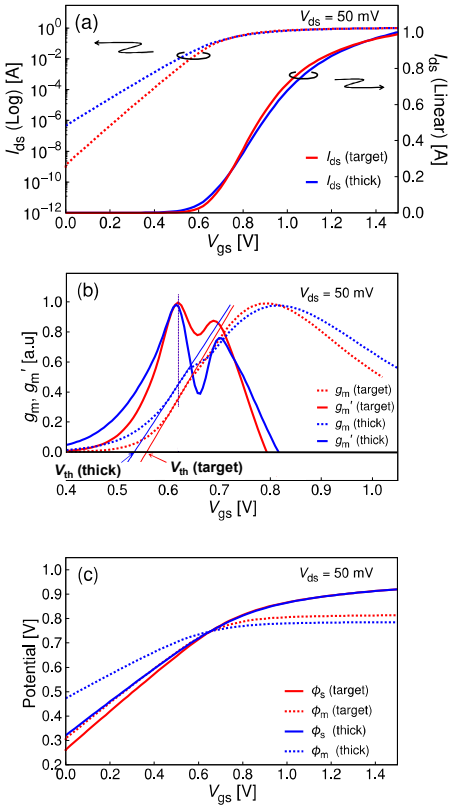

Fig. 5. 3D-device simulation results for two different T_{Si} (Devices #1 and #4); (a) I_{ds} vs. V_{gs} characteristics; (b) g_m and g_m' depicting the V_{th} extraction; (c) Surface potential ϕ_s and middle potential ϕ_m. The thicker device shows stronger short-channel effect due to the diminished T_{si} effect.

which prevent the starting of the inversion condition. This causes the enhancement of the short-channel effect. However, the T_{Si} increase causes much enhanced subthreshold degradation. It can be seen that the most effective scaling is the T_{Si} reduction. However, the reduction of T_{Si} causes enhanced quantum-mechanical effect, which prevents again T_{Si} from reducing further. Sum of these three contributions describes the V_{th} characteristics.

Figs. 7a and 7b compare calculated potential values with HiSIM_GAA to those of 3D-device simulation for two different L lengths. The comparison is done for the values in the channel middle. Good agreement has been achieved for all values. For the long-channel case, all potential values are identical between the DG part and the RCF part, except ϕ_s for $V_{gs} > V_{th}$. Under the condition, the RCF value is higher than the DG ones. The reason is the electric-field enhancement due to the structural feature of the RCF part. On the contrary, the short-channel case shows additionally splitted subthreshold characteristics. Mainly, the short-channel effect is the origin. The influence of the short-channel effect is suppressed strongly in the RCF region. The volume-inversion effect is observed in the extension of the linear dependence of V_{gs} as shown in Fig. 7c for the T_{Si} = 5nm case. With increase T_{Si}, the deviation from the linearity starts earlier than that of the thin T_{Si} case. For the short-channel case, it is enhanced by the potential ϕ_m increase. Under the $V_{gs} > V_{th}$ condition, the potential increases due to the field confinement effect is enhanced because the potential change is located only at the surface. For the short-channel case (see Fig. 7b), the potential

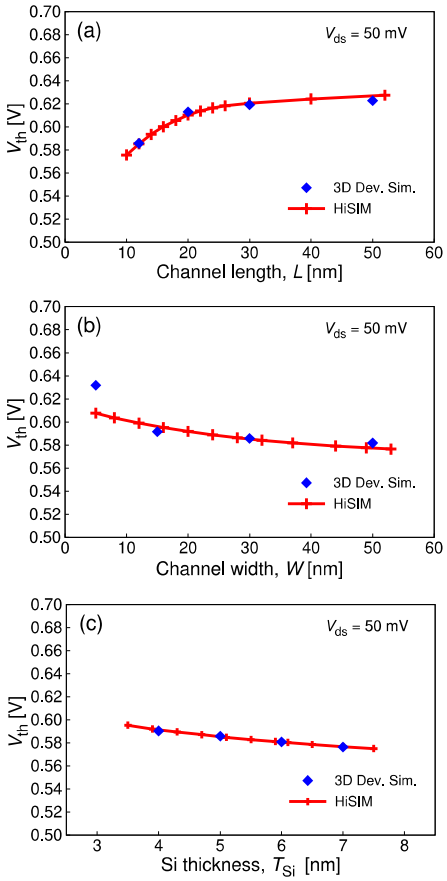

Fig. 6. Extracted V_{th} from calculated I_{ds}-V_{gs} with HiSIM_GAA in comparison to that of 3D device simulation results, (a) channel-length L variation, (b) channel-width W variation, and (c) T_{Si} variation. For the V_{th} extraction, the GLME method is applied.

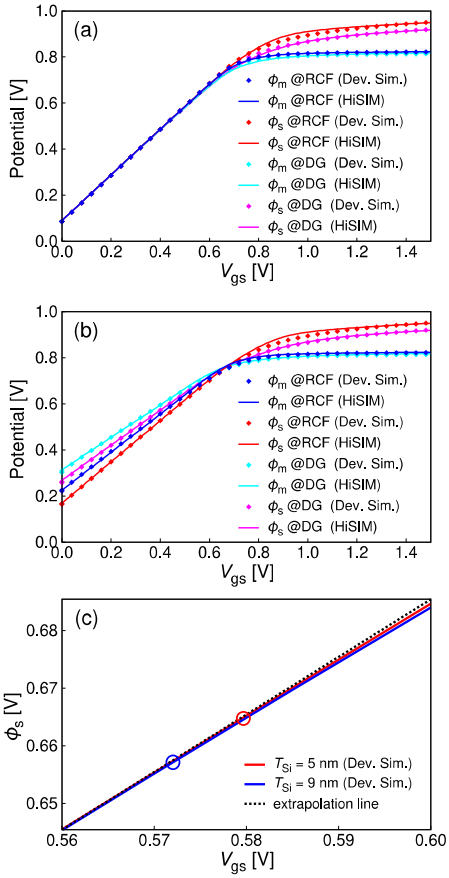

Fig. 7. Comparison of potential distributions calculated with HiSIM_GAA to those of 3D device simulation results, (a) L = 3 µm; (b) L = 12 nm; (c) Surface potential values of 3D-device simulation results as a function of V_{gs} for L = 3 µm with T_{Si} of 5 nm and 9 nm. The blue open circle denotes deviation point of the blue line (the 9 nm case) from the linear extrapolation line, and the red circle (the 5 nm case) denotes deviation point from the blue line.

distribution is independent of the channel length for $V_{gs} > V_{th}$. However, in the $V_{gs} < V_{th}$ range, two potential distributions extended from two surfaces start to overlap, which results in the $\phi_s < \phi_m$ condition.

IV. Summaries

We have developed a compact model for circuit simulation, which solves the Poisson equation explicitly. The accuracy of the calculated potential distribution within the GAA-FET is verified with 3D-device simulation. With the model the volume-inversion effect on the potential distribution is investigated. The reason for the observed two peaks in the derivative of the trans-conductance is attributed to the ϕ_m contribution, which causes drastic V_{th} reduction for the channel length reduction. Transistor starts to switch on not at the surface but rather in the channel middle. This volume-inversion effect is an inherent feature of thin-film MOSFET. This effect is enhanced by any device-size scaling down. On the contrary, the RCF region, non-flat surface, V_{gs} can control the carrier density more strongly than the DG region due to the field confinement caused by the structural feature. It has been demonstrated that three transistor size variations influence on V_{th} differently. Sum of these contributions is observed as the V_{th}. The developed model has been demonstrated to be applicable even for the optimization.

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