On the Channel and Wafer Orientation Dependence in Unstrained and Strained p–Type Nanosheets

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***Abstract*—The performance dependence on wafer and channel orientation in nanosheet pFETs with a sheet width of W_{NS}=12 nm and a sheet thickness of t_{NS}=5 nm is investigated by Monte Carlo (MC) device simulation. It is shown that (a) the influence of the sidewall changes the orientation dependence of the long–channel mobility in planar bulk pMOSFETs and (b) that this orientation dependence further changes in short–channel devices with (110)/⟨100⟩ having the hightest on–current in the absence of stress. The strongest performance is obtained for uniaxial compressive stress in ⟨111⟩ channel direction, while high uniaxial tensile stress in ⟨100⟩ direction enables only a modest gain.**

***Index Terms*—Wafer orientation, channel orientation, nanosheet, Monte Carlo, effective hole mobility, piezoresistance**

I. Introduction

With the introduction of nanosheets to replace FinFETs for future technology nodes, the dominant surface is becoming the standard (001) wafer orientation which is unfavorable for holes and favorable for electrons. One challenge is therefore to achieve the same performance for nanosheet pFETs as for nFETs, also in view of the problem to introduce stress.

This has led to experimental [1] and theoretical investigations [2], [3] on how pFET performance can be optimized with unconventional wafer/channel or stress configurations considering that in complementary FET (CFET) technology different orientations can be used for top and bottom devices with wafer bonding. However, these works in part only addressed a particular configuration [1], [3] or only addressed the ballistic regime [2] or low-field transport in bulk Si [3].

Here, we extend these works covering a comprehensive range of orientation and stress configurations with MC simulations of an advanced CFET–node nanosheet pFET. In particular, we include a physical discussion on how the impact of the sidewall and the gate length changes the orientation dependence of long–channel planar bulk MOSFET performance.

II. Simulation Approach

We employ MC device simulation [4] using the nonlocal empirical pseudopotential band structure [5] including spin–orbit interaction [4]. An effective quantum correction is adopted extracting effective work functions and different effective oxide permittivities for top–side and sidewall of the nanosheet from density–gradient simulation [6]. The phonon scattering model is as specified in [7] where also a comparison with the measured temperature–dependence of the bulk low–field mobility in silicon is shown. For ionized impurity scattering the Brooks–Herring model is adopted where the rate is multiplied with a doping–dependent prefactor calibrated to reproduce the Masetti mobility measurements [8]. A combination of specular and diffusive surface scattering is used with a diffusive ratio of 15 % which reproduces measured long–channel FinFET mobilities for different sidewall orientations [9]. Whereas the diffusive part is related to surface roughness, the specular part is governed by energy and parallel–momentum conservation and is responsible for the orientation–dependence of the effective mobility [9].

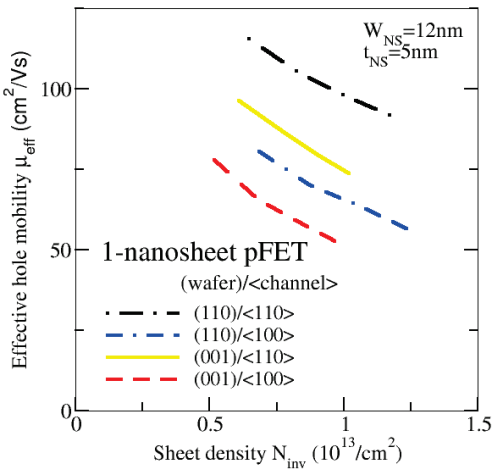

Fig. 1. Long–channel (L_G=0.5 μm) effective hole mobility in a single–sheet p–type nanosheet FET as a function of inversion density for different wafer and channel orientations.

III. Orientation–dependence without stress

While the long–channel mobility with (001) wafer orientation does not depend on channel direction in planar FETs [10] due to symmetry, the mobility for (001)/⟨110⟩ in Fig. 1 is larger than for (001)/⟨100⟩ and even for (110)/⟨100⟩ orientation. This is due to its associated (110)/⟨110⟩ sidewall/channel orientation which is the most favorable combination. And the contribution of the (110) surface is stronger than the t_{NS}/W_{NS} ratio because of its larger quantization mass [6] which implies a smaller effective oxide thickness with a better gate control.

However, the ⟨100⟩ channel direction has a smaller heavy–hole transport mass. Its impact becomes stronger in the quasi–

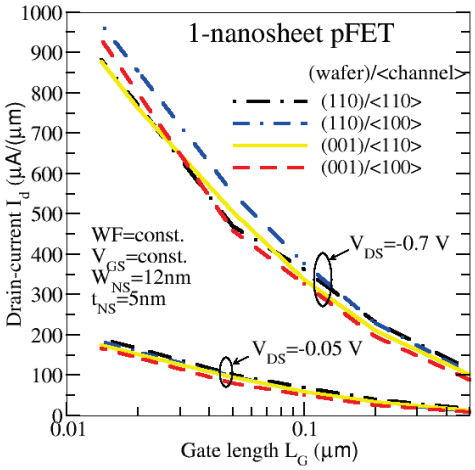

Fig. 2. Drain current, normalized by the effective gate width (W_{eff}=2 W_{NS} + 2 t_{NS}), as a function of gate length at V_{DS} = -0.7 V and V_{DS} = -0.05 V.

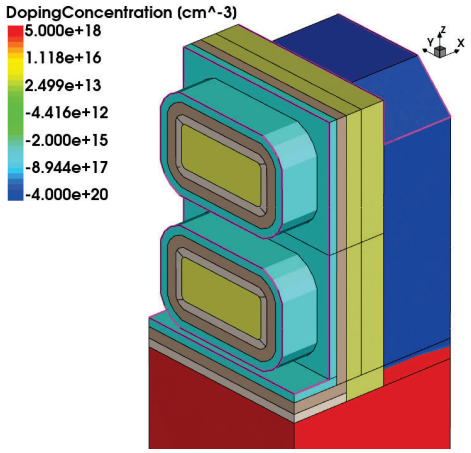

Fig. 3. Geometry (z=wafer-, x=channel- and y=sidewall-direction) and doping profile of the p–type short–channel (L_G=14 nm) nanosheet device. The contact resistivity is 1.5 x 10^{-9} Ω cm^2.

ballistic regime and leads at short gate length for higher driving fields in Fig. 2 to a higher on-current (ION) in consistency with short–channel ION measurements [11].

This different orientation–dependence of long–channel low–field mobility in Fig. 1 and short–channel ION in Fig. 2 is due to different transport regimes. Long–channel transport is governed by the surface impact which depends on the surface orientation and partly also on the channel direction. In contrast, quasi–ballistic short–channel transport is dominated by the transport mass, which depends on the channel direction, because the velocity gain during collision–less flight is the stronger the smaller the transport mass and the higher the driving field. In addition, the influence of the surface orientation on ION becomes weaker for shorter gate lengths as also demonstrated experimentally [10]. This difference between transport regimes leads the configurations with $\langle 100 \rangle$ channel direction to have the smallest effective mobilities in Fig. 1 and the highest on–currents at the shortest gate length in Fig. 2. Between these two limiting regimes there is a continuous transition as a function of gate length and applied drain voltage which determine the relevance of scattering and the strength of the driving field.

Simulating the realistic device in Fig. 3 with two sheets and contact resistance, where doping profiles and contact resistivity are as calibrated to state–of–the–art FinFET measurements [12], increases the access resistance and hence reduces the driving field, but Fig. 4 still shows 14 % ION gain for (110)/$\langle 100 \rangle$ over the standard (001)/$\langle 110 \rangle$ configuration. Note that the drain currents in Fig. 4 are, after normalization with the effective gate width, smaller than those in Fig. 2 at the smallest gate length. This is due not only to the higher access resistance, but also because of a smaller gate–over drive.

IV. Orientation–Dependence with Stress

The most fundamental quantity for the impact of stress on transport are the linear piezoresistance coefficients which have been measured for silicon and germanium [13] and

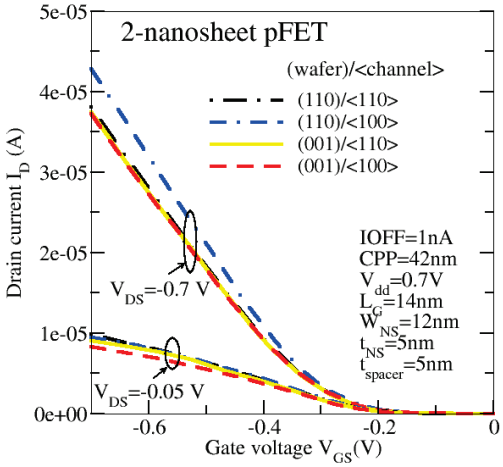

Fig. 4. Transfer characteristics of the p–type nanosheet device in Fig. 3 at V_{DS}=-0.7 V and V_{DS}=-0.05 V for different wafer and channel orientations.

allow to determine the low–field mobility response to a given stress tensor. In this work, we are concerned with uniaxial stress in different crystallographic directions described by the corresponding longitudinal piezocoefficient Π_{long}. They are explicitly given in [13] in units of $10^{-11}\,\text{Pa}^{-1}$ for $\langle 100 \rangle$ and $\langle 110 \rangle$ direction according to

$$\Pi_{\text{long}}(\langle 100 \rangle) = \Pi_{11} = 6.6 \quad (1)$$

$$\Pi_{\text{long}}(\langle 110 \rangle) = \frac{1}{2}(\Pi_{11} + \Pi_{12} + \Pi_{44}) = 71.8 \quad (2)$$

for p–type silicon. Here, we calculate the coefficient also for $\langle 111 \rangle$ direction with the result

$$\Pi_{\text{long}}(\langle 111 \rangle) = \frac{1}{3}(\Pi_{11} + 2\,\Pi_{12} + 2\,\Pi_{44}) = 93.5. \quad (3)$$

It demonstrates that the mobility response to uniaxial stress in $\langle 111 \rangle$ direction is stronger than that in $\langle 110 \rangle$ direction. This is reflected in the phonon–limited low–field mobilities as a function of uniaxial stress in Fig. 5 which shows that

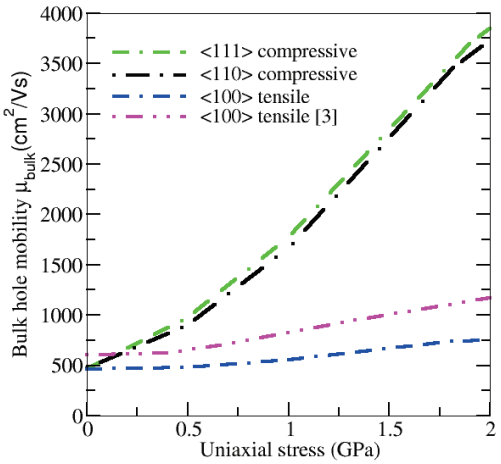

Fig. 5. Phonon–limited mobility of holes in bulk silicon as a function of uniaxial stress according to bulk MC simulation with a field of 0.1 kV/cm in comparison to theoretical mobilities from literature [3], where we have converted strain to stress via Hooke's law.

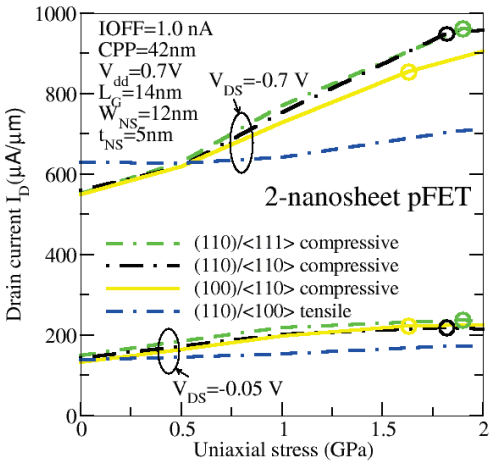

Fig. 6. Drain current, normalized by $W_{\rm eff}$, of the p–type nanosheet device in Fig. 3 as a function of uniaxial stress at $V_{\rm DS}$ = -0.7 V and $V_{\rm DS}$ = -0.05 V. The circles correspond to the channel stress values obtained by mechanical stress simulation for a $Si_{1-x}Ge_x$ source/drain stressor with x=0.5 where also the impact of the replacement metal gate (RMG) process step on stress is considered.

uniaxial compressive stress in ⟨111⟩ direction involves a somewhat stronger hole mobility improvement in bulk Si than in ⟨110⟩ direction. Consistent with the small value of the longitudinal piezoresistance coefficient for ⟨100⟩ direction in (1) the corresponding mobility in Fig. 5 is insensitive to small stress. However, for large tensile stress in ⟨100⟩ direction there is a noticeable mobility enhancement of up to 60 % at 2 GPa. This is of potential interest as it could enable a new stress configuration for pFETs. However, our mobility increase for tensile stress is smaller than the 90 % at 2 GPa reported recently [3].

But this tensile stress of 2 GPa in ⟨100⟩ direction leads to 14 % stress–induced ION enhancement in Fig. 6 which shows the drain currents at high and low drain voltage as a function of uniaxial stress for different configurations of stress and wafer as well as channel orientations. Compared to ION for ⟨110⟩ or ⟨111⟩ channel orientations without stress the improvement is even about 30 %.

For compressive stress, changing the standard (001)/⟨110⟩ orientation involves only a limited ION gain for given stress. But stress simulation [14] shows that a changed wafer orientation leads for the same stressor to a higher channel stress enabling 13 % ION enhancement in total. This is again consistent with ION measurements [15] which display for the same stressors a strong ION gain for (110)/⟨111⟩ over the (001)/⟨110⟩ configuration. Note that a drain voltage of 50 mV involves at the short gate length of 14 nm an increased driving field which leads to transport beyond the linear regime, but not yet to quasi–ballistic velocity overshoot therefore limiting the stress–induced performance gain (compare the discussion of linear, nonlinear and quasi–ballistic transport in [16]).

V. Conclusions

We have performed a comprehensive Monte Carlo study of the performance dependence on channel and wafer orientations in unstrained and strained p–type nanosheet devices. It has been shown that the optimum orientations can be different between long and short channels and between unstrained and strained devices. Therefore the present work can serve as a guideline to optimize device performance for different device options such as the CFET architecture and under different process conditions like the presence or absence of stress.

Acknowledgment

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