Self-Heating Coupled Hot Carrier Degradation in Stacked GAA FETs Based on Full Quantum Simulation Framework

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***Abstract*—Despite the superior electrical performance of GAA FETs, their reliability faces significant challenges due to self-heating and hot-carrier degradation (HCD). We introduce a full quantum reliability simulation framework that uses quantum transport to model electron–phonon interactions, defining BEOL-level heat sources from net phonon emission and overheated electrons, and solving heat transport via a two branch phonon transport model. Furthermore, the electrothermal results, including electron energy distribution, single trap induced threshold voltage shift, and lattice temperature, feed into the HCD model to predict trap generation and threshold shifts. Applying this framework, the impact of self-heating on HCD is investigated, and the critical role of thermal management is elucidated.**

***Index Terms*—GAA FETs, quantum transport, self-heating effect, hot carrier degradation.**

I. Introduction

GAA FETs benefit from channels fully enclosed by the gate, yielding excellent electrostatic control and electrical performance. However, their compact geometry and aggressive scaling incur severe self-heating effect (SHE) and hot-carrier degradation (HCD) [1]–[3]. Accurate and efficient modeling of these reliability challenges is therefore critical.

At nanometer scales, quantum tunneling and confinement invalidate drift-diffusion transport, requiring quantum transport [4]. Likewise, classical Joule and Fourier thermal models fail, necessitating a treatment for heat generation by phonon counting and phonon transport [5]. For HCD, the carrier-energy and resonance-state distributions driven model provides a more rigorous physical description [6], [7].

To address SHE and HCD reliability in stacked GAA FETs, we propose a novel electrothermal simulation framework based on quantum transport as well as BEOL thermal transport. Applying this framework, the impact of self-heating on HCD is investigated, and the pivotal role of thermal management in device reliability through buried-oxide (BOX) material design is demonstrated.

II. Model and Simulation

Fig. 1 illustrates the proposed TCAD reliability framework. The self-consistent electrothermal simulation is achieved by coupling quantum transport for the FEOL-level electrical behavior and two branch phonon transport for the BEOL-level thermal response. Then the extracted electron energy distribution (EDF), single trap induced V_{th} shift (η), and lattice temperature (T) feed into the HCD model to predict defect generation and threshold voltage shifts.

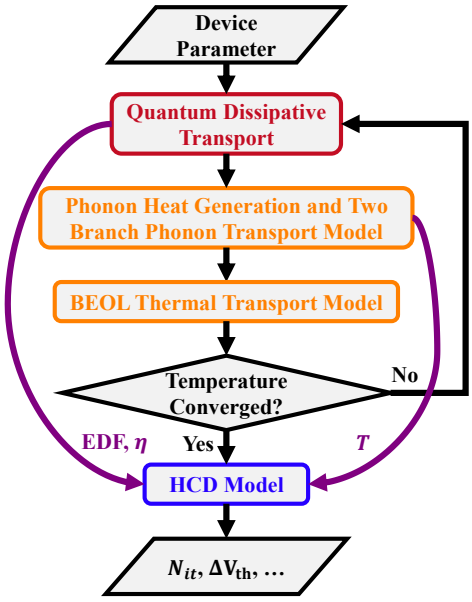

Fig. 1. The proposed TCAD framework to investigate SHE and HCD based on the quantum transport model.

Fig. 2(a) illustrates the 3D FEOL structure of a nanosheet (NS) GAA FET. Exploiting its quasi-1D geometry, the dissipative non-equilibrium Green's function (NEGF) quantum transport model employs the mode space approach to significantly

reduce computational complexity. And the quantum confinement of the nanoscale cross-section of the NS is considered within the Poisson-Schrödinger equations **(Fig. 2(b))** [8], [9]. In **Fig. 3**, the calibration results exhibit excellent agreement between simulation and experimental data [10].

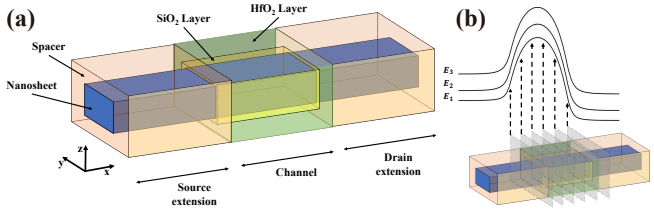

Fig. 2. (a) The 3D FEOL structure of a NS GAA FET. Note that in this paper, x is the transport direction. (b) The mode space method applied to the NS FET.

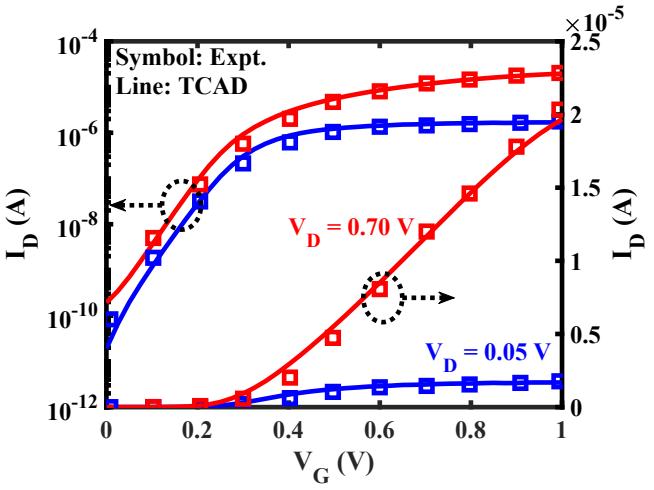

Fig. 3. The calibration of the transfer characteristics of the NS FET with the experiment data [10].

Fig. 4 demonstrates the electron energy flux distribution used to extract phonon heat, with electron–phonon interactions rigorously treated using the dissipative NEGF method (**Eq. (4-6)**) [11], [12]. As depicted in **Fig. 5**, only a small portion of the supplied energy is dissipated as phonon heat within the NS, while a significant amount of heat is carried by high-energy electrons dissipating in the drain side.

Consequently, the BEOL structure of the stacked NS device incorporates the heat source configuration shown in **Fig. 6**, including the phonon heat in three NS layers and the overheated carrier's heat in the drain contact. Utilizing the two branch phonon transport model (**Fig. 7**), the temperature distributions of both acoustic (AC) and optical (OP) phonons, as well as the lattice, are obtained [13].

Finally, the HCD model considering single vibration excitation (SVE) as well as multiple vibration excitation (MVE) driven by high-energy electrons and resonance states is shown in **Fig. 8** [7], [14].

III. Results and Disscussion

This study examines a three-layer stacked NS FET with a 10 nm gate length and a 5 nm×5 nm cross-section. **Fig. 9** shows

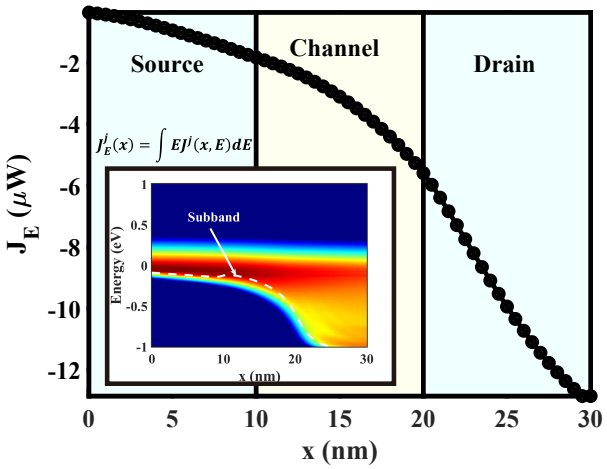

Fig. 4. Electron energy flux distribution obtained from the dissipative NEGF method, with the inset showing one of the subbands and its corresponding current-energy spectrum.

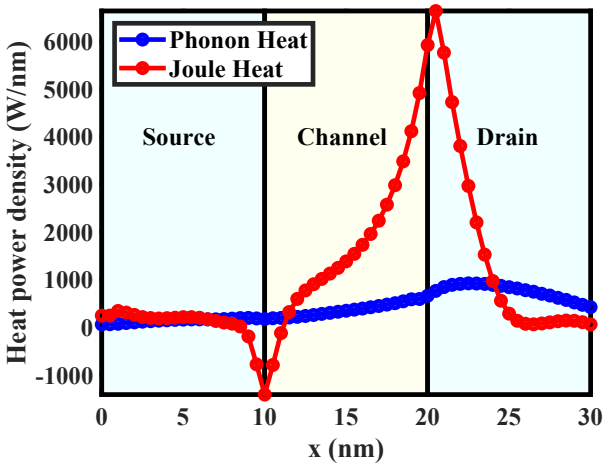

Fig. 5. The distribution of the phonon heat and the Joule heat along the transport direction, indicating that only a small fraction of the supplied energy is dissipated within the nanosheet.

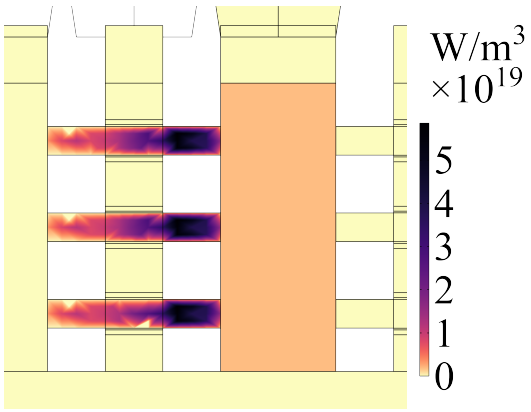

Fig. 6. The heat source setting in the stacked NS FET BEOL structure, including the phonon heat in three NS layers and the overheated carrier's heat in the drain contact.

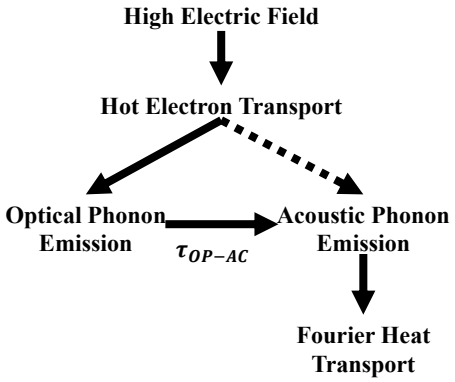

Fig. 7. The two branch phonon transport model applied to obtain the temperature distributions of the AC, OP phonons, and lattice in the NS. The dotted line indicates electron–AC phonon scattering, whose contribution to energy transport is minor and therefore neglected in this work.

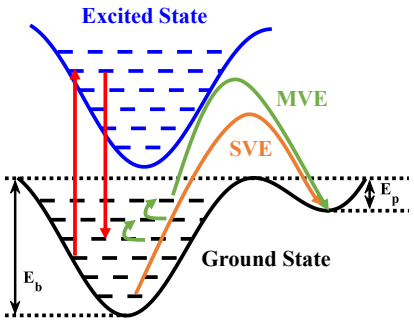

Fig. 8. The MVE and SVE model of the interface traps generation during the HCD process.

TABLE I
EQUATIONS USED IN THIS WORK

Dissipative NEGF

(1) $G = [EI - H - \Sigma_L - \Sigma_R - \Sigma_S]^{-1}$

(2) $\Sigma^{in,j}_{AC,S}(E) = \frac{\Xi_0^2 k_B T}{\rho v_s}\sum_i G^{n,i}F^i_j$

(3) $\Sigma^{in,j}_{OP,S}(E) = \frac{\hbar\Xi_0^2}{2\rho\omega}\sum_i[(N_\omega+1)G^{n,i}(E+\hbar\omega) + N_\omega G^{n,i}(E-\hbar\omega)]F^i_j$

Phonon Heat Generation

(4) $J^j_E(x) = \int EJ^j(x,E)dE$

(5) $Q^j_{1D}(x) = -\nabla\cdot J^j_E(x)$

(6) $Q_{ph}(x,y,z) = \sum_j Q^j_{1D}(x)|\phi^j(y,z)|^2$

Two Branch Phonon Transport

(7) $C_{AC}\frac{\partial T_{AC}}{\partial t} = \nabla\cdot(k_{AC}\nabla T_{AC}) - H$

(8) $H = C_{OP}\left(\frac{T_{OP}-T_{AC}}{\tau_{OP-AC}}\right)$

(9) $T_{lattice} = \frac{T_{AC}C_{AC}+T_{OP}C_{OP}}{C_{AC}+C_{OP}}$

BEOL Heat Source Components

(10) $H_{DC} = \frac{Q_{Joule}-Q_{ph}}{V_{DC}}$

(11) $H_{tot} = H_{NS} + H_{DC}$

Hot Carrier Degradation

(12) $\frac{dN_{it}}{dt} = (N_0 - N_{it})R_a - N^2_{it}R_p$

(13) $\Delta V_{th} = \sum_i \eta_i N_{it,i}S_{grid,i}$

the device's temperature distribution at $V_D = V_G = 1$ V. Due to OP phonon contributions, the actual lattice temperature in the NS is about 50 K higher than that predicted by Fourier's law, indicating significant SHE. **Fig. 10** displays the extracted EDF and $|\eta|$. Results reveal that SHE drives carriers toward higher energy levels, and $|\eta|$ increases closer to the channel center, both along the transport direction and laterally.

Incorporating these results into the HCD model yields predictions of defect evolution and threshold voltage degradation.

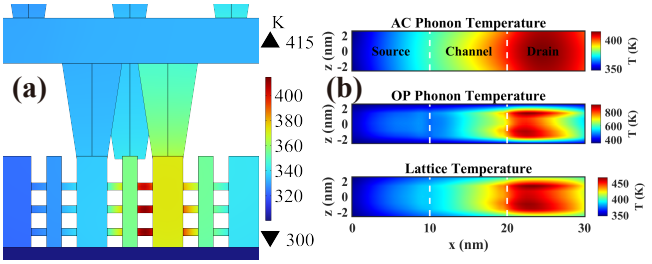

Fig. 9. The temperature profile of (a) the BEOL device solved by the Fourier law and (b) the AC, OP phonons and lattice in the middle NS layer solved by two branch phonon transport model on the cross section of $y = 0$.

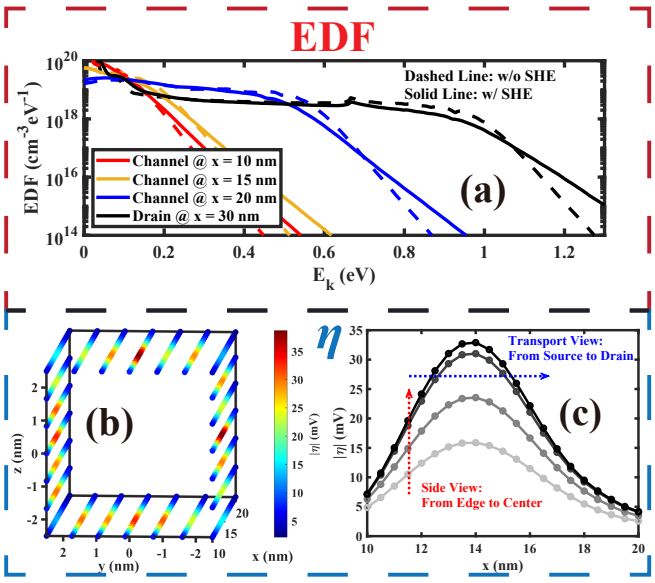

Fig. 10. (a) The EDF of different locations with and without SHE at $V_D = V_G = 1$ V. (b) The extracted $|\eta|$ on each interface grid node in 3D view. (c) The $|\eta|$ profile observed from the side view and transport view. Note that in this work, $|\eta|$ is extracted at $V_D = 0.7$ V.

Specifically, **Fig. 11**(a) illustrates that defect concentration near the source is initially low but accumulates over time, while that near the drain side remains consistently high with minimal variation. **Fig. 11**(b) shows that self-heating further exacerbates HCD by about 4.5 mV at 10^4 s. A comparison among the three NS layers shows highly similar HCD behavior, with only the middle layer exhibiting slightly more severe $|\Delta V_{th}|$ degradation, due to its slightly higher temperature.

Crystalline diamond-like carbon (DLC) has gained attention as a BOX material due to its exceptional thermal conductivity [15]. As shown in **Fig. 12**, replacing SiO_2 with a DLC layer reduces the peak temperature of the middle layer by 59 K and lessens HCD by 2.5 mV at 10^4 s. These findings demonstrate that optimized thermal design is crucial for both thermal management and HCD mitigation.

IV. CONCLUSION

Based on a rigorous transport and reliability model, this work proposes a full quantum simulation framework for SHE

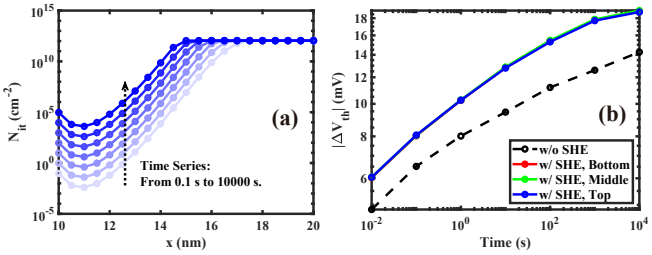

Fig. 11. (a) The interface traps generation along the transport direction over the aging time. (b) The $|\Delta V_{th}|$ degeneration of three different BEOL layers with and without SHE.

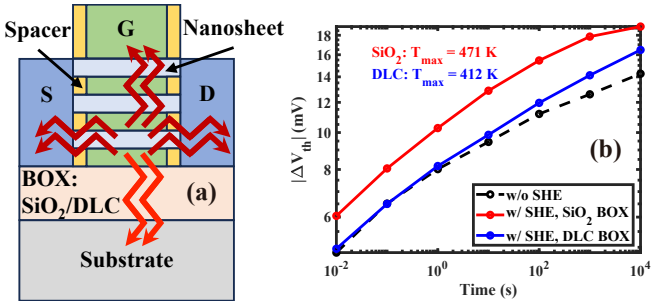

Fig. 12. (a) The structure of a NS FET with SiO_2 ($k_{th} = 1.4$ W/(K · m)) or DLC ($k_{th} = 2000$ W/(K · m)) as the BOX material, which is critical to the heat dissipation path indicated by the scarlet red arrow. (b) The $|\Delta V_{th}|$ degeneration of different BOX materials with and without SHE. Note that only the middle layer's degradation process is shown here since all three NS layers share similar HCD behavior according to **Fig. 11(b).**

and HCD in stacked NS GAA FETs that balances both accuracy and efficiency. The simulation results show a substantial temperature rise in the devices, with SHE significantly exacerbating HCD. Finally, our study of the BOX layer material underscores the vital role of optimized thermal design in ensuring both thermal and electrical reliability.

Acknowledgement

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