Device-to-Package Level Thermal Risk Analysis of the Back-Side Power Delivery Network

Dongun Shin
Computational Science and Engineering Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
dongun.shin@samsung.com

Jae Hee Choi
Computational Science and Engineering Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
joyful.choi@samsung.com

Takeshi Okagaki
Computational Science and Engineering Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
t.okagaki@samsung.com

Jeesoo Chang
Computational Science and Engineering Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
jess.chang@samsung.com

Eun Bi Nam
Computational Science and Engineering Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
eunbi95.nam@samsung.com

Yonghee Park
Computational Science and Engineering Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
central.park@samsung.com

Jinkyu Kim
Logic Technology Development Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
jkcool.kim@samsung.com

Hidenobu Fukutome
Logic Technology Development Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
h.fukutome@samsung.com

Hyeongsub Song
Process Design Kit Development Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
hs2020.song@samsung.com

SungJoon Park
Process Design Kit Development Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
sjune.park@samsung.com

Keun Hwi Cho
Logic Technology Development Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
keunhwi.cho@samsung.com

Sungjae Lee
Process Design Kit Development Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
sung-jae.lee@samsung.com

Dae Sin Kim
Computational Science and Engineering Team
Samsung Electronics Co., Ltd.
Hwasung-si, Republic of Korea
daesin.kim@samsung.com

***Abstract*—In this study, we present a novel approach to enhance the coverage and accuracy of 3D-FEM thermal simulations across the entire range from device-level to package-level by implementing an appropriate boundary modeling technique. The method was validated through the comparison of simulation results with a device under test element group measurements, which demonstrated a high level of consistency. We found that the back-side power delivery network has a significant impact on heat dissipation, with a 30.1% contribution to the thermal flow from the device through the back-side to the front-side back end of line. In a real product scenario, where multiple hotspots and package thermal resistance are considered, the lateral heat spreading is suppressed, leading to an increased contribution of the bonding layer and the sustain wafer from 16.0% to 93.3%.**

Keywords— self-heating effect, thermal simulation, multiscale, modeling, 3D-FEM, back-side power delivery network

I. INTRODUCTION

The competition of logic device scaling has been continued, but the total power consumption and operating frequency of a chip have stagnated since the mid-2000s, indicating a thermal bottleneck [1]. Furthermore, Back-Side Power Delivery Network(BSPDN), considered essential for sub-2nm, has greater concerns about the self-heating due to heat dissipation via the Front Side Back End of Line(FS-BEOL) and wafer bonding layer [2]. Therefore, it is crucial to have a simulation solution that accurately predicts heat transfer and device temperature. Although device-only electro-thermal simulation can accurately obtain both device performance degradation due to self-heating and lattice temperature, it introduces ambiguity in selecting Boundary Conditions. (B.C.) Fig. 1(a)(b) shows the results of a 3D TCAD electro-thermal device simulation as a preliminary study for this research. The results show that the device temperature rise due to self-heating is strongly influenced by the ambient temperature. Furthermore, variations in the thermal resistance of the BEOL significantly alter the distribution of heat flow among terminals, which suggests that inaccurate B.C. in device-level simulations can lead to misleading or unrealistic results.

Recently, there has been active research on heat dissipation of the whole system [3]. In addition, several commercial thermal simulation tools are able to cover the package-level; however, they have a resolution limit of several micrometers. We argue that a proper simulation solution at an intermediate scale with nanoscale resolution between the device and package-level is necessary, because the impact of lateral heat spreading is greater as it gets closer to the hotspot.

In this study, we present a novel method for extracting the reasonable thermal B.C. of 3D-FEM simulation through global-to-local analysis, and demonstrate that the model constructed by the new method provides predictable results,

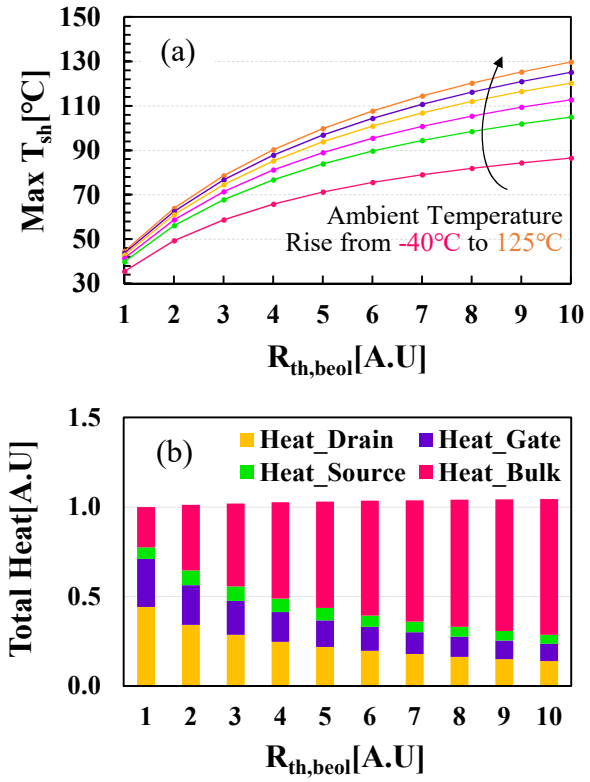

Fig. 1. 3D TCAD electro-thermal device simulation. (a) Escalation of self-heating when reflecting thermal resistances of the BEOL stack. Rth,beol=1 means that metal 1 is considered, and Rth,beol=10 means that metal 1 to top metal is considered. (b) Changes of the heat ratio exiting each terminal.

comparing them with measurements. By using the model, we quantitatively evaluate the contribution of each layer for device self-heating temperature rise. Moreover, we show that the self-heating results of a small IP block can differ from those of Device Under Test(DUT), because of the package thermal resistance and multiple hotspots.

II. Methodology

We created three types of the simulation structure - 1) BEOL metal patterned layers for extracting anisotropic effective thermal conductivities: $k_{eff,x}$, $k_{eff,y}$, and $k_{eff,z}$, 2) layer-wise structure without metal patterns, 3) full structure including from nanosheet devices to the bonding layer and a part of sustain wafer. Subsequently, 3D-FEM TCAD thermal simulation was executed following the simulation flow introduced in Fig. 2.

The layer-wise structure is described in Fig. 3, which is ultimately utilized to set the B.C. of the full structure. A rectangular uniform heat source is located in the center, characterized by a thickness of 40nm and a footprint equivalent to the active area of the full structure. The top and bottom B.C. are identical to those of the full structure, whereas the lateral B.C. are prescribed as adiabatic, thereby precluding heat transfer across these boundaries. To accurately simulate the thermal behavior of the layer-wise structure, $k_{eff,x}$, $k_{eff,y}$, and $k_{eff,z}$ of the BEOL layer are separately extracted from each metal-patterned layers. These extracted anisotropic effective thermal conductivities are subsequently applied to the layer-wise structure. The thermal properties employed in the simulation are listed in Table 1. The values of the silicon regions in Front End of Line (FEOL) and copper interconnects were determined considering the thickness dependency of thermal conductivity. As illustrated in Fig. 4, a lateral dimension of 50μm is adopted, as it ensures that the temperature near the lateral surfaces converges to the ambient temperature, indicating that the lateral heat spreading is fully reflected. Subsequently, the total heat flux through the virtual boundaries, as described in Fig. 3, is extracted. Ultimately, this extracted heat flux is imposed upon the full structure as a lateral heat flux B.C., thereby effectively accounting for the influence outside the simulation boundary.

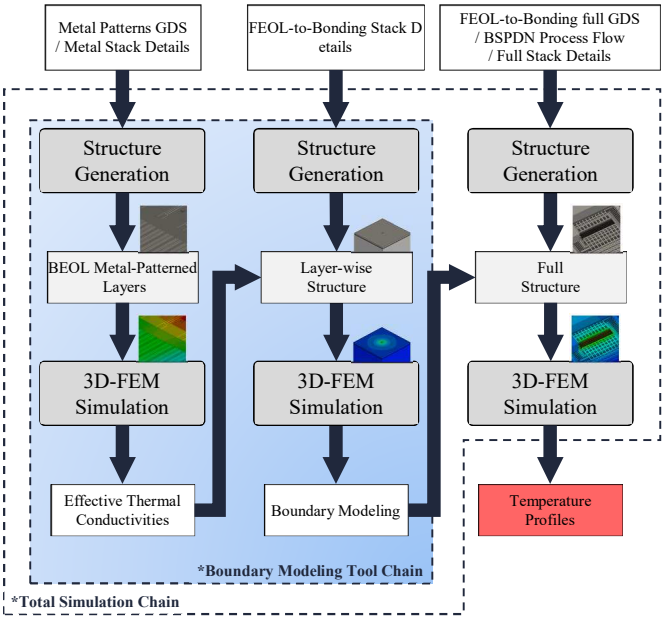

Fig. 2. Overall simulation flowchart. Three types of structures used in the 3D-FEM TCAD thermal simulations are illustrated. The region shaded in light blue indicates the novel boundary modeling technique developed in this work.

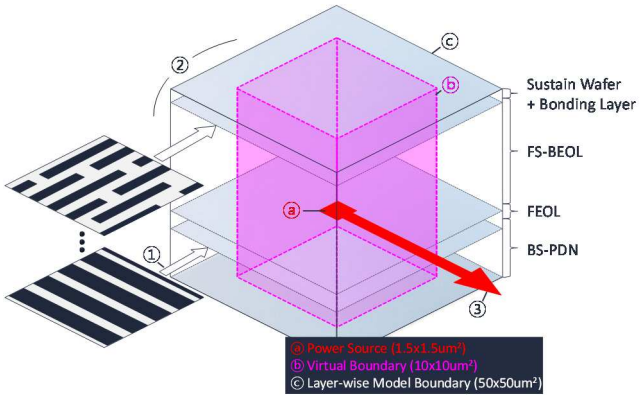

Fig. 3. Visualization of the boundary modeling toolchain using BEOL metal-patterned layers and a layer-wise structure. To determine the boundary conditions for the full structure, the following steps are performed. ① Extraction and application of the anisotropic thermal conductivities ② 3D-FEM thermal simulation with layer-wise structure ③ Extraction of lateral heat flux across the virtual boundaries

TABLE I. Thermal Conductivities Applied in the Simulation

Materials	Thermal Conductivity [W/m·K]
Silicon	20 – 148 [4]
Oxides	1.3
Nitrides	2.4
Gate	100
Source/Drain	50
Cu	153 – 385 [5]
Al	205
Bonding Layer	1.0

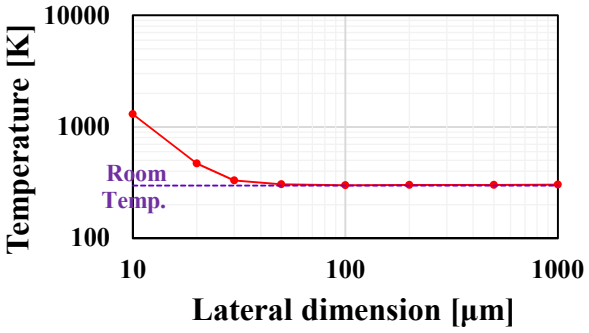

Fig. 4. Temperature rise at the side boundary induced by a centered heat source in the layer-wise structure, as a function of lateral dimension. A lateral dimension of 50µm is imployed for the simulation domain, because it adequately captures lateral heat spreading.

In the operation of actual products, multiple hotspots exist and package thermal resistance must be taken into account; therefore, additional simulations were conducted. First, a small IP block structure was constructed, and the power map extracted from Fusion Compiler was applied to nanosheet channels. Second, 1D package thermal resistance was added at the top and bottom of the structure and self-consistently solved within the 3D-FEM simulation. Finally, a side reflective B.C. was applied to account for the repetitive arrangement of blocks.

III. Results and Discussions

Fig. 5 shows (a) the 3D temperature profile and (b) the comparison of measured and simulated results of 10 Devices Under Test(DUT) with varying geometries. The measurements were obtained using the S-parameter based AC conductance method [6]. For DUTs with different active areas, appropriate Side Heat Transfer Coefficient (SHTC) values—separately extracted from the layer-wise model—were applied using the following equation, which conserves the total heat obtained from the layer-wise simulation.

$$Side\ Heat\ Flux = -SHTC\ (\ T - T_{ambient}\ ) \qquad (1)$$

Heat is generated in each nanosheet channel, and the device temperature is calculated as the average temperature of all channel materials, which closely corresponds to the temperature obtained from the AC conductance method. The squared of the Pearson correlation coefficient exceeds 0.9, demonstrating that the proposed methodology is sufficiently predictable. In other words, this approach enables the simulation of a reduced 10µm x 10µm structure with boundary modeling, eliminating the need to simulate the full 50µm x 50µm domain and thereby overcoming the size limitation of conventional simulation methods. With the exception of data point #1, which cannot be directly compared with other points due to the difference in technology nodes, and #8, whose measurement result is in doubt, all other data points exhibit consistent trends between simulation and measurements.

Fig. 6 illustrates the potential impact on the device temperature when it is assumed that the thermal conductivity of each layer is doubled. More specifically, the thermal conductivity of all materials within a given layer was doubled, and the resulting decrease in device temperature was computed. This procedure was repeated for all layers, and the reduction in device temperature calculated for each layer was quantitatively compared and represented as a percentage of the total, normalized to 100%. Regarding (a), although almost all heat is ultimately transferred to the sustain wafer connected to a perfect heat sink, the FEOL and BEOL regions, which have lower vertical thermal resistance but are closer to the heat source than the bonding layer and sustain wafer, contribute 17.8% and 36.0%, respectively. What is noteworthy is that the BSPDN has a 30.1% influence, representing the heat flow that is laterally spread along BS and then returned to FS-BEOL via FEOL. This implies that the heat dissipation design through BSPDN should be given due consideration.

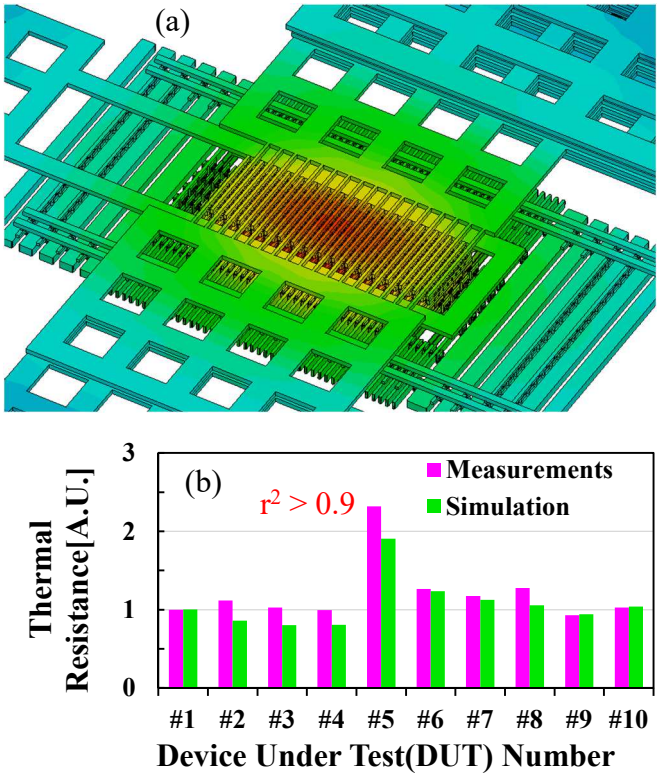

Fig. 5. (a) 3D Temperature profile of Device Under Test #1. Different SHTC values were applied to each material. (b) Comparison of measurement and simulation results.

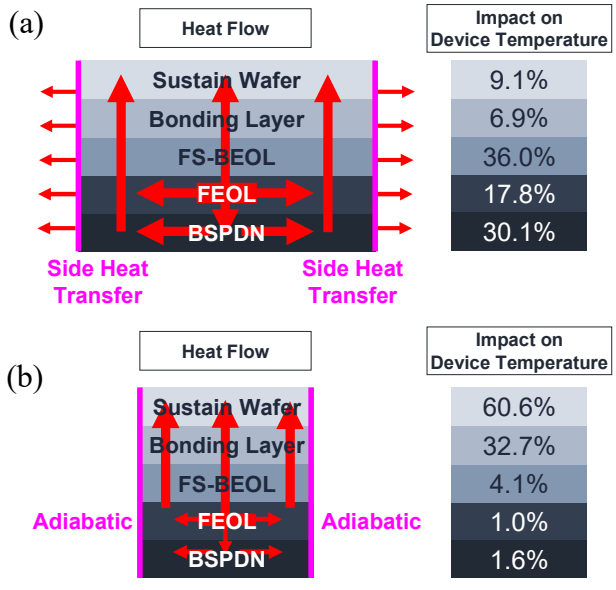

Fig. 6. Percentage of sensitivity to device maximum temperature. The impact of each layer was estimated assuming that its thermal conductivity was doubled. (a) Device Under Test (DUT) scenario (b) Product-like scenario.

Fig. 7 illustrates the 3D temperature profile of the small IP block with the power map applied. In actual chip design, the IP block is surrounded by other densely packed blocks, leading to additional heat sources outside the block. Therefore, it is reasonable adopting an adiabatic boundary condition for the simulation. Furthermore, the vertical package thermal resistance exacerbates this behavior. Under this assumption, the temperature distribution exhibits a significant vertical variation, even though the nonuniform heat generation from the nanosheet channels is already accounted for by the applied power map. Consequently, vertical thermal resistance plays a crucial role in heat dissipation, while lateral heat spreading is suppressed. As shown in Fig. 6(b), vertical heat flow becomes dominant across all regions, in contrast to the single-hotspot case where lateral spreading was more significant. Moreover, when package thermal resistance is included, the device temperature becomes highly sensitive to it. According to our simulation design and results, the package thermal resistance accounts for a significant portion of the total thermal resistance, emphasizing the importance of package-level heat sink design in scenarios where vertical heat flow dominates.

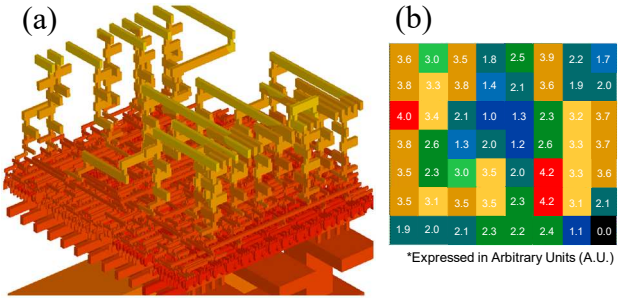

Fig. 7. (a) 3D Temperature profile of a small IP block with (b) 8x7 power map applied.

IV. Conclusion

The proposed multiscale thermal simulation model quantitatively analyzes the impact of not only lateral heat spreading but also the heat returning to the front side via BSPDN. Its high accuracy is validated through comparison with measurement results. The significance of this model lies in its ability to overcome the structural size and the number of mesh limitations inherent in conventional simulation methods. Furthermore, the simulation results show that the device temperature can increase significantly in scenarios involving the repeated logic blocks and package thermal resistance—where vertical heat flow dominates and the package thermal resistance has a substantial impact. This underscores the importance of considering multiscale aspects in future studies, ranging from lateral heat spreading in metal layers near logic devices to package-level thermal resistance, including the placement of local hotspots.

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