Thermal Resistance Decomposition of Packaging Solutions in Advanced CMOS Nodes

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***Abstract*—We have characterized the thermal dissipation P_{diss} of a single heat source using power amplifier (PA), from chip to package level, by using a combination of physical characterization and TCAD simulations. We do this for a 3D-FinFET in a die-attach package, and advanced FDSOI in a Quad-Flat-No-lead (QFN) package. Our differentiated approach eliminates the need for laterally replicated heat source (reflecting boundary condition), enabling a large simulation domain to be rapidly solved. Thermal resistances are extracted at all packaging levels using a decomposition simulation methodology. At P_{diss} ~ 1W, junction temperature rise T_J ~60C for die-attach and ~34C for QFN packages is observed. In both cases the printed circuit board (PCB) is a significant thermal barrier. We also identify the Cu-pillar region above the PCB in the die-attached package, and the epoxy in the QFN package, as critical regions for heat transfer. We report calibrated heat transfer coefficient values that can be used as boundary conditions in advanced 3D thermal packaging models.**

Keywords—TCAD, thermal resistance, thermal imaging, packaging, reliability

I. Introduction

Advanced packaging techniques are driving increased thermal and reliability challenges in technology nodes, requiring a stronger focus on adequate cooling [1-2]. An accurate thermal 3D profile is crucial to locate potential thermal bottlenecks, but predicting this ultimately depends upon a) mimicking the correct structure (lateral direction) and b) assuming appropriate boundary conditions of the packaged part (vertical direction). Note that, in contrast to some thermo-electrical simulation approaches for finding temperature profiles within a die, this work addresses the next level out: packaged chip on printed circuit board (PCB). In addition, experimental verification is inherently difficult [1].

The thermal resistance between two points is defined as $\theta_{12}=(T_1-T_2)/P_{diss}$, where P_{diss} is the power dissipated by the heat source. The primary interest for reliability is the total $\theta_{J\text{-}A}$ (junction-to-ambient) [2]. Once this is known (or predicted with confidence), one can assume an ambient T_2, and calculate the max power which will keep local temp T_1 below the design target. This total θ is readily decomposed into components (additive) to allow identification of critical regions.

To give confidence in our approach, we simulated two different packages - 3D-FinFETs [3] in a die-attach Cu-pillar package, and FDSOI [4] in a QFN package. Temperatures were measured by infrared (IR), and thermocouple, respectively. After calibration, we identify hotspots and show basic studies for lowering temperatures.

II. Simulation Setup

In the die, the PA is modeled as a heat-generating block in bulk Si, and the BEOL has an effective thermal conductivity (k_{th}) value (mix of Cu & oxide). In the PC board, the full GDS is mapped, including the thru-board Cu vias. For boundary conditions, in the lateral direction, we allow for an isolated heat source, without demanding it repeat (reflecting boundary condition). This differs from other published results, which use vertical thermal resistances to thermally describe the package, effectively reducing the package to a 1D problem [5-7]. Because of the distances required ($100\text{x}100\text{mm}^2$), and the concomitant large number of grid points, this is not easily addressed by conventional TCAD tools. In contrast, the software Heatwave [8] enables 3D simulation of very large grids but requires the structure to be modeled as a vertical stack of equal-area layers, with only conduction (not convection) allowed within / between layers. Any sidewall on the chip/package therefore becomes conduction heat transfer to a low thermal conductivity material mimicking air.

In the vertical direction, we desire reasonable estimates for the heat transfer coefficients to ambient. We use Robin (3^{rd}-kind) boundary conditions at the top and bottom of the package, which fixes T at some distance from the surface [9]. The top and bottom heat transfer coefficients are calibrated to match the temperature measurements. In addition, to obtain confidence in our "air = low-conductivity-solid" assumption, we ran simulations assuming a top layer of air, with a fixed temp at the top of this air layer and obtained similar heat fluxes at the package/air interface.

While one can argue that the PA is surrounded by many other heat-producing devices, the assumption is

that those are at much lower temps: if needed, they could be modeled as a field at elevated temp, leaving essentially the same problem – a point source in a flat-temp field.

III. 3D-FINFET DIE-ATTACH PACKAGE

A schematic cross-section of the 3D-FinFET-based PA with die-attach Cu-pillar package is shown in Fig. 1. The die is flipped (Si substrate is on top and the Back-End-of-Line (BEOL) is below the heat source. A typical simulated thermal profile is shown in Fig. 1b. Table I shows the dimensions and assumed k_{ths} (primarily from literature). IR measurements (Fig. 2a) were performed using a pre-calibrated, handheld FLIR camera, at different V_{DD} (P_{diss}), and used to calibrate the TCAD deck. A top view of simulated thermal profile is shown in Fig. 3a. In Fig. 3b we plot the vertical heat flux (W/m^2), which is mostly confined to the heat source region. Layouts near the heat source have a flux at least 10x higher than in any other region of the package, validating our desire to move away from 1D modeling.

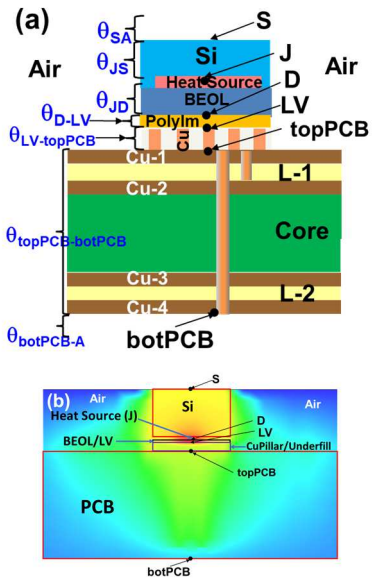

Fig. 1. a) 3D-FinFET die-attached cross-section schematic showing thermal resistance decomposition. A=Air, S=Top of substrate, J= Junction, D= interface between BEOL and LV, LV= bottom of LV layer, topPCB= interface between Cu pillars and PCB, botPCB= bottom of PCB. b) Front view thermal profile from simulation.

For calibration, the top and bottom heat transfer coefficients (h) are input variables. To match the temperature measurements, we fix those h values to ~7200 $W/(m^2*K)$ and ~3000 $W/(m^2*K)$, respectively. It is interesting that the estimates of h values are in the thousands and not in the tens or hundreds, as it is usually assumed for natural convection or forced convection boundary conditions, respectively [10]. In general, fixing the temperature is a very strong boundary condition since it implies a very high heat transfer coefficient (in the hundreds of thousands of $W/(m^2*K)$). Having this in mind, our h values reflect the fact that our Robin BC's fix the temperature somewhere away from the package. We also note that others [7] use similar h values to match their measured results, further validating our approach.

	X [um]	Y [um]	Z [um]	k_{th}= W/(K-m)
Air				0.024
Die substrate	1100	1100	700	Si (150 to 80)
Heat source	350	100	0.006	Si (150 to 80)
Die BEOL	1100	1100	21	27
LV(Polyimide)	1100	1100	2.9	0.5
Cu Pillar (75um)	1100	1100	73	398
Underfill	1100	1100	73	1
Cu-1 and Cu-4			38.1	398
Cu-2 and Cu-3			15.2	398
Diel L-1			101.6	0.66
Diel L-2			101.6	0.44
Core			1246	0.44
Air				0.024

Table I. 3D-FinFET die-attached dimensions and thermal conductivities used in simulations. Some kth values are temp dependent, so span a range.

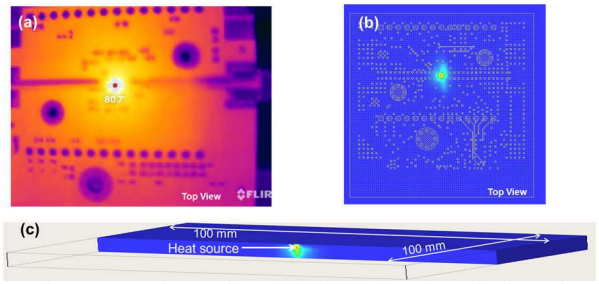

Fig. 2. a) 3D-FinFET die-attached IR measurement b) thermal simulation c) 3D simulation domain.

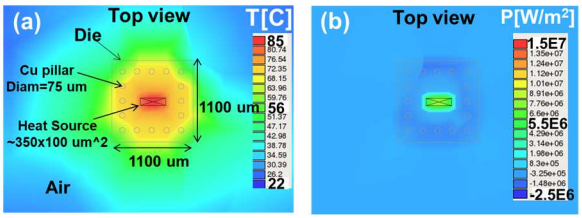

Fig 3. 3D-FinFET die-attached simulation profiles a) temperature and b) heat flux outputs in the plane-of-point J of Fig. 1a. (+ve=up, -ve=down).

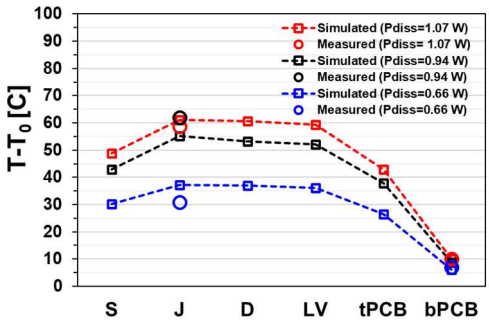

Fig. 4. 3D-FinFET die-attached simulated (square) and measured (circles) temperature rise ($T-T_0$) at P_{diss} of 0.66 W, 0.94 W and 1.07 W. All points/junctions are as described in Fig 1a. tPCB=top of PCB, and bPCB= bottom of PCB.

Simulated temperature rises defined as ($T-T_0$) are shown along with measurements in Fig. 4. Temperature remains constant going through the BEOL and final (LV) layers, and only starts to drop after reaching the Cu pillar. IR measurements were performed at the top of the flipped die and the bottom of the PCB. The Si substrate at the top of the die is transparent to IR therefore this measured top temperature corresponds to the doping junction temperature.

Figure 5 shows the comparison between top-down IR measurements (Microsanj EZ-THERM E2500A) and simulated temperature profiles at three different points across the package: at the die center, at the die edge, and at the top of the PCB not directly below the die. The comparison is very good, further validating the simulated 3D profile. The model indicates that roughly 50% of the heat flows out through the top surface, and 50% through the PCB.

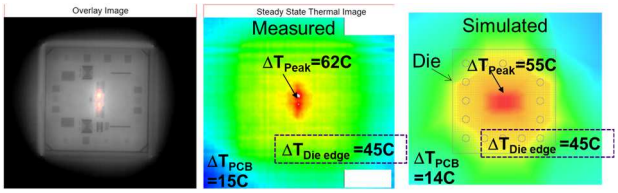

Fig 5. 3D-FinFET die-attached simulated vs measured temperature rise for $T_{Ambient}$=28C and P_{diss}=0.94W.

Having performed the model-hardware calibration to the outer surfaces, we decompose the thermal resistances described in Fig. 1a (see Table II): the key

Pdiss [W]=	0.66	0.94	1.07
Simulated	[C/W]	[C/W]	[C/W]
θ_{S-A} =	45.7	45.7	45.7
θ_{J-S} =	10.6	13.1	11.5
θ_{J-D} =	0.4	2.1	0.4
θ_{D-LV} =	1.2	1.3	1.3
$\theta_{LV-topPCB}$ =	14.6	15.2	15.3
$\theta_{topPCB-botPCB}$ =	30.8	30.9	30.9
$\theta_{botPCB-A}$ =	9.3	9.3	9.3

Table II. 3D-FinFET die-attached simulated thermal resistances at several P_{diss}. The fact that θ is independent of power means that the slope of ΔT vs. P_{diss} is linear as also electrically validated in [2].

resistance of interest θ_{JA} is simply a sum of its intermediate θs. We are not averaging temperatures across the whole package in this plane; we are extracting the maximum thermal resistances at each level of the package (center of the PA), which will identify possible improvement areas for reducing T_J. If we vary Cu pillar height from 0 to 75um (Fig. 6), we observe <5% improvement in ΔT_J. In Fig. 7 we decrease the Cu pillar diameter from 75um to 0 um, resulting in ~21% increase in ΔT_J. Decreasing the Core height has negligible effects on ΔT_J (not shown), as does varying the underfill thermal conductivity from 0.5 to 2.0 W/(m*K) (also not shown). In addition to the above structural variations, we did simulations at higher ambient temperature (T_0) of 75C (vs. 25C) and found only a 4% increase in ΔT_J.

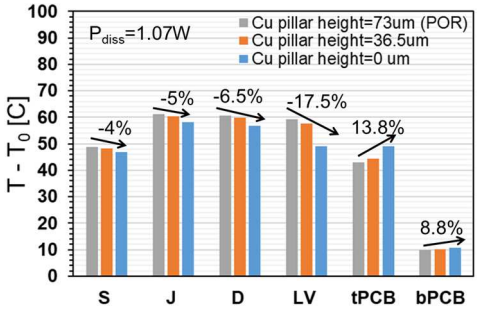

Fig 6. 3D-FinFET die-attached simulated temperature rise with varying Cu pillar heights. All points/junctions are described in Fig 1.

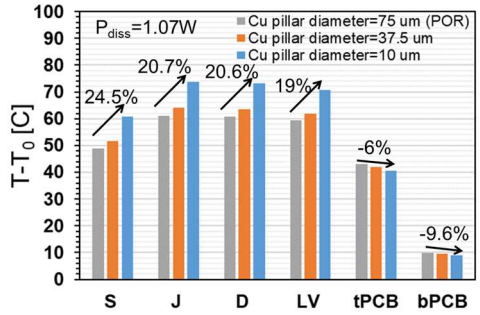

Fig 7. 3D-FinFET die-attached simulated temperature rise with different Cu pillar diameters. All points/junctions are described in Fig 1.

IV. FDSOI -QFN PACKAGE

A schematic of the advanced FDSOI-QFN package is shown in Fig. 8. In this case the die is not flipped. Below the die is an epoxy, a die pad, and solder paste layers that attach to the PCB layers [11]. Above the die

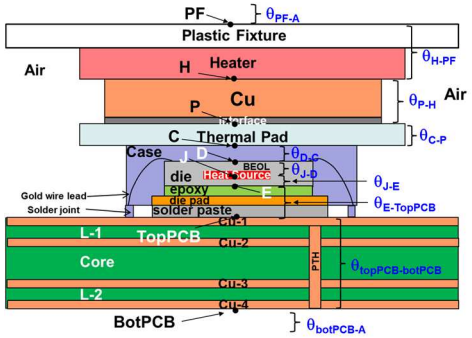

Fig. 8. FDSOI-QFN cross-section schematic with heater on top.

is a mold compound case, a thermal pad, and a Cu layer that attaches to a top heater with a plastic fixture on top of it. With the device powered off, the heater was set to several powers, and temp measurements were made via a thermocouple attached to the top of the thermal pad, enabling calibration of the materials above the die, unique to this setup. Then, with the heater turned off, we applied 1W to the amp, and selected top/bottom *h* values

(for Robin BC) to match the measured thermocouple reading. Table III shows the dimensions and assumed

	X [um]	Y [um]	Z [um]	k_{th}= W/(K-m)
Plastic Fixture	100mm	100mm	3e4	0.07
Heater	7620	6350	1270	170 to 82 (AlN)
Cu below heater	4013	4013	4267	398
Interface	4013	4013	1270	35
Thermal Pad	7620	7620	508	2.2
Case mold without leads	2630	2630	50	0.68 [*]
Case mold with leads	2630	2630	1046	100
Die BEOL	700	1225	21	27
Heat source	100	100	0.006	22
Die substrate	700	1225	775	Si (150 to 80)
Epoxy	700	1225	50	1.2 [*]
Die pad	1260	1260	200	385 [*]
Solder paste	1260	1260	50	78.4 [*]
Cu-1 to Cu-4	51mm	51mm	34	398
Diel L-1, L2	51mm	51mm	236	0.4
Core	51mm	51mm	966	0.4
Air				0.024

Table III. FDSOI-QFN package dimensions and thermal conductivities used in simulations. Some kth values are temp dependent, so span a range. *=from [11].

Thermal resistance	Simulated θ [C/W]
$\theta_{PF\text{-}A}$ = Plastic Fixture-to-Ambient	0.14
$\theta_{H\text{-}PF}$ = Heater-to-Plastic Fixture	8.7
$\theta_{P\text{-}H}$ = Thermal pad-to-Heater	0.4*
$\theta_{C\text{-}P}$ = Case-to-thermal pad	9.94
$\theta_{D\text{-}C}$ = Die-to-Case	14.1
$\theta_{J\text{-}D}$ = Junction-to-top of Die	1.2**
$\theta_{J\text{-}E}$ = Junction-to-Epoxy	22.9
$\theta_{E\text{-}TopPCB}$ = Epoxy-to-TopPCB	1.9
$\theta_{TopPCB\text{-}BotPCB}$ = TopPCB-to-BotPCB	5.2
$\theta_{BotPCB\text{-}A}$ = BotPCB-to-Ambient	4.4

Table IV. FDSOI-QFN simulated thermal resistances. *From heater calibration. **From BEOL calibration to measured Rth [from 12].

material properties [12]. We find best fits to data, assuming h values 15 W/(m^2*K) and 2400 W/(m^2*K)

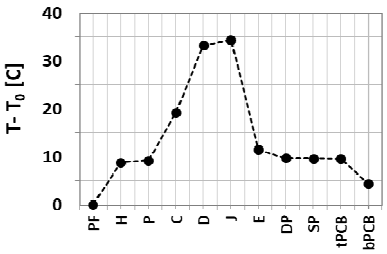

Fig. 9. FDSOI-QFN temperature rise at different points in structure for P_{diss}=1 W. All points/junctions PF, H etc are from Fig. 8.

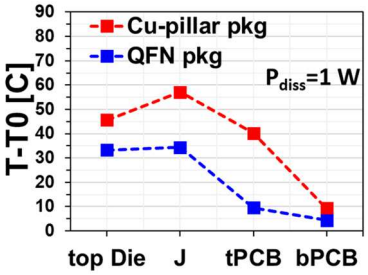

Fig. 10. Simulated temperature rise (T-T_0) for Cu-pillar die-attached and QFN packages at: the top of the die, Junction (J), top of PCB (tPCB), and bottom of PCB (bPCB) at T_0=25C.

for the top and bottom, respectively. In contrast to the die-attach package, here over 90% of the heat flows out through the PCB. Fig. 9 shows the simulated temperature rise at different points in a vertical slice through the structure; the junction/epoxy interface is the critical junction for heat dissipation. To mimic the effect of the leads, we assume a higher k_{th} (100 W/(K*m)) for the case material that touches the sides of the die. This lowers θ_{JA} by a factor of 2. Table IV shows the simulated thermal resistances. Fig. 10 gives a comparison of the temperature rise between Cu-pillar die-attached package and QFN package.

V. CONCLUSION

Using IR and thermocouple measurements, we have thermally characterized die-attach/3D-FinFET and QFN /FDSOI packages, and well-modeled them with 3D-TCAD simulations. We report thermal resistances and heat transfer coefficients for both. At P_{diss} ~ 1W, junction temperature rise T_J ~60C for die-attach and ~34C for QFN packages is observed. Apart from the PCB, we identify the critical regions for heat flow to be the Cu-pillar region above the PCB in the die-attached package, and the epoxy in the QFN package. We report calibrated heat transfer coefficient values that can be used as boundary conditions in advanced 3D thermal packaging models. This methodology can readily be implemented for other types of packages.

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