

Modeling and Analysis of Electron Trapping Mechanisms in $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ and $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4/\text{SiO}_2$ Charge Trap Devices

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Abstract — This work analyzes the electron trapping mechanisms in $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ (AN) and $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4/\text{SiO}_2$ (ANO) charge trap devices using Sentaurus technology computer-aided design (TCAD) simulations. The simulation results are compared with measurements of fabricated devices and show good agreement, validating the accuracy of the model. Two injection mechanisms—Fowler–Nordheim (FN) tunneling and direct injection—are considered, and their impact on the spatial distribution of trapped electrons is investigated under varying programming voltage (V_{PGM}) and programming time (T_{PGM}). In addition, threshold voltage shift (ΔV_{th}) characteristics are analyzed with respect to temperature, trap energy level (E_t), and tunneling effective mass (m^*). These findings provide insight into the structural dependence of trapping behavior and support accurate modeling of charge trap memory devices.

Keywords— Charge trap device, Electron Trap, TCAD simulation, Tunneling

I. INTRODUCTION

Charge trap devices have gained considerable interest for nonvolatile memory applications due to their excellent scalability, integration capability, and retention performance [1]. Among various charge trapping structures, $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4$ (AN) and $\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4/\text{SiO}_2$ (ANO) devices have emerged as promising candidates owing to their process simplicity, compatibility, and potential for low-voltage operation and high reliability. The key structural difference between these two configurations lies in the presence (ANO) or absence (AN) of a tunneling oxide layer, which fundamentally alters the dominant electron injection and trapping mechanisms [2–4]. This structural variation directly influences the spatial distribution of trapped charges during program operations.

Despite the importance of such investigations, a detailed comparative analysis of the injection mechanisms and trapping characteristics between AN and ANO devices remains underexplored. In this work, we perform Sentaurus technology computer-aided design (TCAD) simulations to investigate the electron trapping behavior in both structures [5]. By varying key physical parameters, we analyze the spatial distribution of trapped electrons and the resulting threshold voltage shift (ΔV_{th}), thereby providing deeper physical insight into the structure-dependent trapping mechanisms in charge trap memory devices.

II. TCAD MODELING FOR AN AND ANO DEVICES

Sentaurus TCAD simulations were conducted to analyze and compare electron trapping behaviors in AN and ANO charge trap devices. Fig. 1(a) shows the schematic of the simulated ANO device, where the detailed fabrication process is described in [6]. The gate insulator consists of Al_2O_3 (A, 7 nm) as the blocking oxide, Si_3N_4 (N, 4 nm) as the charge trap layer, and SiO_2 (O, 3 nm) as the tunneling oxide. Beneath the stack, the undoped poly-Si (P, 20 nm) serves as the channel, while the source and drain, which supply electrons during the program operation, are formed using n^+ poly-Si (S and D, respectively). The AN device shares the same structure, except that the O layer is excluded. Figs. 1(b) and (c) compare the structural configurations and electron trapping mechanisms of the ANO and AN devices, emphasizing the differences caused by the presence of the O layer. In the ANO device, as illustrated in Figs. 1(d) and (f), electrons are injected from the channel and subsequently trapped in the N layer after passing through the O layer via Fowler–Nordheim (FN) tunneling, following the conventional program operation of flash memory.

In contrast, the AN device exhibits two distinct trapping mechanisms, as shown in Figs. 1(e) and (g). First, FN tunneling can still occur through the N layer, resulting in electron trapping primarily near—but not exactly at—the A/N interface. This is attributed to potential interfacial reactions between A and N, such as the formation of SiO_xN_y and the presence of oxygen-deficient regions, which may locally reduce trap efficiency [7]. Second, direct injection takes place when the conduction band of the poly-Si channel aligns with the trap energy levels in the middle of the N layer [8]. Due to the absence of the tunneling oxide and the occurrence of direct injection, the AN device facilitates deeper electron trapping compared to the ANO device.

Here, the dotted line denotes the trap energy level (E_t), which is located between the conduction band edge (E_c) and the valence band edge (E_v) [9]. As E_t increases (i.e., moves further below E_c), the traps become deeper and are capable of capturing more injected electrons. In this work, both FN tunneling and direct injection mechanisms are considered, and the simulation parameters—including E_t , spatial trap distribution, and tunneling effective mass (m^*)—are set to reflect the distinct characteristics of each mechanism.

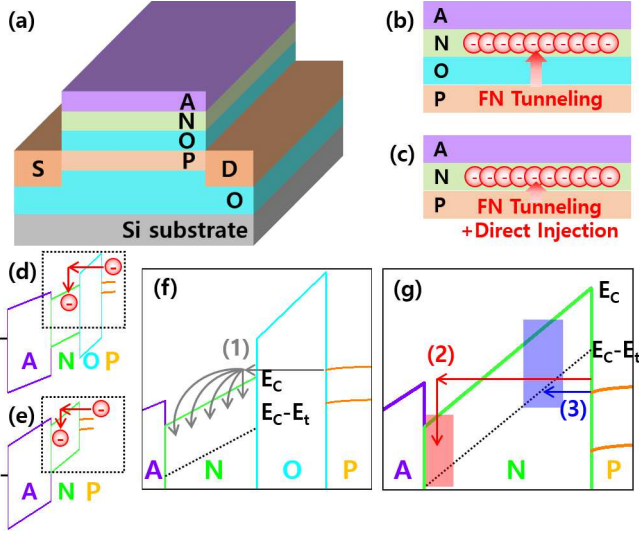


Fig. 1. (a) Schematic of the device and gate insulator structure. (b) ANO and (c) AN device structure. Electron trapping in the (d), (f) ANO and (e), (g) AN devices during program operation.

III. SIMULATION RESULTS AND ANALYSIS

To validate the proposed trapping model, TCAD simulations were conducted under various programming voltages (V_{PGM}) and programming times (T_{PGM}), and the results were compared with measured data. The key outcomes are summarized in Figs. 2 and 3. Fig. 2(a) shows the spatial trap distribution model adopted in this work. This model was carefully constructed to reflect the physical trapping behavior, incorporating both direct injection toward the middle of the N layer and FN tunneling near the A/N interface, as described in Section II. As a result, this leads to a non-uniform trap profile across the N layer. Since a flat spatial trap distribution resulted in weak representations of both FN tunneling and direct injection, this model was insufficient, and thus a non-uniform profile, as shown in Fig. 2(a), was adopted to better reflect their distinct injection regions.

Fig. 2(b) presents the simulated spatial distribution of trapped electron density (n_t) in AN and ANO devices after 1 second of programming operation. Although the same trap distribution model from Fig. 2(a) was applied to both AN and ANO devices, the resulting electron trapping profiles differ significantly. In the AN device, electrons accumulate both near the middle of the N layer and close to the A/N interface, reflecting the influence of both FN tunneling and direct injection. In contrast, the ANO device exhibits electron trapping primarily near the middle of the N layer, with a smaller portion trapped near the N/O interface. Due to the presence of the tunneling oxide, direct injection is effectively blocked, limiting the injection path to FN tunneling alone and making it difficult for electrons to be trapped near the A/N interface. This distinction highlights the critical role of the tunneling oxide in modulating both the depth and directionality of electron trapping.

Figs. 2(c) and (d) illustrate how the spatial n_t profile varies with V_{PGM} for AN and ANO devices, respectively. In the AN device, minimal trapping is observed at $V_{\text{PGM}} = 4$ V due to the insufficient electric field strength; FN tunneling does not occur, and only a small amount of direct injection takes place. As V_{PGM} increases, FN tunneling becomes active, and the

contribution from direct injection increases significantly, resulting in a deeper and more spatially distributed trapping profile, which is consistent with the intended shape shown in Fig. 2(a). In the ANO device, the tunneling oxide layer significantly suppresses electron injection at lower voltages. Only when V_{PGM} exceeds 6 V does FN tunneling through the O layer become strong enough to produce noticeable trapping. As V_{PGM} increases, more electrons are trapped toward the middle of the N layer, forming a broad trapping profile. At $V_{\text{PGM}} = 8$ V, the trapped electron density becomes comparable to that of the AN device at $V_{\text{PGM}} = 6$ V, clearly indicating that a higher voltage is required to overcome the tunneling barrier formed by the O layer.

The time dependence of trapping behavior is shown in Figs. 2(e) and (f). For the AN device under $V_{\text{PGM}} = 6$ V, the n_t profile gradually increases with time due to the combined contributions of FN tunneling and direct injection. The resulting distribution exhibits a two-directional trapping profile, with electrons accumulating from the A/N interface toward the middle of the N layer. For the ANO device programmed at 8 V, n_t also increases with T_{PGM} ; however, since only FN tunneling is present, a one-directional trapping profile is observed. Electrons are initially trapped near the N/O interface and gradually extend toward the middle of the N layer. These results confirm that the presence of the O layer raises the threshold voltage required for effective electron trapping and effectively suppresses direct injection, leading to a fundamentally different trapping profile compared to the AN device.

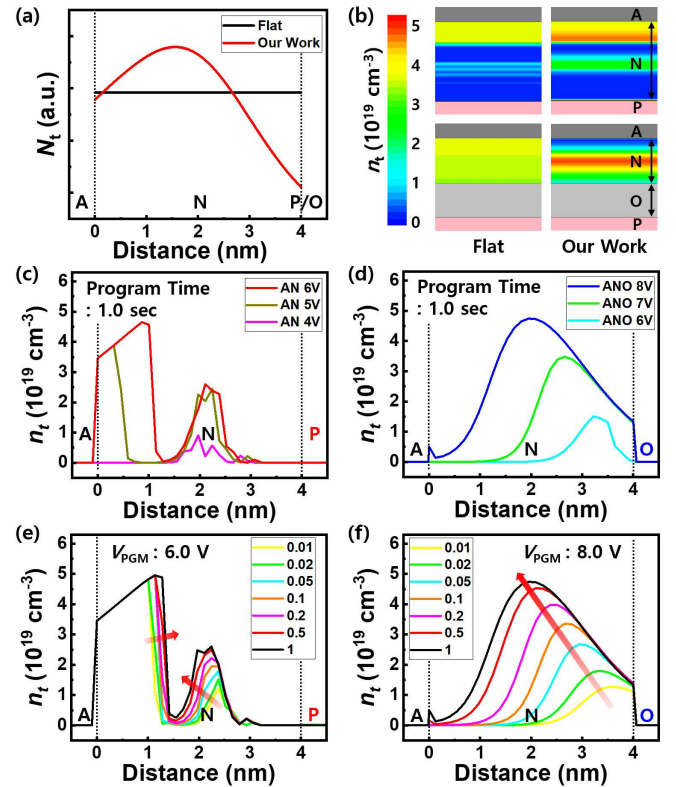


Fig. 2. (a) Spatial trap distribution model adopted in this work. (b) Spatial distribution of trapped electrons in AN and ANO devices. Simulated n_t distribution as a parameter of V_{PGM} at 1 second for the (c) AN and (d) ANO devices. Simulated n_t distribution as a parameter of T_{PGM} for the (e) AN device at $V_{\text{PGM}} = 6$ V and (f) ANO device at $V_{\text{PGM}} = 8$ V.

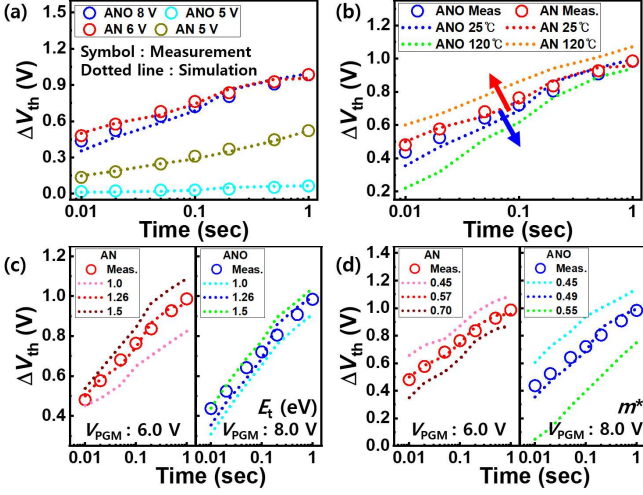


Fig. 3. (a) Comparison of measured and simulated ΔV_{th} for AN and ANO devices. Variation in ΔV_{th} depending on (b) temperature, (c) E_t (varied in the N layer for both devices), and (d) m^* (N layer for AN, O layer for ANO).

Fig. 3 compares the measured and simulated ΔV_{th} under various conditions to validate the proposed trapping model. This comparison serves as a critical check on the accuracy and physical validity of the simulation. Fig. 3(a) shows the time-dependent ΔV_{th} characteristics of AN and ANO devices under different V_{PGM} . The simulation results (dotted lines) closely match the measured data (symbols). In the AN device, ΔV_{th} increases significantly when V_{PGM} exceeds 5 V, which aligns with the activation of FN tunneling and direct injection discussed in Fig. 2(c). In contrast, the ANO device exhibits negligible ΔV_{th} at $V_{PGM} = 5$ V due to the suppression of electron injection through the tunneling oxide. At this voltage, the field strength is insufficient to drive a meaningful tunneling current through the O layer, resulting in limited charge trapping. This behavior can also be explained by the following expression for trap probability:

$$\text{Trap probability} \propto \exp(-2O_{thk}\sqrt{2qm^*E_b/\hbar}) \quad (1)$$

Here, O_{thk} represents the tunneling oxide thickness, q is the elementary charge (1.602×10^{-19} C), E_b is the barrier height for electron tunneling, and \hbar is the reduced Planck constant (\hbar divided by 2π) [10]. This expression shows how tunneling behavior is influenced by both material and geometric parameters. A notable increase in ΔV_{th} is observed at $V_{PGM} = 8$ V, indicating that a higher electric field is required to enable FN tunneling through the O layer. Notably, the ΔV_{th} of the ANO device at 8 V is comparable to that of the AN device at 6 V, as discussed in Fig. 2.

Fig. 3(b) demonstrates the temperature dependence of ΔV_{th} . Interestingly, the AN and ANO devices exhibit opposite trends with temperature, despite both showing increased ΔV_{th} over time. In the AN device, the absence of a tunneling oxide allows electrons to be trapped relatively deeper in the nitride layer [11]. These deeply trapped electrons are generally less susceptible to thermal emission, and the increased carrier energy at higher temperatures enhances injection efficiency, leading to increased ΔV_{th} . On the other hand, the ANO device, dominated by shallow traps near the N/O interface [12], shows a decrease in ΔV_{th} with temperature. This is attributed to thermally activated emission and lateral redistribution of electrons away from the channel region, effectively reducing the number of trapped charges. Therefore, the thermal

response of ΔV_{th} serves as further evidence of the different trapping depths and mechanisms in AN and ANO devices.

The effect of E_t on ΔV_{th} is illustrated in Fig. 3(c), where E_t was varied in the N layer of both devices. In the AN device, where deep traps are more abundant, higher E_t values (i.e., deeper trap levels) lead to enhanced trapping capacity and result in a notable increase in ΔV_{th} . This is because deeper traps can retain more injected electrons and are less likely to release them via thermal emission, thereby contributing more significantly to the overall charge storage. While increasing E_t enhances the trap probability in both AN and ANO devices, the effect is more pronounced in AN. In the ANO device, the presence of the tunneling oxide limits the injection mechanism to FN tunneling through a thick energy barrier formed by the O layer, thereby reducing the sensitivity of electron trapping to changes in E_t . As a result, deeper traps become less accessible even at higher E_t . In contrast, the AN device supports both FN tunneling and direct injection, allowing electrons to reach deeper trap sites more efficiently as E_t increases. This contrast further supports the interpretation that trapping in ANO predominantly occurs in shallow states near the interface [13].

Fig. 3(d) investigates the influence of m^* on ΔV_{th} . Since the tunneling layer is different in the two structures, m^* was varied in the N layer for the AN device and in the O layer for the ANO device. In both cases, a lower m^* increases the tunneling probability, resulting in higher ΔV_{th} , which is consistent with the FN tunneling mechanism [14]. This trend is also described by equation (1), where the trap probability increases as m^* decreases. A smaller m^* reduces the effective barrier width, thereby facilitating electron injection and improving trapping efficiency. Notably, the ANO device exhibits a more sensitive response to changes in m^* , indicating that electron injection is more strongly governed by the tunneling properties of the O layer.

IV. CONCLUSION

In this study, TCAD-based simulations were conducted to analyze the electron trapping behavior in AN and ANO charge trap devices, and the results were successfully matched with experimental measurements. Both FN tunneling and direct injection mechanisms were considered to examine electron trapping in the N layer in terms of spatial distribution, V_{PGM} , and T_{PGM} . Furthermore, ΔV_{th} characteristics were analyzed with respect to temperature, E_t , and m^* . The simulation results revealed distinct trapping profiles and sensitivities for AN and ANO devices, depending on the structural differences and dominant injection paths. This work provided valuable physical insight into the underlying trapping mechanisms in charge trap memory structures and offered guidance for optimizing future device designs.

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REFERENCES

- [1] Goda. A, et al., *Electronics*, 10, 24, 3156-3171, 2021.
- [2] K. A. Nasyrov, et al., *Journal of Experimental and Theoretical Physics*, 102, 5, 810-820, 2006.
- [3] C-H. LEE, et al., *Appl. Phys. Lett.*, 86, 15, 152908, 2005.
- [4] T. Ishida, et al., *IEEE Transactions on Electron Devices*, 60, 2, 863-869, 2013.
- [5] Sentaurus Device Manual, Synopsys, Santa Clara, 2013.
- [6] M-K. Park, et al., *Advanced Electronic Materials*, 10, 4, 2300866, 2024.
- [7] J. Park, et al., *Microscopy and Microanalysis*, 19, S5, 109-113, 2013.
- [8] F. J-Molinos, et al., *J. Appl. Phys.*, 91, 8, 5116-5124, 2002.
- [9] Yu. N. Novikov, et al., *J. Appl. Phys*, 136, 1, 014101, 2024.
- [10] T. H. Kim et al., *Appl. Phys. Lett.*, 85, 4, p660, 2004.
- [11] B-J Yang, et al., *IEEE Transactions on Electron Devices*, 65, 2, 2018.
- [12] Y. J. Seo, et al., *Appl. Phys. Lett.*, 92, 132104 2008.
- [13] TH. Kim, et al., *Appl. Phys. Lett.*, 85, 4, 660-662, 2004.
- [14] E. Nadimi, et al., *IEEE Transactions on Electron Devices*, 55, 9, 2462-2468, 2008.