Unveiling fast interface trap dynamics in monolayer MoS_2 FETs

Rittik Ghosh*, Alexandros Provias*, Alexander Karl*, Rajarshi Roy Chaudhuri†, Dominic Waldhör*, Theresia Knobloch*, Christoph Wilhelmer*, and Tibor Grasser*
*Institute for Microelectronics, TU Wien, Gusshausstrasse 27–29, 1040 Vienna, Austria
†Institute of Solid State Electronics, TU Wien, Gusshausstrasse 25, 1040 Vienna, Austria
Email: {ghosh|grasser}@iue.tuwien.ac.at

***Abstract*—Two-dimensional materials like molybdenum disulfide (MoS_2) are viable candidates for future ultra-scaled stacked nanosheet field-effect transistors. For current transistor prototypes based on 2D materials, a hysteresis in the transfer characteristics is often observed. Threshold voltage hysteresis in 2D FETs is typically ascribed to insulator traps. While fast interface traps are typically associated with changes in the subthreshold swing, here we show that they can also contribute to the hysteresis at low temperatures and fast operating frequencies. We employ the full quantum-mechanical non-radiative multi-phonon model to analyze trap-mediated charge transition in monolayer (1-L) MoS_2 FETs at 300 K and 77 K. Simulating the trap responses over a wide range of parameters reveals that, depending on the trap properties, the charge transition is either thermally activated or dominated by nuclear tunneling. We further demonstrate that the hysteresis of thermally activated traps can shift into the measurement window at low temperatures.**

***Index Terms*—2D materials, MoS_2 FETs, fast interface traps, reliability, hysteresis, physics-based models**

I. Introduction

Monolayer (1-L) molybdenum disulfide (MoS_2) has emerged as a promising channel material due to its large direct band gap (E_G) and decent mobility (μ) at sub 1 nm thickness [1], [2]. However, unfavorable band alignments and immature processing frequently result in observed hysteresis (ΔV_h) in the $I_D(V_G)$ transfer characteristics [3]–[5]. While slow border traps are responsible for ΔV_h at room temperature, interface traps are too fast to contribute and hence lie outside the typical measurement window of hysteresis measurements at room temperature [3], [6]. In particular, charge traps associated with MoS_2 itself typically show a small time constant distribution due to the crystalline nature of MoS_2 [3], [7]. Measurement methods that can be used to study fast interface traps at room temperature include admittance spectroscopy, hence capacitance voltage measurements on suitable test structures with a large enough area, and current transient spectroscopy [8], [9].

This work sheds light on the mechanisms of charge transitions (CTs) at interface traps in 1-L MoS_2 FETs at cryogenic temperatures, which has recently been the focus of several experimental studies [10]–[12]. We analyze the CTs using a full quantum-mechanical nonradiative multi-phonon (NMP) model [13] and derive their theoretical hysteresis ΔV_h response at different frequencies and temperatures. Within the harmonic approximation, potential energy curves (PECs) of distinct diabatic electronic states are modeled within a grid of trap levels (E_T), relaxation energies (E_R) and the configuration coordinate change (ΔQ). We evaluate the temperature dependence of the CTs and thereby identify which parameter combination allows a trap to contribute to the hysteresis ΔV_h in the transfer characteristics at cryogenic temperatures. We show that particular traps with small ΔQ are remarkably temperature-insensitive and typically do not exhibit ΔV_h measurable using the frequency ranges employed for conventional $I_D(V_G)$ curves (mHz to kHz) [10], [14]. Furthermore, by systematically sampling the three-dimensional trap parameter space (E_T, E_R, ΔQ) and tracking the sweep frequency response at 300 K and 77 K, we provide a theoretical understanding of the temperature dependence of hysteresis.

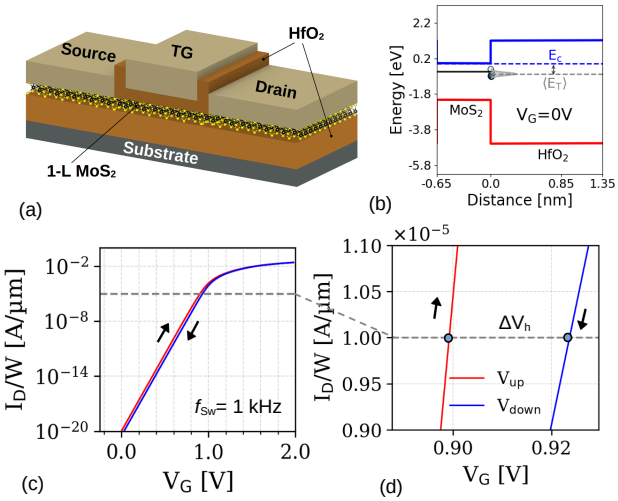

Fig. 1. (a) Schematic of a top-gated MoS_2 FET used in our TCAD simulations. (b) Energy band diagram at flatband conditions showing traps at the MoS_2/HfO_2 interface with mean trap level $\langle E_T \rangle$ = 0.48 eV below E_C. (c) Simulated $I_D(V_G)$ for up/down sweeps at f_{Sw}=1 kHz. (d) Magnified view of ΔV_h extracted at $I_{th}=10^{-5}$ A/µm.

This work was supported by the Austrian Science Fund (FWF) through the doctoral college TU-DX and the European Research Council (ERC) under Grant agreement no. 101055379 (F2GO)

II. TCAD MODELING

The schematic of a top-gated 1-L MoS_2 FET as simulated with our 1-D TCAD simulator Comphy [14], [15] is shown in Fig. 1(a). The device geometry is based on MoS_2 FETs recently reported by Intel [16] with a 0.65 nm thin MoS_2 channel with E_G= 2.06 eV [17] and a 4.3 nm HfO_2 top gate oxide with E_G= 5.7 eV along with their electron affinities (χ_s) amounting to 4.2 eV [18] and 2.7 eV [19] respectively. The gate work function (E_W) and the channel mobility (μ) are set to 5.2 eV [20] and 80 cm^2/Vs [21] respectively. We use the same device dimensions as in [3] with W=1 µm and L= 5 µm. Fig. 1(b) shows the energy band diagram with interface traps at V_G= 0 V. Fig. 1(c) presents the simulated $I_D(V_G)$ at a sweep frequency of $f_{Sw} = 1$ kHz and Fig. 1(d) highlights ΔV_h in a magnified view.

III. ANALYSIS OF THE CHARGE TRAPPING MECHANISMS

The fast interface traps with an assumed density of $N_{it} = 10^{12}$ cm^{-2} [3] are modeled using the full quantum mechanical (QM) NMP charge transition rates based on Fermi's golden rule [22]:

$$k_{12}(T) = \frac{2\pi}{\hbar} |\theta_{12}|^2 \frac{1}{Z} \sum_{\alpha\beta} |\langle \eta_{1\alpha} | \eta_{2\beta} \rangle|^2 \times \delta(E_{1\alpha} - E_{2\beta})\, e^{-E_{1\alpha}/(k_B T)} \quad (1)$$

Here, θ_{12} represents the electron-phonon coupling matrix element, $E_{1\alpha}$ and $E_{2\beta}$ are the vibrational eigenenergies with indices α and β of the initial and final charge states 1 and 2. $\eta_{1\alpha}$ and $\eta_{2\beta}$ are the vibrational wave functions and Z is the canonical partition function.

According to eq. (1), the CT is governed by the overlap of the vibrational wave functions $|\langle \eta_{1\alpha} | \eta_{2\beta} \rangle|$. For this reason, a CT can also occur below the intersection point (IP) of the traps PECs, including the vibrational ground state. This is shown for an exemplary trap with weak electron-phonon coupling in Fig. 2(a). The IP is also often labeled as the classical energy barrier of the charge transition [13], [14], [23]. Conversely, CTs occurring far below the IP are referred to as nuclear tunneling (NT) processes in this work.

The PECs for a trap with strong electron-phonon coupling are sketched in Fig. 2(b). Because there is only a vanishing overlap of the vibrational wave functions in the ground states, CTs can almost exclusively occur when higher vibrational states become occupied by thermal excitation. Such traps are therefore referred to as thermally activated (TA) in this work.

Using the simulation setup described in Section II, we calculated the impact of a single trap on the time-dependent threshold voltage shift (ΔV_{th}) of $I_D(V_G)$ employing the charge-sheet approximation (CSA):

$$\Delta V_{th}(t) = -Q_t \frac{t_{ox}}{\varepsilon_0 \varepsilon_r W L} \quad (2)$$

Thereby, the charge at the trap is treated as a uniform sheet parallel to the 2D channel/oxide interface [3], [15]. Q_t is the product of elementary charge and the trap occupation probability, t_{ox} denotes the oxide thickness, ε_0 is the vacuum permittivity, and ε_r is the relative permittivity of the oxide. ΔV_{th} describes the change in the threshold voltage due to the additional charge at the interface trap Q_t caused by capture of an electron.

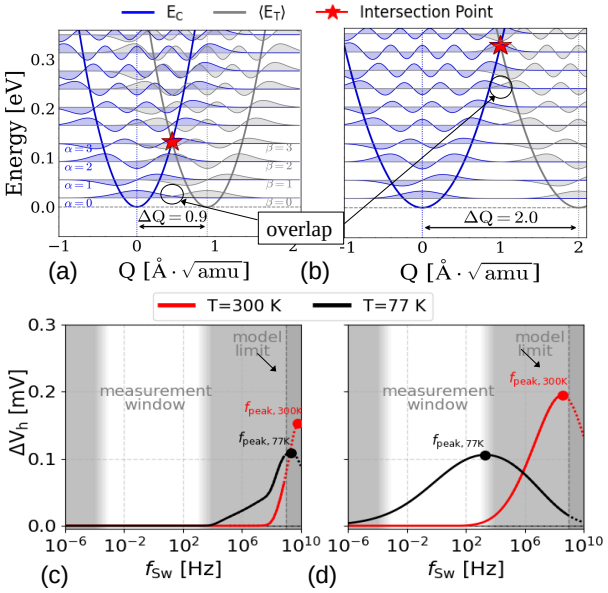

Fig. 2. PECs within the harmonic approximation including the vibrational wave functions $\eta_{\alpha,\beta}$ for two selected trap combinations: (a) NT dominated trap with weak electron-phonon coupling compared to a TA trap with strong coupling in (b). Simulated ΔV_h vs f_{Sw} for (c) the NT trap and (d) the TA trap at $T = 77$ K and 300 K. Shaded regions indicate f_{Sw} outside the typical measurement window.

The frequency at which ΔV_h peaks, denoted as f_{peak}, is temperature dependent and can be extracted to characterize the dynamic behavior of the trap. ΔV_h as a function of f_{Sw} for a NT dominated trap is shown in Fig. 2(c) for $T = 77$ K and $T = 300$ K. f_{peak} exhibits a small shift when the temperature changes, because even QM tunneling retains a slight temperature dependence [24]. However, the hysteresis still remains outside of the measurement window at $T = 77$ K in this case. On the contrary, for a TA trap, f_{peak} moves inside the measurement window at lower temperatures as shown in Fig. 2(d). Were remark that the applicability of our TCAD model at f_{Sw} exceeding approximately 1 GHz is unclear, primarily due to limitations of the drift-diffusion model [25] and the frequency-dependent behavior of permittivity [26].

To further assess the contribution of fast traps on ΔV_h, we simulate their response across a wide range of sweep frequencies (f_{Sw}) considering a grid of trap parameters (E_T, E_R, ΔQ), with E_T ranging from the MoS_2 conduction band edge, E_C, to near midgap, E_R from 0.1 to 4.0 eV and ΔQ from 0.3 to 3.0 Å · $amu^{1/2}$ [22], each discretized with 10 steps.

A trap will only contribute to ΔV_h if it can capture (τ_c) an electron during the up sweep but is too slow to emit (τ_e)

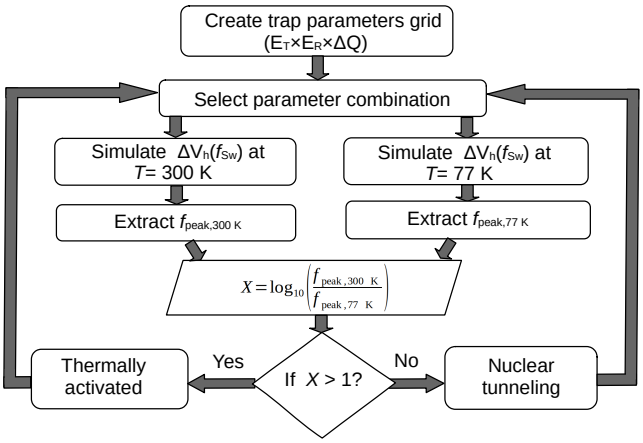

Fig. 3. Proposed simulation flow to identify trap-mediated charge transfer as either TA or NT dominated. For each combination of trap parameters (E_{T}, E_{R} and ΔQ), ΔV_{h} is simulated at 300 K and 77 K and the peak sweep frequency (f_{peak}) corresponding to maximum ΔV_{h} is extracted. The change in f_{peak} is quantified by $X = \log_{10}(f_{\mathrm{peak,300\,K}}/f_{\mathrm{peak,77\,K}})$.

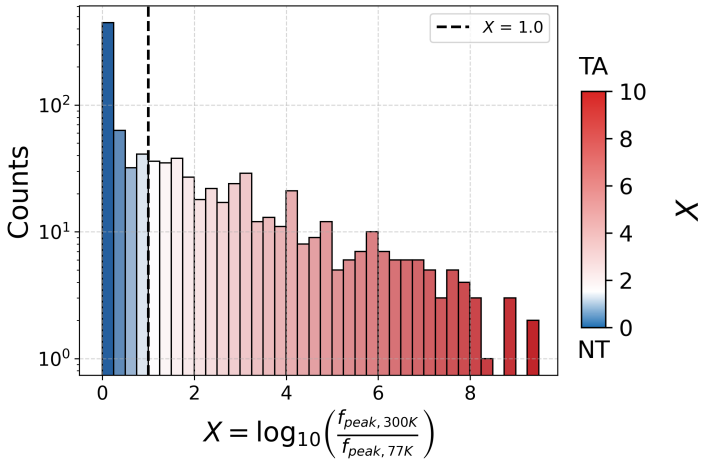

Fig. 4. Statistical classification of charge transfer mechanisms based on the log-scale criterion X across 1000 trap parameter combinations. Defects with $X > 1$ are classified as TA traps.

it during the down sweep, meaning $\tau_{\mathrm{c}} \ll \tau_{\mathrm{e}}$; $\tau_{\mathrm{c}} \ll 1/f_{\mathrm{Sw}}$ and $\tau_{\mathrm{c}} \gg \tau_{\mathrm{e}}$; $\tau_{\mathrm{e}} \gg 1/f_{\mathrm{Sw}}$ during the down sweep [3], [27]. Here, $\tau_{\mathrm{c}} = 1/k_{12}$ and $\tau_{\mathrm{e}} = 1/k_{21}$. Furthermore, the strong dependence of ΔV_{h} on sweep frequency ($f_{\mathrm{Sw}} = 1/t_{\mathrm{Sw}}$) is shown in Fig. 2(c-d) [3], [16], [28], [29].

Fig. 3 outlines the proposed simulation workflow, classifying CT due to fast interface traps as TA or NT dominated based on the criterion

$$X = \log_{10}\left(\frac{f_{\mathrm{peak,300\,K}}}{f_{\mathrm{peak,77\,K}}}\right) \tag{3}$$

with $f_{\mathrm{peak,300K}}$ and $f_{\mathrm{peak,77K}}$ denoting the peak frequencies at 300 K and 77 K, respectively. The criterion considers the impact of temperature on the time constant (τ) distribution. At lower temperatures the average defect capture and emission times τ increase, thereby shifting the overall observed hysteresis ΔV_{h} towards slower f_{Sw} [30].

Fig. 4 shows a statistical distribution of X across 1000 parameter sets, where $X > 1$ indicates TA behavior, caused by a significant shift of f_{peak} from 300 K to 77 K. For this reason, the upper limit of NT is chosen as X = 1. Fig. 5 depicts the distribution of X over the full defect parameters space. The properties of the two defects from Fig. 2(a) and (b) are also highlighted.

Typically, TA dominates at higher E_{R} and ΔQ (strong PEC coupling) while NT is favored at lower values (weak PEC coupling) [7], [14]. NT involves smaller ΔQ and thus larger vibrational overlaps, whereas larger ΔQ suppresses tunneling, leading to a more classical TA behavior [3], [22].

The Arrhenius plots for f_{peak} of six selected defects shown in Fig. 6 demonstrate the temperature-insensitivity of NT dominated traps while TA traps can become measurable at lower temperatures. This shows that even works that claim "hysteresis-free" transistors based on measurements at room temperature might very well show a sizable hysteresis under different measurement conditions, i.e. lower temperatures or faster sweep rates [31], [32].

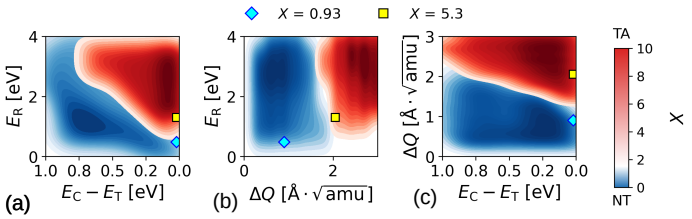

Fig. 5. Distribution of the criterion X as a function of the trap parameters across 1000 simulations: (a) E_{R} vs E_{C}-E_{T} (b) E_{R} vs ΔQ (c) ΔQ vs E_{C}-E_{T}. The red areas and blue areas indicate TA and NT dominated mechanisms, respectively. Here, the blue diamonds and the yellow boxes represent the NT and TA traps with parameters (E_{T}, E_{R}, ΔQ) discussed in Fig. 2(a) and (b).

IV. Conclusions

This work elucidates the dynamic behavior of fast interface traps in 1-L MoS_2 FETs using a full quantum-mechanical NMP model framework for identifying critical traps that will result in measurable ΔV_{h} or random-telegraph noise at lower temperatures. By mapping a broad trap parameter space and introducing a temperature-based classification criterion, we distinguish thermally activated and nuclear-tunneling-driven charge-transfer mechanisms. Our results highlight that even traps traditionally considered too fast to generate hysteresis at room temperature can become relevant under different measurement conditions, emphasizing the importance of comprehensive trap characterization for future 2D device reliability assessments.

References

[1] F. Schwierz, J. Pezoldt, and R. Granzner, "Two-dimensional materials and their prospects in transistor electronics," *Nanoscale*, vol. 7, no. 18, pp. 8261–8283, 2015.

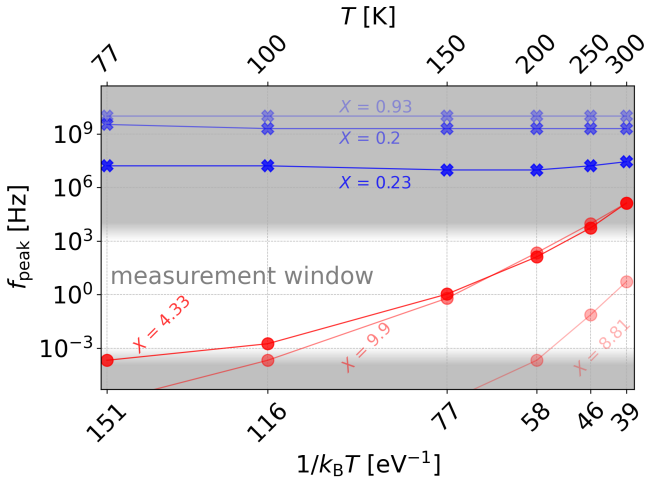

Fig. 6. Peak sweep frequency (f_{peak}) corresponding to maximum ΔV_{h} vs $1/k_{\mathrm{B}}\mathrm{T}$ for selected trap parameter combinations showing temperature insensitive NT (blue crosses) and TA mechanisms (red circles).

[2] Y. Liu, X. Duan, *et al.*, "Promises and prospects of two-dimensional transistors," *Nature*, vol. 591, no. 7848, pp. 43–53, 2021.

[3] R. Ghosh, A. Provias, A. Karl, C. Wilhelmer, T. Knobloch, *et al.*, "Theoretical insights into the impact of border and interface traps on hysteresis in monolayer MoS_2 FETs," *Microelectronic Engineering*, vol. 299, p. 112333, 2025.

[4] D. J. Late, B. Liu, H. R. Matte, V. P. Dravid, and C. Rao, "Hysteresis in single-layer MoS_2 field effect transistors," *ACS nano*, vol. 6, no. 6, pp. 5635–5641, 2012.

[5] I. M. Datye, A. J. Gabourie, C. D. English, K. K. Smithe, C. J. McClellan, N. C. Wang, and E. Pop, "Reduction of hysteresis in MoS_2 transistors using pulsed voltage measurements," *2D Materials*, vol. 6, no. 1, p. 011004, 2018.

[6] R. Ghosh, T. Knobloch, A. Karl, C. Wilhelmer, A. Provias, D. Waldhör, and T. Grasser, "Modeling the impact of interface and border traps on hysteresis in encapsulated monolayer MoS_2 based double gated FETs," in *2024 Austrochip Workshop on Microelectronics (Austrochip)*, pp. 1–4, IEEE, 2024.

[7] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectronics Reliability*, vol. 52, no. 1, pp. 39–70, 2012.

[8] A. Gaur, T. Agarwal, I. Asselberghs, I. Radu, M. Heyns, and D. Lin, "A mos capacitor model for ultra-thin 2D semiconductors: the impact of interface defects and channel resistance," *2D Materials*, vol. 7, no. 3, p. 035018, 2020.

[9] K. Taniguchi, N. Fang, and K. Nagashio, "Direct observation of electron capture and emission processes by the time domain charge pumping measurement of MoS_2 FET," *Applied Physics Letters*, vol. 113, no. 13, 2018.

[10] H. Ravichandran, T. Knobloch, A. Pannone, A. Karl, B. Stampfer, D. Waldhoer, Y. Zheng, N. U. Sakib, M. U. Karim Sadaf, R. Pendurthi, *et al.*, "Observation of rich defect dynamics in monolayer MoS_2," *ACS nano*, vol. 17, no. 15, pp. 14449–14460, 2023.

[11] H. Ravichandran, T. Knobloch, S. Subbulakshmi Radhakrishnan, C. Wilhelmer, *et al.*, "A stochastic encoder using point defects in two-dimensional materials," *Nature communications*, vol. 15, no. 1, pp. 1–11, 2024.

[12] S. M. Sattari-Esfahlan, A. J. Yang, R. Ghosh, *et al.*, "Stability and reliability of van der waals high-κ $SrTiO_3$ field-effect transistors with small hysteresis," *ACS nano*, vol. 19, no. 12, pp. 12288–12297, 2025.

[13] A. Alkauskas, Q. Yan, and C. G. Van de Walle, "First-principles theory of nonradiative carrier capture via multiphonon emission," *Physical Review B*, vol. 90, no. 7, p. 075202, 2014.

[14] D. Waldhoer, C. Schleich, J. Michl, A. Grill, D. Claes, A. Karl, T. Knobloch, G. Rzepa, J. Franco, B. Kaczer, *et al.*, "Comphy V3.0—a compact-physics framework for modeling charge trapping related reliability phenomena in mos devices," *Microelectronics Reliability*, vol. 146, p. 115004, 2023.

[15] G. Rzepa, J. Franco, B. O'Sullivan, A. Subirats, M. Simicic, G. Hellings, P. Weckx, M. Jech, T. Knobloch, M. Waltl, *et al.*, "Comphy—a compact-physics framework for unified modeling of bti," *Microelectronics Reliability*, vol. 85, pp. 49–65, 2018.

[16] A. Provias, T. Knobloch, A. Kitamura, K. O'Brien, C. Dorow, D. Waldhoer, B. Stampfer, A. Penumatcha, S. Lee, R. Ramamurthy, *et al.*, "Reliability assessment of double-gated wafer-scale MoS_2 field effect transistors through hysteresis and bias temperature instability analyses," in *2023 International Electron Devices Meeting (IEDM)*, pp. 1–4, IEEE, 2023.

[17] W. Hou, H. Mi, R. Peng, S. Peng, W. Zeng, and Q. Zhou, "First-principle insight into ga-doped MoS_2 for sensing SO_2, SOF_2 and SO_2F_2," *Nanomaterials*, vol. 11, no. 2, p. 314, 2021.

[18] S. Haastrup, M. Strange, M. Pandey, T. Deilmann, P. S. Schmidt, N. F. Hinsche, M. N. Gjerding, D. Torelli, P. M. Larsen, A. C. Riis-Jensen, *et al.*, "The computational 2D materials database: high-throughput modeling and discovery of atomically thin crystals," *2D Materials*, vol. 5, no. 4, p. 042002, 2018.

[19] J. Strand, P. La Torraca, *et al.*, "Dielectric breakdown in HfO_2 dielectrics: Using multiscale modeling to identify the critical physical processes involved in oxide degradation," *Journal of Applied Physics*, vol. 131, no. 23, 2022.

[20] R. Ghosh, "Performance investigation of dual trench split-control-gate MOSFET as hydrogen gas sensor: A catalytic metal gate approach," *IEEE Sensors Letters*, vol. 7, no. 5, pp. 1–4, 2023.

[21] Y. Zhang, H. L. Zhao, *et al.*, "Enhancing carrier mobility in monolayer MoS_2 transistors with process-induced strain," *ACS nano*, vol. 18, no. 19, pp. 12377–12385, 2024.

[22] J. Michl, A. Grill, D. Waldhoer, W. Goes, *et al.*, "Efficient modeling of charge trapping at cryogenic temperatures—part II: Experimental," *IEEE Transactions on Electron Devices*, vol. 68, no. 12, pp. 6372–6378, 2021.

[23] C. Wilhelmer, D. Waldhoer, M. Jech, A.-M. B. El-Sayed, L. Cvitkovich, M. Waltl, and T. Grasser, "Ab initio investigations in amorphous silicon dioxide: Proposing a multi-state defect model for electron and hole capture," *Microelectron. Reliab.*, vol. 139, p. 114801, 2022.

[24] H. Grabert, U. Weiss, and P. Hanggi, "Quantum tunneling in dissipative systems at finite temperatures," *Physical review letters*, vol. 52, no. 25, p. 2193, 1984.

[25] C. Jungemann, T. Grasser, B. Neinhuus, and B. Meinerzhagen, "Failure of moments-based transport models in nanoscale devices near equilibrium," *IEEE Transactions on Electron Devices*, vol. 52, no. 11, pp. 2404–2408, 2005.

[26] K. Deshmukh, S. Sankaran, *et al.*, "Dielectric spectroscopy," in *Spectroscopic Methods for Nanomaterials Characterization*, pp. 237–299, Elsevier, 2017.

[27] T. Knobloch, G. Rzepa, Y. Y. Illarionov, M. Waltl, F. Schanovsky, B. Stampfer, M. M. Furchi, T. Mueller, and T. Grasser, "A physical model for the hysteresis in MoS_2 transistors," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 972–978, 2018.

[28] N. H. Patoary, F. A. Mamun, J. Xie, T. Grasser, and I. Sanchez Esqueda, "Analysis and eot scaling on top-and double-gate 2D cvd-grown monolayer MoS_2 FETs," *Advanced Electronic Materials*, vol. 10, no. 11, p. 2400152, 2024.

[29] Y. Y. Illarionov, G. Rzepa, M. Waltl, T. Knobloch, A. Grill, M. M. Furchi, T. Mueller, and T. Grasser, "The role of charge trapping in MoS_2/SiO_2 and MoS_2/hBN field-effect transistors," *2D Materials*, vol. 3, no. 3, p. 035004, 2016.

[30] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Gös, and B. Kaczer, "The time dependent defect spectroscopy (tdds) for the characterization of the bias temperature instability," in *2010 IEEE international reliability physics symposium*, pp. 16–25, IEEE, 2010.

[31] S. K. Mallik, S. Sahoo, M. C. Sahu, S. K. Gupta, S. P. Dash, R. Ahuja, and S. Sahoo, "Salt-assisted growth of monolayer MoS_2 for high-performance hysteresis-free field-effect transistor," *Journal of Applied Physics*, vol. 129, no. 14, 2021.

[32] J. Tang, L. Liu, Y. Shao, X. Wang, Y. Shi, and S. Li, "A nanogapped hysteresis-free field-effect transistor," *Applied Physics Letters*, vol. 121, no. 2, 2022.