Modeling of PMOS Off-State Stress by introducing an energy resonant cross-section into the energy-driven hot carrier degradation model

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***Abstract*— The changes of off-current, threshold voltage, and on-current due to Off-Sate Stress on PMOS devices are successfully simulated by introducing an energy resonant form of the reaction cross-section instead of the Keldysh-like reaction cross-section in the energy-driven hot carrier degradation model, for changing the drain stress bias conditions. The degradation mechanism is analyzed, and the primary cause for the degradation is identified as Single Vibrational Excitation (SVE) by the secondary generated electron carriers at the drain side. It is demonstrated that additional hole traps at Si-Oxide interface can lead to a counter-intuitive decrease of the linear mode on-current, unlike saturation-mode on-current, and a turn-around effect at very long time and high drain bias stress.**

Keywords*— *Off-State Stress, Hot-Carrier, Degradation, Keldysh cross-section, Energy-driven, PMOS, Interface Trap

I. INTRODUCTION

Reliability is a very crucial characteristic of a device. Even if a device exhibits outstanding performance, one lacking reliability is unsuitable for mass production. Therefore, accurately estimating and predicting device lifetime is critical. Lifetime estimation via measurements under user bias conditions is time-consuming, often taking several months. To accelerate this, elevated temperatures and biases are typically applied to extrapolate lifetime from accelerated stress tests [1,2]. However, this could activate additional degradation mechanisms that would give small contributions under the user condition. Thus, it is important to develop a methodology to estimate lifetime quickly and cost-effectively. Simulation paired with a reliable degradation model offers an efficient approach for lifetime prediction under the user operation conditions.

Hot-carrier-induced degradation is a key reliability concern. Many modeling and simulation approaches have been proposed and shown to be successful in each applied area [3-13]. Recently, a fully atomistic approach provided fundamental understandings and well-matched simulation results for interface traps to device characteristics [11-13]. However, a full quantum approach takes time and would be appropriate for a simplified device structure. The previous approaches [3-10], especially, under energy-driven paradigm with SVE (Single Vibrational Excitation) and MVE (Multi-Vibrational Excitation) mechanisms, were successful. However, they also have some limited application ranges for biases, scaled or non-scaled devices, power devices and so on.

In this paper, Off-State Stress, which is the extreme case of hot carrier degradation at high drain bias and zero gate bias, is modeled and analyzed for PMOS device. Most of the previous researches focused on the drift of on-currents and threshold voltages, but off-current degradation is equally critical for standby applications. The previous energy-driven model [4], based on a Keldysh-form cross-section [14], fails at describing the change of the device's degradation under changing stress bias condition. It needs to be improved for the model to be predictive in estimating the lifetime of a device under user bias condition. Modification of the cross-section to include the energy-resonance in the interaction between carriers and Si-H bonds greatly enhances the accuracy for the bias-dependent degradation behavior of the model.

In the next sections, the device structure and the energy-driven hot carrier degradation model are introduced. Modification of interaction cross-section and analysis of the main degradation mechanism follow. And we suggest the possibility of an additional hole trap and its degradation for a turn-around effect [9,15-17] at long time stress.

II. Device Structure and Original Degradation Model.

A. Device Structure

The considered PMOS device has an n-doped poly-Si gate length of 0.22μm and an oxide thickness of 61Å. The structure and doping profile of a buried channel PMOS are shown in Fig.1. The initial characteristics of Vth, Ion, and Ioff have been calibrated. The stress drain biases are -5.5V and -6.6V.

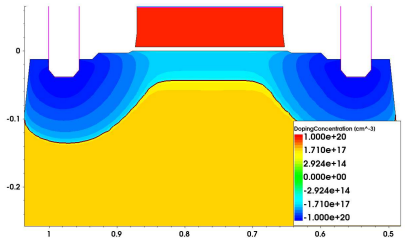

Fig. 1. Structure and doping profile for PMOS PSiON device.

B. Original Energy-Driven Degradation Model

The formulation used in this paper is based on Ref. [4]. The trap generation occurs via two pathways. One is SVE (Single Vibrational Excitation), in which a carrier with sufficiently high energy induces the vibration of a Si-H bond to break. The other is MVE (Multi-Vibrational Excitation), in which multiple carriers with low energies are coherently involved in the breakage of a Si-H bond. MVE becomes dominant when the density of carrier is high enough. For the simplicity, the formulation for SVE is introduced in this paper. The amount of generated interface trap by SVE is as follow.

$$N_{it,SVE}(t,\epsilon_{th}) = N_0\left[1 - e^{-k_{SVE}(\epsilon_{th})t}\right] \quad (1)$$

where N_0 is the maximum number of Si-H bonds. The reaction rate, $k_{SVE}(\epsilon_{th})$, is defined by the acceleration integral[5]

$$k_{SVE}(\epsilon_{th}) = \int_{\epsilon_{th}}^{\infty} f(\epsilon)g(\epsilon)v_g(\epsilon)\sigma_{SVE}(\epsilon,\epsilon_{th})d\epsilon \quad (2)$$

where $f(\epsilon)$, $g(\epsilon)$, $v_g(\epsilon)$are the carrier energy distribution , the density of states and group velocity, respectively. The reaction cross-section is given in the Keldysh-form [14] with a threshold energy, ϵ_{th}.

$$\sigma_{SVE}(\epsilon,\epsilon_{th}) = \sigma_0(\epsilon - \epsilon_{th})^p \quad (3)$$

In Ref. [4], an analytic function was used for carrier-energy distribution. In this paper, the 1st-order SHE-BTE is solved iteratively at each time step to consider the change of carrier energy distribution with time, together with Drift-Diffusion equation. MVE contribution and bond energy dispersion are also considered following the original formulation in Ref. [4].

The model shows a good match for the off-current drift at the relatively low bias of -5.5V stress with a tuned parameter set. But the mismatch of the off-current at -6.6V is very large as shown in Fig. 2 when the same parameter set is used. Using a parameter set calibrated at -6.6V gives under-estimation for the degradation at -5.5V (not shown).

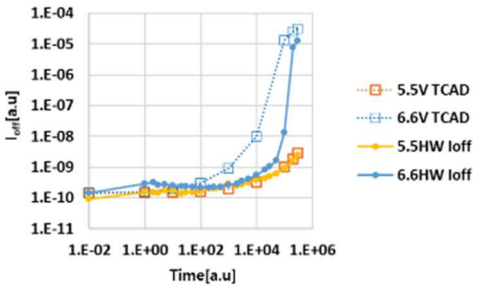

Fig. 2. Off-current changes for 5.5V & 6.6V stress bias with previous energy driven model[4]

III. Resonant Cross-Section and Degradation Mechanism

A. Application of Resonant Cross-Section

The above mismatch can be understood by looking into carrier energy distribution and the Keldysh-form cross-section, $(\epsilon - \epsilon_{th})^p$, Fig. 3. When the bias is increased, the carrier energy increases. The Keldysh-form cross-section is monotonically changing function. Especially high energy portion is greatly enhanced. Thus, All the high energy carriers get involved in Si-H bond breakage, which gives a large miss match for an increased bias. However, the carrier's interaction with Si-H bonds is quantum mechanical and energy-resonant. A fraction of the carriers would take part in the bond breakage. Thus, the Keldysh-like reaction cross section should be modified to consider the resonant interaction as follow.

$$\sigma(\epsilon,\epsilon_{res},\epsilon_{th}) = \frac{\sigma_0 \cdot \Delta_{SE}^2}{(\epsilon-\epsilon_{res})^2+\Delta_{SE}^2} \cdot (\epsilon - \epsilon_{th})^p \quad (4)$$

where ϵ, ϵ_{res}, Δ_{SE}, ϵ_{th}, σ_0 are a carrier energy, a resonant energy for a Si-H bond break, a resonance width, a threshold energy and a cross-section pre-factor, respectively. This has a similar form of the cross-section from quantum mechanical approaches[12,13]. This can be modified further to involve SVE-MVE mixing but the above is enough for the current condition, Off-State Stress. Here, the original Keldysh-form is maintained for calibration but 1 is used for the exponent p instead of 11 unlike in the previous results[4,5,7-10], even though it describes SVE. The calculated results are shown in Fig. 4, using the modified cross-section. The overall behaviors of off-currents, saturation mode on-currents, and threshold voltages are well matched to the experimental results for both of -5.5V and -6.6V stress voltages. In the used model, MVE is also considered but its contribution is very small because

the carrier density is not high enough in the Off-State situation.

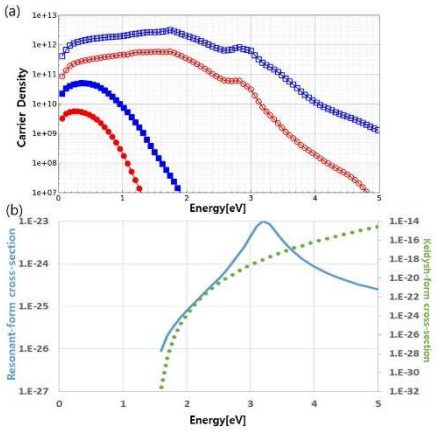

Fig. 3. (a) Energetic distributions of e/h carriers at drain side. (Open : electrons, Filled : holes ; Circle : 5.5V , Square: 6.6V). (b) Resonant-form cross-section(line) vs. Keldysh-form cross-section(Dot) with the exponent of 11.

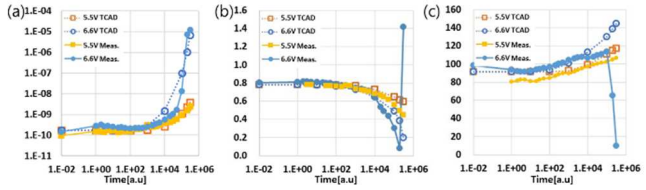

Fig. 4. Changes of (a)off-currents, (b)threshold voltages, and (c)saturation on-currents for 5.5V & 6.6V stress bias with the modified resonant cross-section.

The changes of off-currents, on-currents, and threshold voltages indicates the increase of negative charges due to interface trap. At very long time stress, the simulated results show under-estimation for threshold voltage and over-estimation for on-currents. The measured result shows even a turn-around effect for sufficiently long time stress at -6.6V. These facts lead to a suggestion for the existence of an additional mechanism which could be induced at a long time and high stress bias condition.

B. Main Degradation Mechanism

According to atomistic calculation, the SVE related bond-break energies are around 3eV for electrons and around 4eV for holes [12]. The electron carriers show high enough energies to break a Si-H bond but the hole carriers don't, as shown in Fig.3(a). The electron carriers are generated at drain side and accelerated to source side. Fig. 5 illustrates the band-to-band generation at the drain side, carrier energy distributions and current densities of electron and holes at 0 sec. The band-to-band generation occurs due to high bias applied to the drain side. Holes flow deep under the surface due to the buried-channel structure, while electrons travel right beneath the surface. Consequently, the secondary electrons generated at the drain side mainly dominate interface trap formation and some of electrons are trapped to give the effect from the negative charges. Fig. 6 shows the interface trap distribution along the channel direction and its evolution with the increase of stress time.

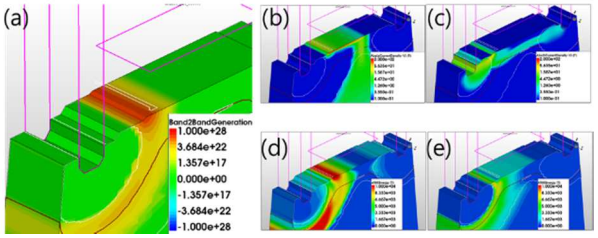

Fig. 5. (a) Band-to-Band generation rate profile. (b) electron current density (c) hole current density (d) spatial SHE energy distribution of electron carriers (e) spatial SHE energy distribution of hole carriers at time 0 sec.

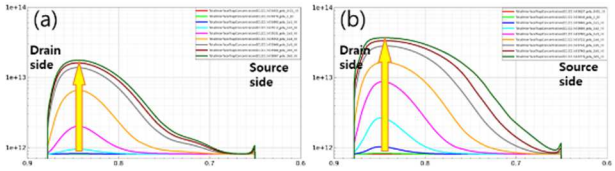

Fig. 6. The evolutions of the total interface trap concentrations for (a) -5.5V drain bias and (b) -6.6V drain bias, along the channel direction. The stress times are from 0.01 to 3e5.

C. Hole Trap Degradation

Experimental data (Fig.4) show a turn-around effect [9,15-17] in the threshold voltage and saturation-mode on-current under -6.6 V stress, absent at -5.5 V. Linear Id-Vg measurements at low drain bias (-0.1 V) confirm on-current degradation (Fig. 7). The decrease of threshold voltage and on-current occurs at the same time. This behavior is replicated in simulations by incorporating additional hole trap states alongside electron traps and its degradation with stress time. The additional hole traps might be due to nitrogen contents in the gate oxide due to Nitridation. This hole trap could be border or bulk trap in the nitrided gate oxide. The hole carrier density is increased near the silicon surface due to the negative charge effect of increased electron trap with respect to the stress time. It enhances the possibility of the hole tunneling into gate oxide. However, with a fixed hole trap density, the turn-around effect has not been reproduced so far. The increase of the hole trap density with time could model the turn-around effect until now. Trap energy levels affect the degree of overall degradation including the turn-around effect because their occupations determine the amount of trapped charges. Further investigation into trap sources and their energy distributions is required for precise lifetime estimation and degradation behavior.

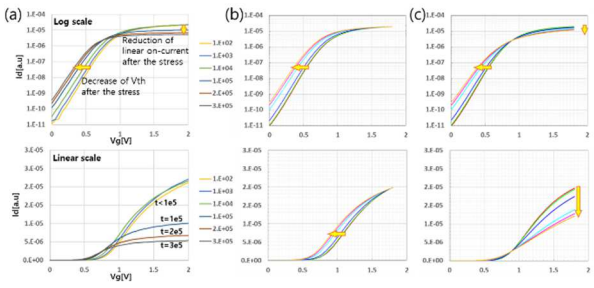

Fig. 7. Linear Id-Vg curves after the stress at -5.5V. (a) Measurement results. (b) TCAD results with the same amounts of e/h trap degradations. (c) TCAD results with additional hole trap degradation together.

IV. Summary

In summary, a resonant energy-dependent cross-section is introduced to model Off-State Stress in PMOS devices, capturing quantum mechanical interactions between carriers and Si-H bonds. The study identifies that additional hole traps contribute to the turn-around effect. The proposed cross-section modification should be validated for on-state hot-carrier degradation (where MVE is prominent), and deeper analysis of trap-state dynamics is warranted to enhance predictive accuracy.

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