3D Wide-Area TCAD Approach to Address Avalanche Breakdown in IGBT Edge Termination

M. Galvagno*, L. Zullino†, S. Mariani†, P. Zuliani†, S. F. Liotta‡, S. Cannizzaro‡, G. Malavena*, C. Monzio Compagnoni*, and A. S. Spinelli*

* Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy

† STMicroelectronics, via C. Olivetti 2, 20864 Agrate Brianza, Italy

‡ STMicroelectronics, stradale Primosole 50, 95121 Catania, Italy

***Abstract*—This work presents a novel approach to perform trustworthy three-dimensional (3D) wide-area Technology Computer-Aided Design (TCAD) simulations of avalanche breakdown at the device edge termination of an insulated gate bipolar transistor (IGBT). By i) skipping computationally-demanding 3D process simulations, ii) introducing suitable approximations in the trench-gate (TG) and source contact (SC) geometry, and iii) properly shaping the simulation domain, the proposed approach allows to accurately address all aspects of device breakdown with affordable computational burdens. That makes the approach a powerful solution for predictive analyses supporting the design of next-generation IGBT technologies.**

***Index Terms*—3D TCAD Simulations, Breakdown Voltage, Device Edge Termination, IGBT, Reliability**

I. Introduction

The trench-gate field-stop (TGFS) insulated gate bipolar transistor (IGBT) [1], [2] is among the most popular power semiconductor devices for electric vehicles, wind farms and photovoltaic power applications [3]–[5]. One of the most critical requirements that the device must fulfill is the capability to withstand a high source-to-collector voltage of the order of many hundreds of Volt or few kiloVolt in the OFF state [6], [7]. To achieve this fulfillment, in the design stage of the device special attention must be paid to the avalanche breakdown phenomenology. This does not mean just that the breakdown voltage (BV) of the device must be accurately predicted as a function of its design parameters. It also means that electrostatic nonuniformities, spots of high carrier generation by impact ionization, and current crowding effects must be carefully assessed and controlled to assure proper and reliable device operation. From the standpoint of avalanche breakdown, device edge termination represents the most critical region for modern IGBTs [8]. Due to the intrinsically 3D nature of this region, Technology Computer-Aided Design (TCAD) simulations based on 2D approaches [9], [10] do not allow to catch the essential physics for the accurate assessment of the device breakdown phenomenology. 3D approaches, instead, typically introduce unaffordable computational burdens, which could be relieved only by neglecting small geometric features or missing the careful description of carrier transport [11]–[13].

In this work, we propose a new 3D wide-area TCAD approach with workable computational load to investigate avalanche breakdown at IGBT edge termination. The approach allows to capture in detail all the aspects involved in the breakdown phenomenology, from the value of the breakdown voltage (BV) to the nonuniformities in the spatial profile of the electric field, of the impact ionization rate, and of the current flow. The approach, implemented by using a commercial tool [14], represents a powerful solution for accurate yet affordable TCAD-assisted design of next-generation IGBT technologies.

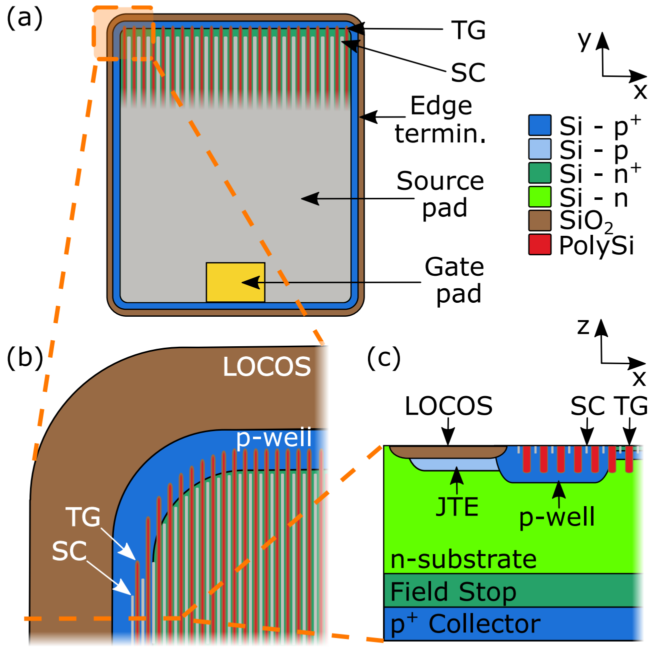

Fig. 1. (a) Schematic top view of the IGBT (the source pad has been softened at the top of the device to highlight the regions under it). (b) Magnified top view of device corner. (c) Side view of the edge termination.

II. Device Structure

State-of-the-art TGFS-IGBTs feature a complex edge termination, as shown in Fig. 1. This termination features three main elements: a Deep p-well, a junction termination extension (JTE) and a local oxidation of silicon (LOCOS) region. The

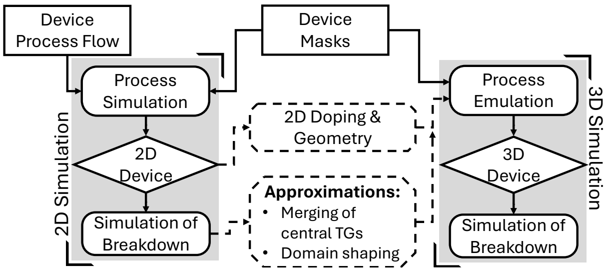

Fig. 2. TCAD simulation approach for avalanche breakdown at IGBT edge termination proposed in this work.

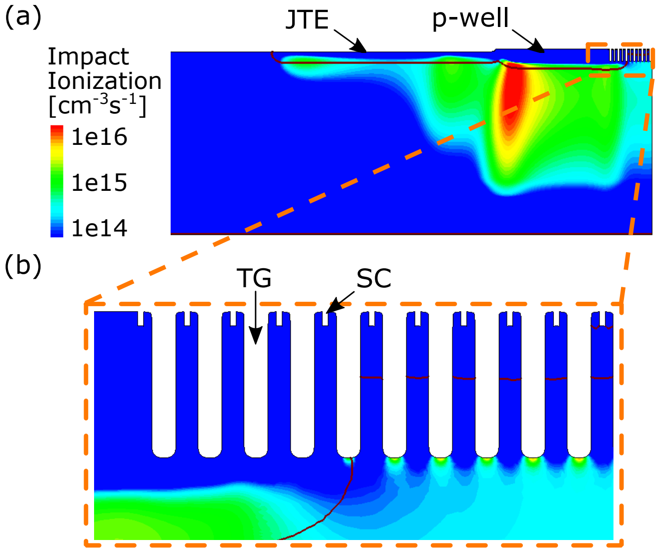

Fig. 3. (a) 2D device structure resulting from the scheme of Fig. 2 and simulation results for impact ionization at the onset of avalanche breakdown. (b) Magnified view of the region of the TGs, showing the negligible role played by its central part from the standpoint of impact ionization.

p-well wraps the upper and lower end of all the micrometer-sized polysilicon trench gates (TGs) and micro-trench source contacts (SCs) and the entire length of some lateral dummy TGs and SCs (dummy TGs and SCs lack the n^+ source region). The JTE and LOCOS regions lie at the side of the p-well. This termination scheme aims to mitigate electric field intensification at the edge of the active area of the device, increasing its BV. However, to achieve that outcome, a proper design of all of its regions is mandatory [15].

III. New 3D TCAD Simulation Approach

While a 3D simulation approach is mandatory to accurately reproduce the phenomenology of avalanche breakdown at the device edge termination, the adoption of such an approach is constrained by the computational burdens introduced by the fine geometry of TGs and SCs. Resolving this geometry structure through a proper simulation mesh, in fact, not only requires a number of nodes that is hardly manageable with ordinary computational resources but also raises severe issues from the standpoint of the numerical convergence of the simulations. To solve this conundrum, we developed the 3D simulation approach schematically depicted in Fig. 2.

The approach requires, first, a 2D process simulation to reproduce the geometry and doping profiles over a vertical cross-section of the device close to its edge termination and orthogonal to the TGs (the process flow and masks of a state-of-the-art IGBT technology were used in this work). Fig. 3 shows the resulting 2D device structure. A breakdown simulation is, then, carried out on the resulting 2D device structure for a preliminary inspection of device behavior. This simulation consists of the quasi-stationary solution of the coupled Poisson and continuity equations for electrons and holes for increasing collector voltage (V) up to the BV, with all the other contacts grounded. The latter voltage was easily identified as the voltage leading to a steep rise of the collector current (I). In the simulation, drift-diffusion transport was assumed for electrons and holes along with Shockley-Read-Hall generation/recombination and avalanche generation by impact ionization. Fig. 3 shows a colormap reproducing the resulting impact ionization rate in the 2D device structure very close to the BV. As expected, the device edge termination represents the most relevant region for avalanche breakdown, with a peak in the impact ionization rate appearing at the outer corner of the p-well. A minor role, instead, is played by the region of the TGs and SCs far from it.

Starting from the 2D device structure and simulation results, a 3D version of the device is built by avoiding computationally expensive 3D process simulations and relying on a simplified emulation procedure. As shown in Fig. 2, this procedure involves i) combining the vertical structure of the device obtained from 2D process simulations with the planar morphology information provided by the process masks; ii) merging all the TGs in the central region of the active area into a unique polysilicon plate, removing all the materials in-between them; iii) properly shaping the boundary of the central region of the active area to minimize the simulation domain. It is important to point out that, to correctly reproduce the current paths in the device, a patterned geometry was preserved for the end of the TGs and SCs and for the entire lateral dummy TGs and SCs. Fig. 4 shows the 3D device structure resulting from this scheme. On it, breakdown simulations are, finally, carried out as previously done on the 2D device structure.

IV. Results and Discussion

Fig. 5 shows a comparison of the I-V curves obtained from 2D and 3D simulations carried out on the device structure of Fig. 3 and Fig. 4, respectively. Results reveal that the BV predicted by 3D simulations is lower than that predicted by 2D simulations and more in agreement with the value obtained from experimental measurements on the state-of-the-art IGBT technology whose process flow is reproduced through the simulation scheme of Fig. 2. 3D simulations, indeed, offer a more correct description of the phenomenology of avalanche breakdown at the outer edge of the p-well than 2D simulations, correctly catching the change of field

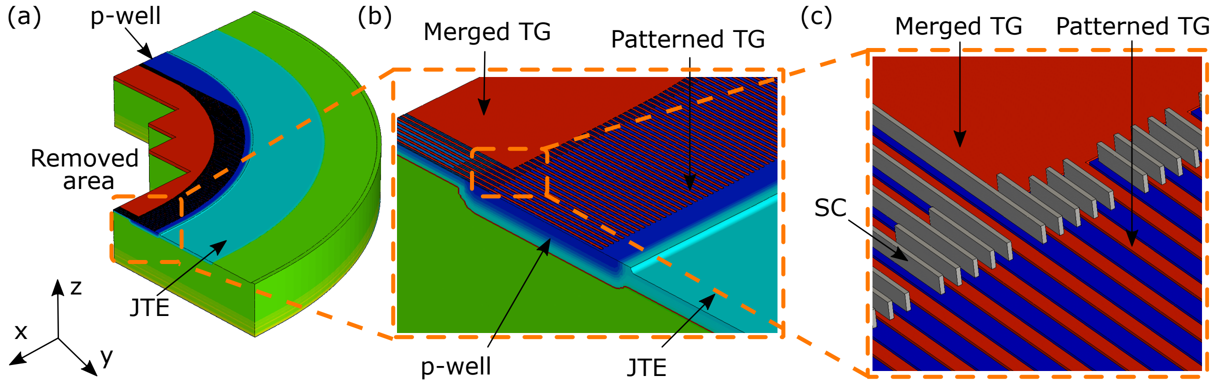

Fig. 4. (a) 3D device structure resulting from the simulation approach of Fig. 2. (b) and (c) are magnified views of the device, highlighting the transition from the merged TG area to the patterned TGs.

intensification and impact ionization along the curvature of that edge.

The change of the impact ionization rate along the curved edge of the p-well at the onset of breakdown resulting from 3D simulations is highlighted in Fig. 6. This change, of course, cannot be reproduced by 2D simulations, which therefore miss an important aspect of the breakdown phenomenology.

3D simulations not only provide a more accurate assessment of the device BV and of the spots where impact ionization is magnified with respect to 2D simulations. They also provide a more comprehensive view of the current flows through the device when the breakdown condition is approached. In this regard, Fig. 7 shows that reproducing the fine 3D array of TGs and SCs is mandatory to correctly catch the spatial profile of the current density and how the total current splits among the SCs.

Neglecting the patterned TGs, for instance, does not allow to reproduce the very strong current crowding towards the outermost dummy SC that appears when accounting for them (compare parts (a)-(b) with parts (c)-(d) of Fig. 7). The extreme SC, in fact, can be reached through a lower resistive path from the point of maximum carrier generation by impact ionization at the edge of the p-well region, with respect to the inner SCs, because it is not surrounded by TGs. As a consequence of that, it gathers most of the holes generated by impact ionization at the outer edge of the p-well region. That strong current crowding can be truly appreciated and optimized only through 3D simulations.

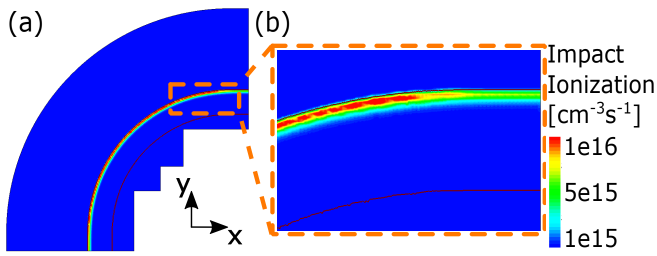

Fig. 6. (a) 3D simulation results for impact ionization at the onset of breakdown. (b) Magnified view of part (a) highlighting nonuniformities in impact ionization along the perimeter of the p-well.

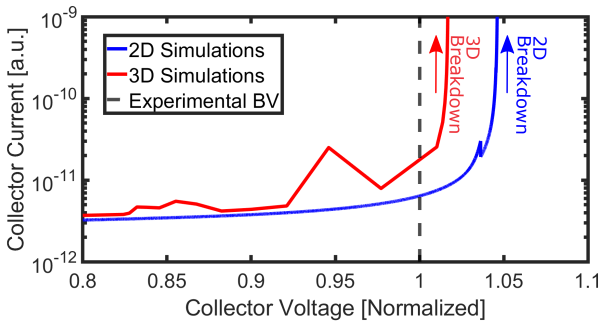

Fig. 5. Simulation results for the collector current vs. voltage near the BV, as resulting from 2D and 3D simulations. The collector voltage has been normalized to the experimental BV of the IGBT devices on which process simulations have been calibrated.

Finally, although including the patterned structure of TGs and SCs worsens the 3D simulation burden, Fig. 8 proves that such can be relieved to an affordable level by properly shaping the boundary of the central region of the active area. In particular, by looking at cases D1, D2, and D3 in Fig. 8, it appears clearly evident that removing a larger portion of the merged TG region allows to halve the time needed for the breakdown simulation on the 3D device structure thanks to a corresponding decrease in the number of simulation nodes (see part (b) of the figure). This reduced simulation burden does not involve any change in the assessment of the BV voltage and, more in general, in the accuracy of the simulation results (see part (c) of the figure). An excessive removal of the merged TG region, however, inevitably leads to failures in reaching convergence with the simulations (see case D4 in Fig. 8). This is due to an improper description of the device structure between the outermost TGs and p-well.

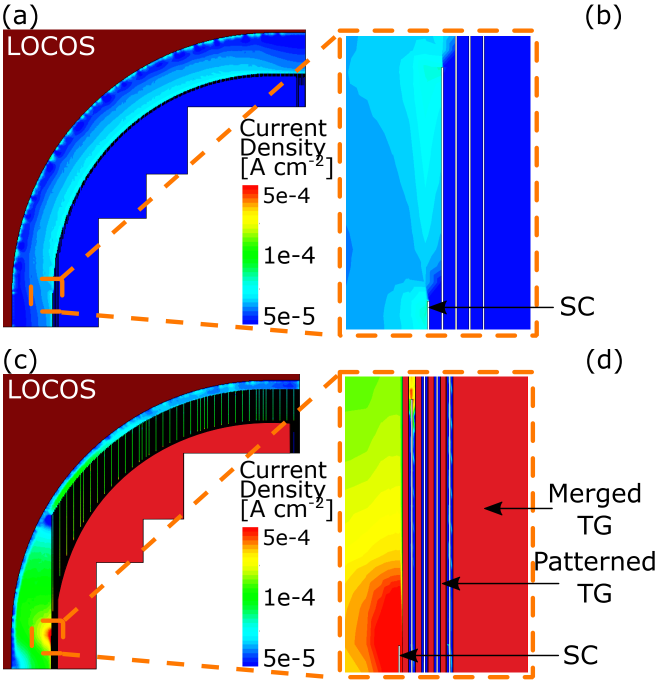

Fig. 7. Avalanche current density at the onset of breakdown when (a) missing and (c) including the TGs in the device structure. (b) and (d) are magnified view of parts (a) and (c) close to the lateral dummy SCs.

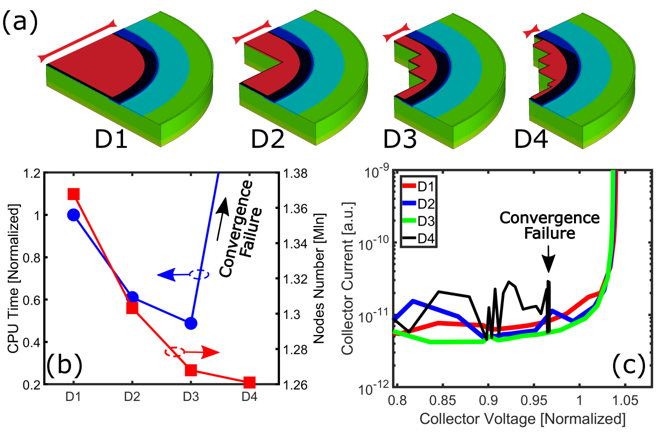

Fig. 8. (a) Different shaping of the simulation domain, resulting in increasing removal of the central part of the device from 1 to 4. (b) CPU time to carry out breakdown simulations and number of mesh nodes for the explored domains. (c) Simulated collector current vs. voltage for the explored domains.

V. Conclusions

We introduced a new approach to perform 3D large-area TCAD simulations of avalanche breakdown at the device edge termination of IGBTs. The approach is based on sensible approximations adopted to build the 3D device structure and allows to fully catch all the aspects of the breakdown phenomenology. By properly reproducing not only the BV but also the percolative current paths in the device, the approach represents a valuable solution to support the development of next-generation IGBT technologies.

Acknowledgments

The authors would like to thank the members of the R&D Power and Discretes group of STMicroelectronics in Agrate Brianza and Catania for support and fruitful discussions.

References

[1] T. Laska, M. Munzer, F. Pfirsch, C. Schaeffer, and T. Schmidt, "The field stop IGBT (FS IGBT). A new power device concept with a great improvement potential," in *12th International Symposium on Power Semiconductor Devices & ICs. Proceedings (Cat. No. 00CH37094)*, pp. 355–358, IEEE, 2000. doi:10.1109/ISPSD.2000.856842.

[2] N. Iwamuro and T. Laska, "IGBT history, state-of-the-art, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 741–752, 2017. doi:10.1109/TED.2017.2654599.

[3] G. Liu, K. Li, Y. Wang, H. Luo, and H. Luo, "Recent advances and trend of HEV/EV-oriented power semiconductors–an overview," *IET Power Electronics*, vol. 13, no. 3, pp. 394–404, 2020. doi:10.1049/iet-pel.2019.0401.

[4] C. Busca, R. Teodorescu, F. Blaabjerg, S. Munk-Nielsen, L. Helle, T. Abeyasekera, and P. Rodríguez, "An overview of the reliability prediction related aspects of high power IGBTs in wind power applications," *Microel. Reliab.*, vol. 51, no. 9-11, pp. 1903–1907, 2011. doi:10.1016/j.microrel.2011.06.053.

[5] M. Shahzad, K. V S Bharath., M. A. Khan, and A. Haque, "Review on reliability of power electronic components in photovoltaic inverters," in *Proc. ICPECA*, pp. 1–6, 2019. doi:10.1109/ICPECA47973.2019.8975585.

[6] M. Arab, S. Lefebvre, Z. Khatir, and S. Bontemps, "Experimental investigations of trench field stop IGBT under repetitive short-circuits operations," in *2008 IEEE Power Electronics Specialists Conference*, pp. 4355–4360, IEEE, 2008. doi:10.1109/PESC.2008.4592645.

[7] Y. Onozawa, D. Ozaki, H. Nakano, T. Yamazaki, and N. Fujishima, "Development of the next generation 1700V trench-gate FS-IGBT," in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, pp. 52–55, IEEE, 2011. doi:10.1109/ISPSD.2011.5890788.

[8] N. Thapar and B. J. Baliga, "Influence of the trench corner design on edge termination of UMOS power devices," *Solid-State Electron.*, vol. 41, no. 12, pp. 1929–1936, 1997. doi:10.1016/S0038-1101(97)00165-2.

[9] X. Tong, S. Liu, W. Sun, and J. Wu, "Complete avalanche process and failure mechanism of trench-gate FS-IGBT under unclamped inductive switching by using infrared visualization method," *IEEE Trans. Electron Devices*, vol. 67, no. 9, pp. 3908–3911, 2020. doi:10.1109/TED.2020.3011644.

[10] P. Mirone, L. Maresca, M. Riccio, G. De Falco, G. Romano, A. Irace, and G. Breglio, "A comprehensive study of current conduction during breakdown of Floating Field Ring terminations at arbitrary current levels," in *Proc. PCIM Europe*, pp. 1–8, 2015.

[11] A. Shimbori and A. Q. Huang, "Design optimization and surge current capability of 4H-SiC lateral deep $p+$ JBS diode on thin RESURF layer," in *Proc. WiPDA*, pp. 17–21, 2022. doi:10.1109/WiPDA56483.2022.9955046.

[12] S. Noblecourt, F. Morancho, K. Isoird, P. Austin, and J. Tasselli, "An improved junction termination design using deep trenches for superjunction power devices," in *Proc. MIXDES*, pp. 547–551, 2015. doi:10.1109/MIXDES.2015.7208583.

[13] J. Lee, J. M. Kim, M. B. Pyun, W. K. Cho, K. Y. Ko, and H. Nah, "3D simulation method to predict breakdown voltage of complex large-scale ring corner in SJ MOSFET," in *Proc. SISPAD*, pp. 257–260, 2023. doi:10.23919/SISPAD57422.2023.10319528.

[14] Synopsys, Mountain View, CA, USA, *Sentaurus Device User Guide V. W-2024.09*, 2024.

[15] J. Zhu, Z. Yang, W. Sun, Y. Du, Y. Sun, Y. Zhu, P. Ye, and Z. Li, "Investigation on the Breakdown Failure in Stripe Trench-Gate Field-Stop Insulated Bipolar Transistor With Low-Saturation Voltage," *IEEE Trans. on Device and Materials Reliability*, vol. 16, no. 3, pp. 384–387, 2016. doi:10.1109/TDMR.2016.2587438.