Advances in Power Electronics Design Fueled by Hyperconvergence

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***Abstract*—Power electronics is at an inflection point, with innovative power transistor design being introduced to serve a variety of applications like fast chargers for consumer devices, EV traction inverters and on-board chargers, LIDAR, data center power supplies, and integrated voltage regulators. We review a recent trend of hyperconvergence of several key design aspects: ab initio material engineering, 3D TCAD analysis of unit cell performance and breakdown, full chip electro-thermal hot spot analysis and layout optimization.**

Keywords—power electronics, power device, design, circuit, DTCO, TCAD, electro-thermal, ab-initio, SiC, GaN

I. Introduction

Power devices consist of a large number of components, such as the active area unit cells, edge terminations and in-chip gate interconnects (Fig. 1). The number of unit cells ranges from thousands to millions for a single full chip power device.

The goal of designing a power device is to simultaneously achieve multiple targets [1, 2]:

- Low on-state resistance to minimize conduction losses
- Breakdown voltage above certain level
- Low off-state leakage
- Short switching delay for low dynamic loss at target frequency
- Reliability and lifetime
- Cost (chip size)
- Fast time-to-market

II. Design of Unit Cells and Termination Devices

Recent advances in meshing techniques, GPU acceleration of numerical algorithms, and physics models for Si, wide bandgap (WBG) and ultra-wide bandgap (UWBG) materials enable 3D TCAD design of unit cells and edge terminations to achieve optimum trade-off in on-state resistance, off-state leakage, breakdown and reliability.

Systematic TCAD-based optimization of edge terminations further enables area (cost) reduction while maintaining required off-state breakdown rating. In particular, 3D TCAD design and verification of corner termination devices lead to multi-day simulations with traditional CPU methodologies which benefit substantially from GPU acceleration, shrinking it from days to hours.

The unit cells tend to fill over 90% of the chip area and define most of the device performance. TCAD has been widely used for fine tuning of the unit cells, usually requiring 3D analysis (Fig. 2).

Edge termination devices are designed mainly to avoid premature breakdown that would happen if all you have is unit cells, just because the last unit cell will have higher electric field due to the geometry at the edge of the cell array.

Edge termination devices tend to have a sophisticated design with field plates, trenches, and super-junctions. TCAD tools have been the workhorse for fine-tuning edge terminations with fast and efficient 2D analysis (Fig. 3).

The corner termination devices have similar requirements to the edge terminations, but are much more challenging, both in terms of the higher electric field in the corners and because of their large size with multiple fine details. This is where GPU acceleration is especially valuable (Fig. 4).

The main task here is to create a corner device that keeps electric field below certain level to avoid premature breakdown (Figs. 5 and 6). TCAD has been heavily used for designing and optimizing the unit cells and the termination devices, but full chip layout design does far beyond such traditional analysis.

III. Optimization of Full Chip Layout

Power transistor design requires co-design of the active area unit cells, edge terminations and in-chip gate interconnects (gate fingers).

Traditionally, power transistor design has been addressed sequentially with multiple trial-and-error iterations. Lack of a full chip design flow results in designs that exhibit failures due to in-chip current and temperature imbalances [3]. These issues become more severe as transistor operational off-state voltage and switching frequency increase.

A hyperconvergence of design tools covering a wide range from ab-initio material engineering to 3D TCAD, electro-thermal analysis, and layout optimization of the power transistor is being introduced to address all these critical design aspects in an automated way.

In the hyperconvergence workflow, the layout is partitioned into tiles representing the components described in Fig. 1 to reduce the number of nodes to a range that can be handled in SPICE. Each tile has a layout view and an associated electro-thermal SPICE model.

The full chip area is filled with scalable tiles, each comprising many unit cells. This tile-based approach enables efficient electro-thermal (ET) circuit simulation of the full chip with sufficient spatial and temporal resolution to detect and correct in-chip current and thermal imbalances.

The workflow is illustrated though its application to a short-circuit (SC) robustness test of a Si 600V class power transistor, whereby the transistor is switched on until the point of failure. Drain current map tends to have hot spots (Fig. 7). This is caused by a combination of factors, including layout of the gate fingers and interconnects as well as self-heating that triggers an avalanche mode.

Fig. 8 shows the electro-thermal failures. For this technology and layouts, device failures are more commonly observed due to temperature rise near the gate fingers and the pad. Although the multi-finger layout achieves more uniform switching, its maximum internal temperature tends to be higher due to the faster current rise.

Such behavior is one of many in-chip behaviors that need to be characterized to balance trade-offs in power device design. The hyper-convergence workflow supports similar analyses for other key robustness tests, such as unclamped inductive switching, as well as hard- and soft-switching operational conditions (Fig, 9).

IV. Ab Initio Analysis

While the well characterized Si power transistors still comprise most of the market, SiC and GaN power transistors are increasingly being adopted in applications where the higher power capability of SiC and faster switching frequency of GaN offers compelling system benefits, while ultra-wide bandgap (UWBG) materials such as Ga_2O_3, AlN and diamond are being explored to offer further system level benefits.

Ab initio analysis is critical in identifying properties of these innovative materials and defects that affect behavior of power devices but is limited in the size and complexity of the systems that can be investigated, due to the computational cost. This limitation can be overcome by leveraging Machine Learning techniques. The ab initio method of Density Functional Theory (DFT) can be used to establish the structure-property relationship for an ensemble of representative atomic structures. This relationship is then used as the basis for training a Machine Learning Force Field (ML-FF) using the Moment Tensor Potential (MTP) formulation [4] as implemented in the Synopsys QuantumATK® software package [5].

This enables calculation of structural properties, such as energy forces and stress (EFS) in a much more efficient manner than DFT, with only a small loss of accuracy. The top half of Fig. 10 shows two simple atomic structures as examples of what could be used in the training of the ML-FF, whereas the bottom half of Fig. 10 shows a much larger and more complicated structure, which would be infeasible to simulate with DFT, but can be handled with the ML-FF approach.

Fig. 11 shows calculation time as a function of aluminum nitride structure size. Not only is there a significant difference in absolute time, but the MTP also shows better scaling with system size, specifically trending towards linear scaling rather than cubic. This means the TAT advantage only grows as the system becomes bigger and more complex. This computational breakthrough enables analysis of realistic structures with interfaces, crystalline, polycrystalline, and amorphous components that cannot be handled with traditional DFT methodology.

V. Evolution of TCAD Tools and Algorithms

Since introduction of first TCAD tools in the 70's [6], the industry has evolved tremendously, pursuing Moore's law for advanced CMOS technology and More-than-Moore philosophy for power electronics. The TCAD tools evolved in lock step with the industry to keep up with the increasingly sophisticated technology.

Evolution of TCAD tools since their introduction encompasses multiple facets (Fig. 12):

- Larger structure and mesh sizes, evolving from ~1k nodes to now exceeding 10M nodes
- Adding new physics models and paradigms to reflect key phenomena in semiconductor devices
- Evolving from single CPU to multi-CPU and now to GPU algorithms
- Evolving from 1D to 2D to 3D, and then to DTCO and STCO, where TCAD tools exhibit hyperconvergence with adjacent domains: lithography, SPICE, layout, electro-thermal, and digital and analog design tools

VI. Conclusions

The innovative hyperconvergence workflow accelerates balancing of multiple trade-offs in power device design, including ab initio material engineering, design of unit cells and termination devices, layout optimization, and full chip electro-thermal analysis. The TCAD tools and algorithms evolve in lock step with the industry demand and expand usage by integrating with adjacent domains.

References

[1] C.-C. Tu et al, "Industry perspective on power electronics for electric vehicles," *Nature Reviews Electrical Engineering*, 1, pp. 435-452 (2024)

[2] K.M.U. Ahmed et al., "A Review of Data Centers Energy Consumption and Reliabiolity Modeling," *IEEE Access*, 9, pp, 152536-152563 (2021)

[3] T. Biondi *et al*., "Effect of layout parasitics on the current distribution of power MOSFETs operated at high switching frequency," *J. Comput Electron.* 5, pp. 149-153 (2006)

[4] A. Shapeev, "Moment Tensor Potentials: a class of systematically improvable interatomic poten-tials," *Multiscale Modeling & Simulation*, vol. 14, no. 3, pp. 1153–1173 (2015)

[5] S. Smidstrup *et al.*, "QuantumATK: an integrated platform of electronic and atomic-scale modelling tools," *J. Phys.: Condens. Matter*, vol. 32, no. 1, p. 015901 (2020)

[6] D. Antoniadis, S. Hansen, and R. Dutton, "SUPREM II: A program for IC process modeling and simulation," Stanford (1978)

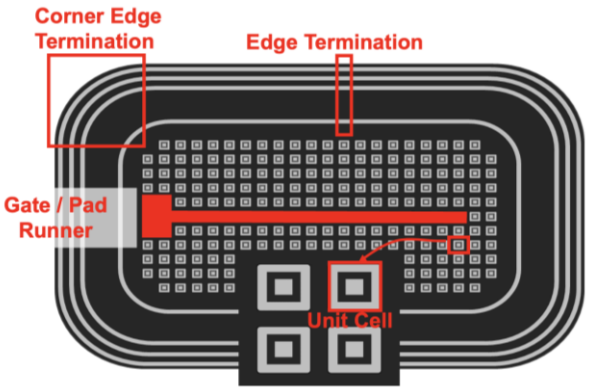

Fig. 1. Layout of a typical power device with unit cells, edge terminations, corner terminations, and gate/pad runners.

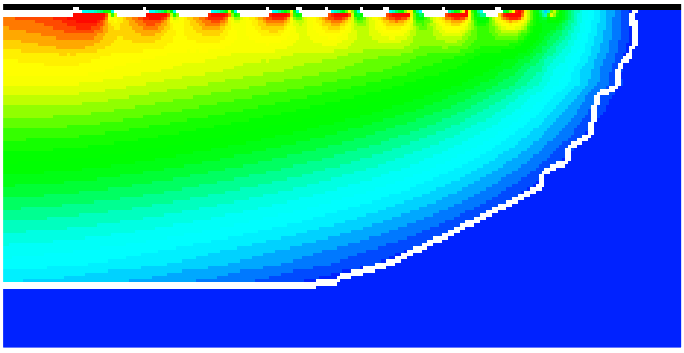

Fig. 3. Cross-section of an edge termination structure with electric field map. Edge terminations protect the chip from premature breakdown and are optimized in TCAD using 2D or quasi-3D simulation.

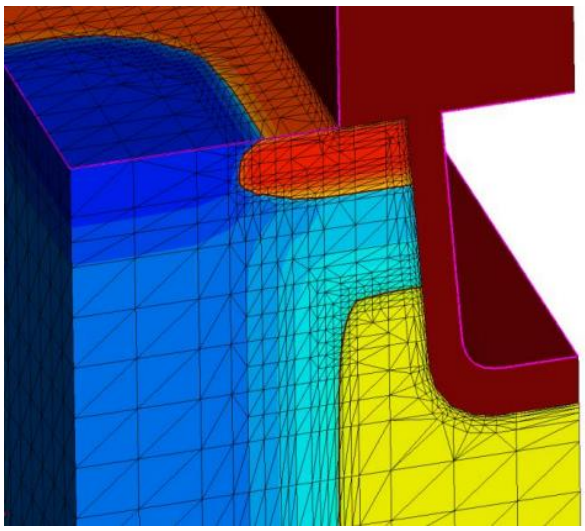

Fig. 2. A 3D view of the unit cell. Power devices tend to have 10^3 to 10^7 unit cells arrayed in striped or cellular (square or hexagonal) layouts.

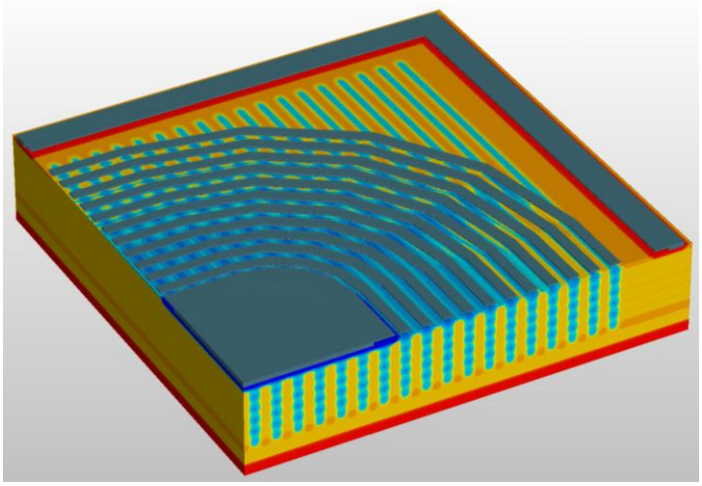

Fig. 4. A 3D view of the corner termination device. Such structures are challenging computationally due to their large size that can span 100's of microns, yet contain a large amount of refined curved junctions which need to be simulated to analyze degradation of the breakdown due to the higher electric field resulting from the junction curvature.

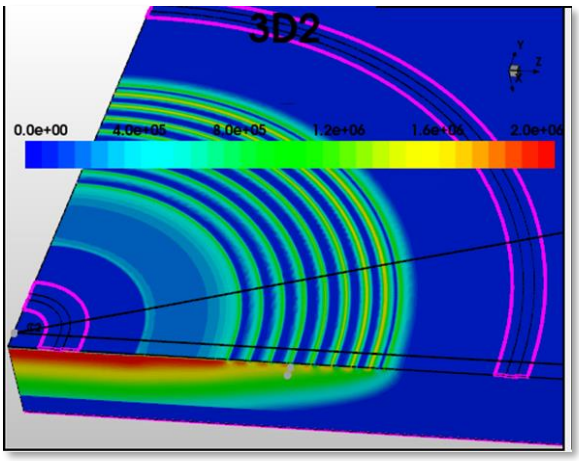

Fig. 5. A 3D view of the corner termination device with electric field map.

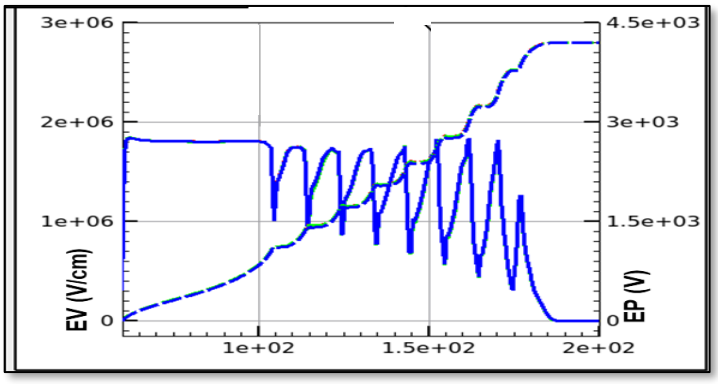

Fig. 6. Electrostatic potential (dashed) and electric field (solid) distributions along the radius of corner termination structure shown on Fig. 5.

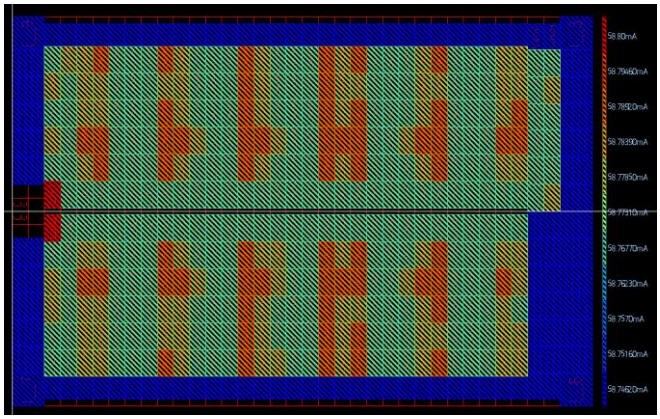

Fig. 7. Full chip drain current map for short-circuit analysis of a 1-gate finger layout configuration with 1.3M cells and 600 V Vdd, with device entering avalanche mode due to self-heating.

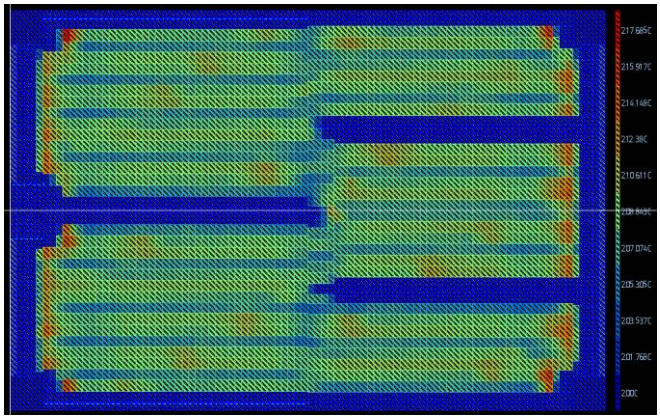

Fig. 8. Full chip temperature map for short-circuit analysis of a 3-gate finger layout configuration with 1.3M cells and 600 V Vdd, with peak T of 218°C.

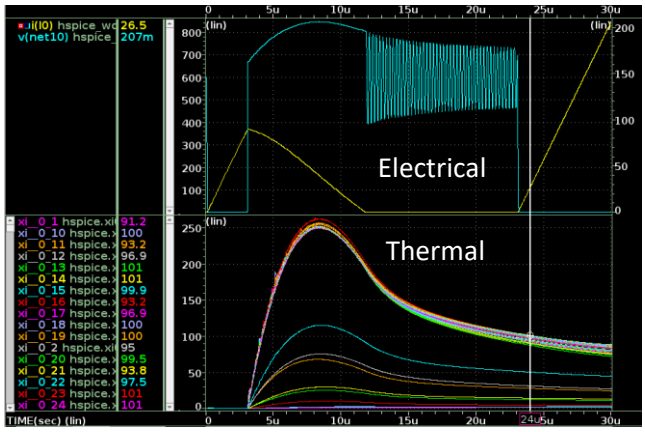

Fig. 9. Self-consistent electrical and thermal behavior analysis of a full chip power device under Unclamped Inductive Switching.

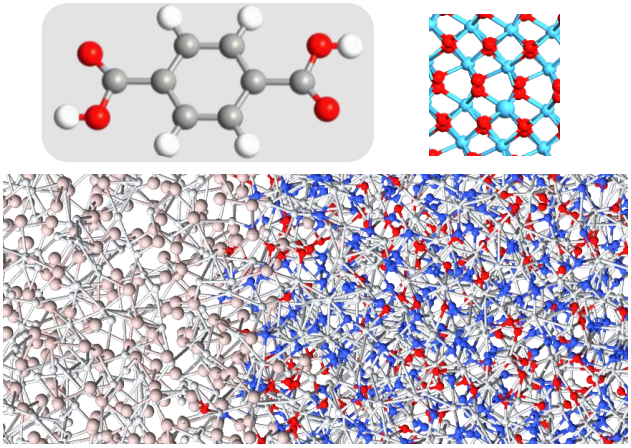

Fig. 10. Density Functional Theory (DFT) analysis of small structures is used to train Moment Tensor-Potential (MTP) formulation for ML-based force fields that enables to expand structure size to thousands of atoms.

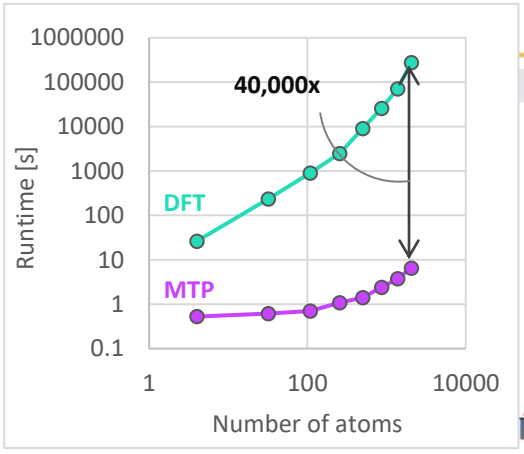

Fig. 11. MTP formulation provides 40,000x speedup for AlN material engineering, enabling analysis of large enough realistic structures with interfaces and crystals, poly-crystals, and amorphous components.

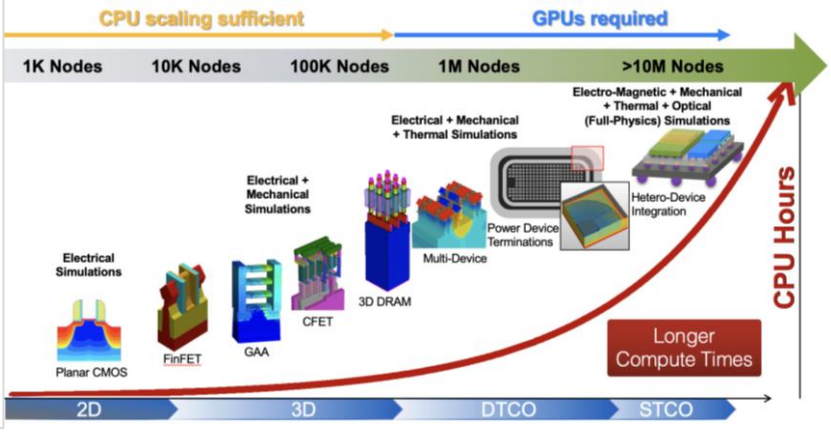

Fig. 12. Evolution of TCAD tools and algorithms in lock step with evolving semiconductor technology.