Data Science Statistical Approach to Percolative Conduction in Poly-Si Based 3D NAND Channels

Aurelio G. Mauri
Micron Technology
Vimercate, Italy
aureliogianc@micron.com

Marco Vezzoli
Micron Technology
Vimercate, Italy
mvezzoli@micron.com

Sebastiano Baggi
Micron Technology
Vimercate, Italy
sbaggi@micron.com

David G. Refaldi
Politecnico di Milano
Milano, Italy
davidgianluigi.refaldi@polimi.it

Alessandro S. Spinelli
Politecnico di Milano
Milano, Italy
alessandro.spinelli@polimi.it

Christian M. Compagnoni
Politecnico di Milano
Milano, Italy
christian.monzio@polimi.it

Luca Chiavarone
Micron Technology
Vimercate, Italy
lchiavar@micron.com

***Abstract*—We present an improved model for the simulation of the string current in 3D NAND Flash cells, able to reproduce experimental data over a temperature range down to 100 K. Statistical results of the model were then explored using Data Science techniques, allowing to understand the dependence of the percolative behavior of the current on grain size and gate bias condition. This information is useful for poly-Si process optimization.**

***Index Terms*—Semiconductor films, Semiconductor device modeling, Polysilicon, Data analysis**

I. Introduction

Accurate modeling of the string current in the poly-Si channel of 3D NAND is essential to evaluate key performance metrics such as sensing margins, cell-to-cell disturbance, quick charge loss, random telegraph noise (RTN), and the scalability of the cell architecture. To this aim, we propose a physics-based statistical model that accurately reproduces the saturation current (I_{sat}) and the neutral cell threshold (V_{T0}) over an extended temperature (T) and grain size range. The model explicitly considers the 3D grain structure and its impact on carrier transport, addressing the inherent poly crystalline nature of the material. Using advanced data science techniques, we also offer a comprehensive analysis of the percolative current paths and their behavior, providing a powerful tool for process analysis and optimization.

II. Polysilicon Mobility Model

To model the impact of polysilicon on carrier transport, we adopt an approach similar to that presented in [1], focusing on mobility degradation rather than variations in the density of states (DOS) induced by grain boundaries ([2], [3]). Within each grain, carriers experience relatively high mobility, while the disruption of lattice continuity at the Grain Boundaries (GBs) leads to significant carrier scattering, even in the absence of charged defects. The mobility within each polysilicon grain can then be calculated from

$$\mu_{G-B} = \mu_{GB_{Tref}} \cdot \left(\frac{T}{T_{ref}}\right)^{-\alpha} \tag{1}$$

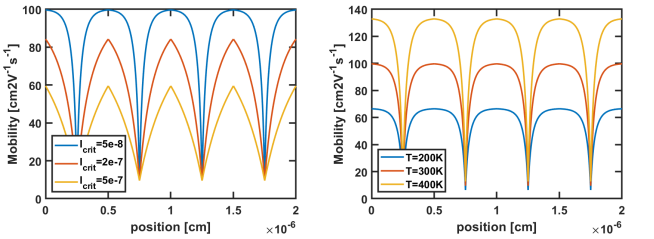

Fig. 1: Electron mobility model dependence on l_{crit} (left) and T (right).

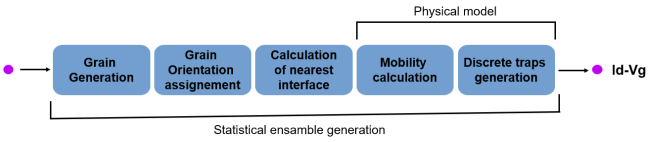

Fig. 2: Simulation flow chart that combines physical and statistical aspects of polysilicon modeling approach.

$$\mu_{GB_{Tref}} = \mu_{G-0} + (\mu_{\text{int}} - \mu_{G-0})\, e^{-\frac{d_{\text{int}}}{l_{\text{crit}}}} \tag{2}$$

where μ_{G-0} and μ_{int} are the bulk and interface mobilities, d_{int} is the distance of the carrier position from the GB interface, and l_{crit} is a parameter accounting for the extent of interface scattering within the grains. Fig. 1 illustrates the key dependences: increasing l_{crit} leads to a reduction in intra-grain mobility (left), as does a temperature reduction, differently to what observed in monocrystalline silicon.

III. Simulation and Numerical Details

The used simulation flow is shown in Fig. 2: The process begins with the generation of grains using Laguerre tessellation [4] subsequently meshed and incorporated into the simulation domain. Fig. 3 presents the resulting grain volume distributions for two representative cases: large (red) and small (yellow) grains. By calibrating the average grain size

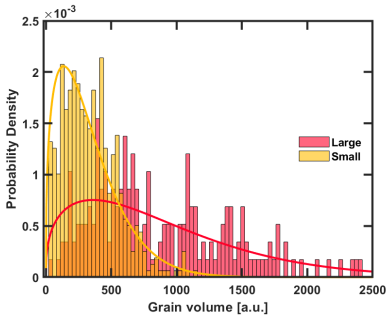

Fig. 3: Grain size volume distribution extracted for two different average grain sizes (large and small).

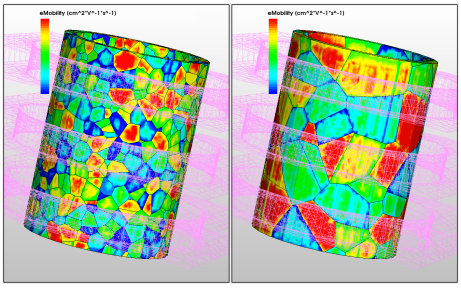

Fig. 4: Electron mobility in the channel for small (left) and large (right) grain size at $T = 300$ K.

and its dispersion using TEM data, the simulation framework can explicitly capture the geometrical effects of the poly-Si channel, enhancing the physical accuracy of the model.

Next, mobilities are calculated accounting for a random assignment of crystal orientations to each grain. Fig. 4 illustrates the spatial distribution of electron mobility within the simulation domain for two different grain size scenarios. As expected from (2), smaller grain size results in significantly reduced mobility, highlighting the critical role of grain structure in carrier transport. The final step of the modeling process involves the explicit incorporation of localized defects at GBs, shown in Fig. 5 for large and small grain size, highlighting the increased defect density associated with smaller grain sizes, which significantly affects carrier transport and device variability.

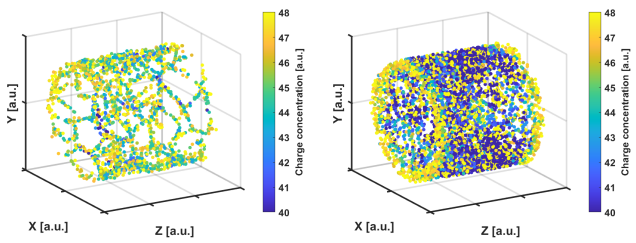

Fig. 5: Grain boundary trap concentration in poly-Si channel for large (left) and small (right) grain size.

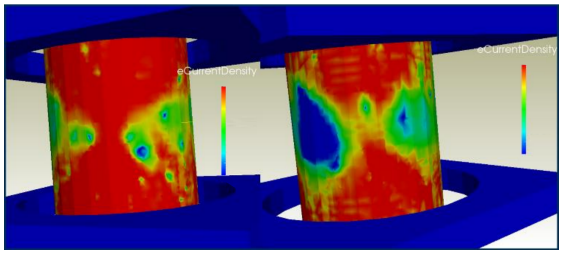

Fig. 6: Example of current density in the 3D NAND channel for small (left) and large (right) grain dimensions at $T = 300$ K.

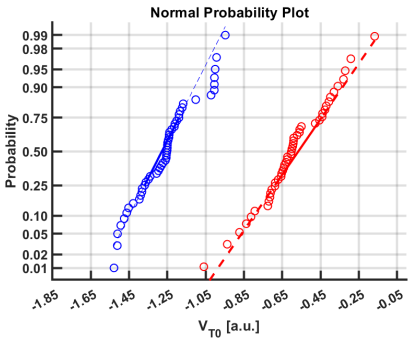

Fig. 7: V_{T0} normal plot for small (blue) and large grain size (red).

The interplay between mobility degradation at GBs and localized charged defects significantly alters the nature of current paths, particularly in the subthreshold regime. A representative example is shown in Fig. 6, where the current flow exhibits a distinct percolation behavior, strongly influenced by such phenomena. Due to the complexity of this modeling approach, achieving convergence of the Drift-Diffusion system often requires a very fine mesh, especially at very low temperatures.

IV. Comparison with Data

To analyze the statistical behavior of the system, a large set of simulation samples was generated by varying grain sizes, shapes, and spatial distribution of defects. Fig. 7 presents the normal probability plot of V_{T0} for two different grain size distributions, revealing not only that the average value of V_{T0} shift with grain size, but also that the distribution broadens significantly for larger grains, indicating increased variability. Fig. 8 shows the comparison between simulations and experimental data for V_{T0} and I_{sat} as a function of the grain size, assuming constant surface defect density: Increasing grain size, V_{T0} reduces because the number of defects per unit volume is lower with larger grains. At the same time, I_{sat} improves because mobility is less degraded by the large grain dimension. In any case, a good matching is achieved. Similar results, but as a function of the polysilicon thickness, are reported in Fig. 9.

Fig. 10 further demonstrates that our simulation approach accurately reproduces experimental data down to 110 K. This agreement is achieved through the temperature-dependent

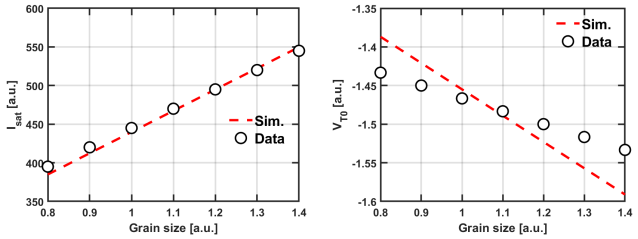

Fig. 8: Comparison between experimental data and simulation results for I_{sat} (left) and V_{T0} (right) as functions of the polysilicon grain size at $T = 300$ K.

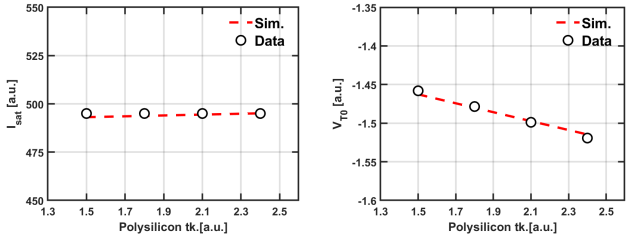

Fig. 9: Same as Fig. 8, but as a functions of the polysilicon thickness.

mobility model described in equation (1), with the best fit obtained for an exponent $\alpha = 1$. Physically, the observed inverse temperature dependence of I_{sat} is attributed to increased trap occupation at lower temperatures, which significantly impacts carrier transport in polycrystalline materials.

V. Data Science Analysis of Percolation Paths

As shown in Fig. 6, current flow in the poly-Si channel exhibits a strongly percolative nature in the subthreshold regime. Understanding how this behavior depends on physical and electrical parameters can be useful in optimizing the polysilicon deposition process, not only to improve I_{sat}, but also to mitigate variability-related phenomena such as RTN. To investigate this, we analyzed conduction by distinguishing between current density flowing along the outer channel surface (J_O, facing the gates) and along the inner surface (J_I, adjacent to the filler dielectric), and defining an average deviation from the mean current, $J_{tk}(V)$, which explicitly depends on gate bias V and polysilicon thickness tk, as:

$$J_{tk}(V) = \frac{\overline{J_I} - \overline{J_O}}{\overline{J}}, \tag{3}$$

where $\overline{J}$ is the mean of the current density of the two surfaces. Note that positive values correspond to current predominantly flowing along the internal channel surface.

Fig. 11 shows the behavior of $J_{tk}(V)$ as a function of gate bias V for various polysilicon thicknesses. Note that the dominant conduction path changes from internal to external surfaces at high gate bias, consistently across all simulated conditions, indicating that this behavior is an intrinsic feature

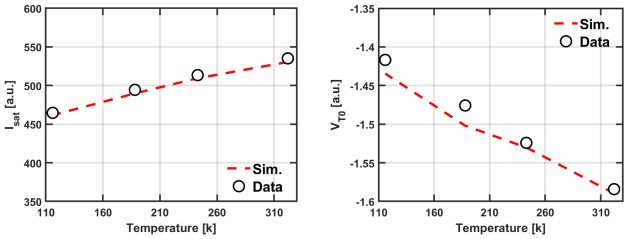

Fig. 10: Same as Fig. 8, but as a function of temperature.

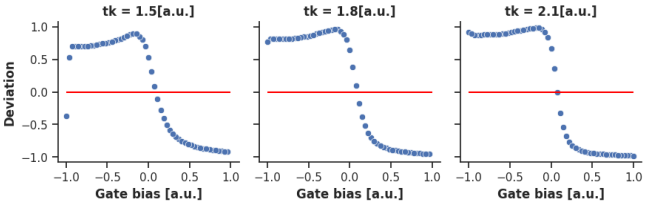

Fig. 11: Typical J_{tk} dependence on gate bias for different poly-Si thickness.

of the hollow-channel architecture. A closer examination of Fig. 11 reveals that the gate bias at which this change occurs slightly increases as the polysilicon thickness decreases. To further investigate the spatial dynamics of this behavior, we turn to a cylindrical coordinate system, with the z axis aligned with the cylindrical symmetry axis of the hollow channel. By evaluating the modulus of the current density within each grain of the polysilicon channel and plotting it against the angular coordinate θ, it becomes possible to track the evolution of current flow as a function of V, for each cell. An example is shown in Fig. 12, where the polar plots reveal how the spatial distribution of current depends on V.

Each percolation path is identified by distinct current density peaks on both the inner (blue) and outer (orange) channel interfaces, as shown after the switching event. Notably, these peaks often occur at the same angular positions on both surfaces, with the inner interface typically contributing more significantly to the total current at low gate bias. As V increases, a switching phenomenon is observed: the dominant current path changes from the inner to the outer interface, while retaining its percolative nature. Only at sufficiently high gate biases the current distribution becomes more uniform, resembling conduction in a standard mono-crystalline material.

To determine whether this behavior is intrinsic to poly-Si channel conduction, we apply data science techniques. Specifically, the current density distributions (*e.g.*, those in Fig. 12) are regressed using Chebyshev polynomials [5] to automatically identify local maxima. Each peak is characterized by its mean angular position, μ_{J_i}, where the index i denotes the i-th percolation path along the θ axis. By tracking μ_{J_i} as a function of gate bias, we can analyze the persistence and evolution of percolation paths in both count and position. To quantify the transition from percolative to uniform conduction,

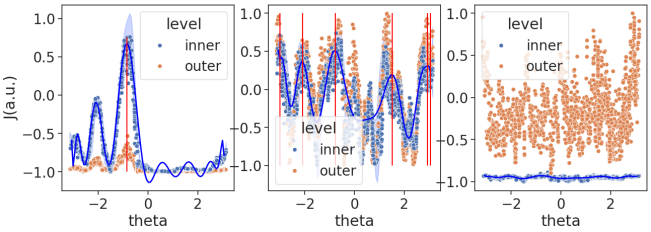

Fig. 12: Distribution plot of the switching dynamics: before (left), during (center), and after switch (right) at $T = 300$ K.

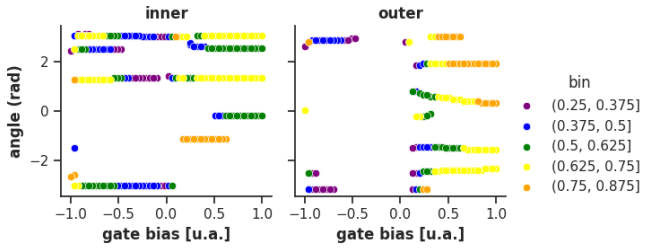

Fig. 13: Analysis of current percolation as a function of V. Colors indicate the relative χ peak value of each percolation path compared to the highest one.

we introduce a statistical index χ, inspired by the Snedecor F-statistic [6]. The current density distribution along the θ axis is discretized into n bins. For each bin, we compute the average current $\mu_i[J_{I,O}]$ and its standard deviation $\sigma_i[J_{I,O}]$, separately for the inner and outer interfaces. The index χ is then defined as the ratio between the average of the current dispersions and the dispersion of the current averages:

$$\chi = \frac{\mu[\sigma[J_{I,O}]]}{\sigma[\mu[J_{I,O}]]}. \tag{4}$$

This metric serves as a robust indicator of percolative behavior: high χ values correspond to localized, peak-dominated conduction, while low values indicate a more uniform current flow. Fig. 13 illustrates a representative case from the simulation ensemble: At the inner channel interface, the current density remains highly localized, confined to a limited number of percolation paths. As the gate bias increases, switching to the outer interface becomes clearly detectable through the previously described procedures. This transition is also accompanied by a noticeable increase in the number of identified percolation peaks, indicating a broader spatial distribution of current flow along the outer surface.

Extending this analysisacross the entire simulation ensemble, we demonstrate that the polysilicon channel consistently exhibits a limited number of stable percolation paths prior to the onset of the switching mechanism. As the gate overdrive increases, a transition from percolative to non-percolative behavior is observed universally across all cases. This transition marks the point at which current flow becomes more uniform and less localized.

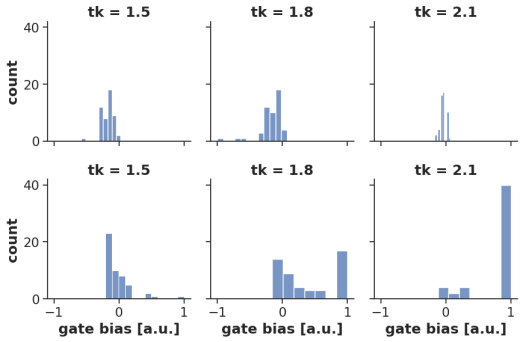

Fig. 14: Distribution of the gate voltages which discriminate percolative and uniform current flow as a function of polysilicon thickness. First row outer interfaces second row inner interface.

A systematic investigation of this phenomenon is presented in Fig. 14, which reports the gate bias at which the percolation-to-uniform transition occurs as a function of polysilicon thickness, for both inner and outer channel interfaces. Focusing on the outer interface (top row of Fig. 14), we observe that increasing the polysilicon thickness results in a tighter distribution of the switching gate bias. This indicates a more consistent and predictable onset of the transition from percolative to uniform conduction as the channel becomes thicker.

VI. Conclusions

We developed a numerical model for transport in the polysilicon that accurately reproduces experimental data over a T range down to 110 K. Via data science methods, we have thoroughly characterized the percolative nature of polysilicon conduction, revealing the bias-driven switching behavior from the inner to the outer Si/iO_2 interface. These findings can provide insights for optimizing the poly-Si process.

Acknowledgments

The authors are grateful to the Micron Advanced NAND Team for experimental support and technical assistance.

References

[1] R. Degraeve et al., "Statistical poly-Si grain boundary model with discrete charging defects and its 2D and 3D implementation for vertical 3D NAND channels," 2015 IEEE IEDM, pp.5.6.1-5.6.4.
[2] M. D. Jacunski et al., "A short-channel DC SPICE model for polysilicon thin-film transistors including temperature effects," IEEE TED, vol. 46, no. 6, pp. 1146-1158, 1999.
[3] D. Resnati et al. "Temperature Effects in NAND Flash Memories: A Comparison Between 2-D and 3-D Arrays," IEEE EDL, vol. 38, no. 4, pp. 461-464, 2017.
[4] R Quey and M Kasemer, "The Neper/FEPX project: free / open-source polycrystal generation, deformation simulation, and post-processing", IOP Materials Science and Engineering, vol. 1249, pp. 012021, 2022.
[5] T. J. Rivlin, "Chebyshev polynomials". Wiley Interscience, 1974.
[6] J., N. Lloyd, S. Kotz and N. Balakrishnan "Continuous Univariate Distributions" , Vol. 2, Sect. 27 (2nd ed.). Wiley. ISBN 0-471-58494-0, 1995.