Airgap-induced Field Enhancement to Improve Memory Operation in 3-D NAND Flash Memory

1st Devin Verreck
imec
Leuven, Belgium
devin.verreck@imec.be

2nd Sana Rachidi
imec
Leuven, Belgium

3rd Geert Van den bosch
imec
Leuven, Belgium

4th Maarten Rosmeulen
imec
Leuven, Belgium

***Abstract*—Airgaps have been proposed to mitigate inter-wordline interference in vertically scaled 3-D NAND flash memories. Here, we show with calibrated simulations that specific airgap configurations also improve the memory operation by increasing the electric field around carrier injection points. We investigate both cylindrical gate-all-around and vertical trench cell architectures. For gate-all-around cells, we find a significant reduction of the programming voltage and improvement in erase onset when the airgaps extend into the tunnel oxide. For trench cells, we propose an inter-channel airgap configuration that strongly improves the programming operation, making it competitive with the gate-all-around architecture.**

***Index Terms*—3-D NAND, flash memory, GAA, trench, airgap**

I. Introduction

The bit density of 3-D NAND flash memories has increased relentlessly over the last decade. This growth has largely been driven by the addition of memory cells to the string, while maintaining a rather relaxed cell pitch [1], [2]. As the aspect ratio of the string grows, however, the anisotropic etch of the cylindrical memory hole becomes progressively more challenging. Consequently, vertical cell pitch scaling has become necessary to limit the total string length [2]. Unfortunately, scaling gate length (L_{G}) or inter-gate spacing (L_{IGS}) of the cells degrades the memory operation and worsens interference between neighboring gates. This necessitates higher programming voltages and results in less effective erase. These issues are exacerbated in new proposed architectures designed to further enhance bit density such as the 3-D trench cell [3]. Such vertical planar cells do not have a gate-all-around (GAA) configuration and therefore do not benefit from a curved geometry, resulting in degraded memory operation.

Inter-cell airgaps have been proposed as a scaling enabler and have recently experimentally been shown to reduce capacitive coupling and lateral migration between wordline gates [4]. However, this coupling reduction typically comes at the expense of degraded memory operation. This is most pronounced for the incremental step pulse erase (ISPE) operation, where the erase onset shifts to more negative voltages. Although the degradation during the incremental step pulse programming (ISPP) operation is less severe, it still results in a reduced programming slope.

Here, we show using calibrated simulations that specific airgap configurations not only reduce cell-to-cell coupling, but also significantly improve the memory operation by enhancing the electric field around carrier injection points. We use our in-house developed modeling framework to demonstrate this effect both in GAA and trench cell architectures. For the trench cell specifically, we leverage the inter-channel spacing (ICS) to propose an airgap configuration that significantly reduces programming voltages.

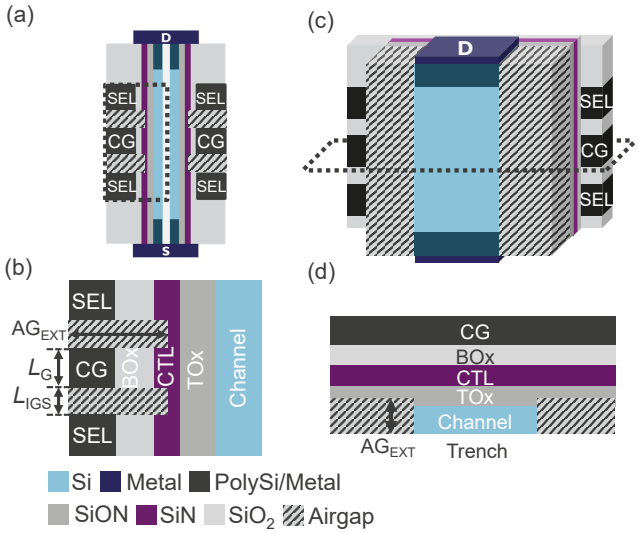

Fig. 1. Simulated 3-D NAND flash structures. (a) Cylindrically symmetric GAA string with dotted box enlarged in (b). (c) 3-D trench cell with dotted cutplane through CG enlarged in (d). An example airgap configuration is shown with a dashed box for both architectures.

II. Simulation Details

Our simulations are based on a memory operation model that was jointly developed with Global TCAD Solutions (GTS) and implemented in the GTS Minimos tool [6]–[8]. During the memory operation, carriers can tunnel through the tunnel oxide (TOx) or blocking oxide (BOx) and are then distributed over the charge trap layer (CTL) based on a Gaussian shape function that represents their energy dissipation. The tunneling probabilities are calculated with the Wentzel-Kramers-Brillouin approach. Carriers are (de-)trapped in traps spread uniformly throughout the CTL due to Shockley-Read-Hall (SRH) processes. During the read operation, the threshold

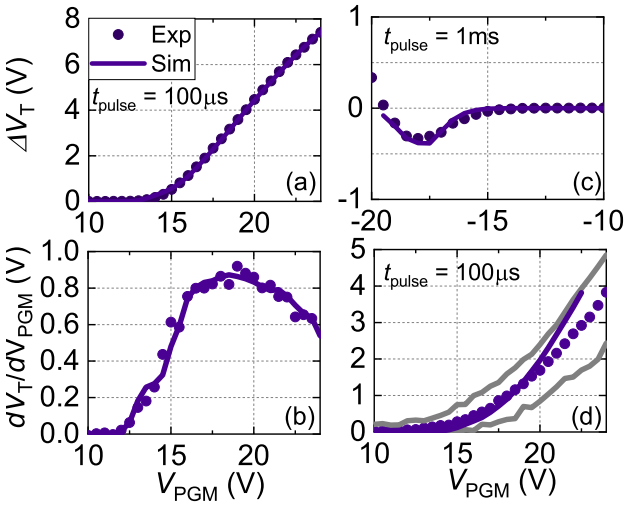

Fig. 2. Calibration to experiment for three-gate test vehicles [3] [5]. (a) GAA ISPP curve and (b) ISPP slope. (c) GAA ISPE from fresh. (d) Trench cell ISPP with grey lines for 5-95% data spread. The structures are shown in Fig. 1 with for the GAA, a memhole diameter of 120 nm, L_G of 50 nm, L_{IGS} of 30 nm and polySi gates with 5e19 cm^{-3} acceptor doping. BOx/CTL/TOx/channel thicknesses are 6/6/6/10 nm. For the trench cell, L_G is 30 nm, L_{IGS} is 20 nm, W_{ch} is 50 nm and a 2 nm high-k layer is present between the gates and the BOx. V_{SEL} is $\pm$ 7 V, V_{DS} is 0.1V. For both configurations, calibrated trap density in the CTL is 4.5e19 cm^{-3} with a capture cross section of 1e-16 cm^2. The channel-TOx conduction band offset is 3.12 eV, for gate-BOx it is 4.03 eV, and the channel-TOx valence band offset is 3.5 eV. Mobility in the CTL is 0.07 cm^2/Vs for electrons and 0.01 cm^2/Vs for holes. Effective masses in the TOx and BOx are 0.45 m_0 for electrons and 0.6 m_0 for holes.

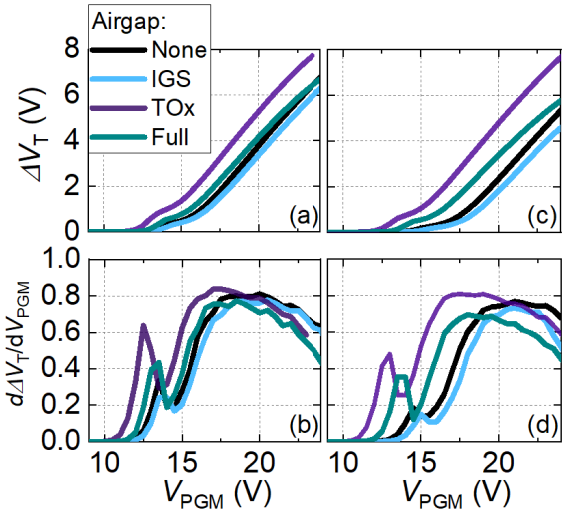

Fig. 3. Impact of airgap configuration on ISPP curves and slopes of a GAA 3-D NAND flash string as in Fig. 1(a-b). For IGS airgaps, AG_{EXT} is 4 nm only in the IGS, for TOx airgaps AG_{EXT} is 6 nm only in the TOx, for full airgaps, AG_{EXT} is 22 nm through entire memory stack. V_{DS} is 0.1 V and V_{SEL} is 7 V. Memhole diameter is 120 nm, BOx/CTL/TOx/channel thicknesses are 6/6/6/10 nm. (a-b) L_G=L_{IGS}=30 nm, (c-d) L_G=L_{IGS}=15 nm.

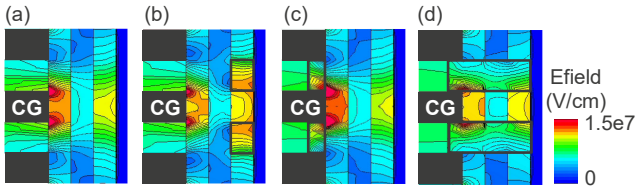

Fig. 4. Impact of airgaps on electric field magnitude during ISPP operation for the same configurations as in Fig 3. V_{PGM} is 18 V. L_G=L_{IGS}=15 nm. (a) No airgaps, (b) TOx airgaps, (c) IGS airgaps, (d) full airgaps.

voltage shift of a cell relative to the fresh state (ΔV_{TH}) is calculated with a standard combination of Poisson's equation and a drift-diffusion model in the channel.

The simulated structures replicate our experimental three-gate vehicles for the GAA and the trench cell (see Fig. 1) [5], and a comparison of simulated memory operation curves with experimental data is shown in Fig. 2. The simulated GAA curves show a close calibration to experiment for both ISPP and ISPE from fresh, with the calibrated parameters indicated in the caption. For the same parameters, the ISPP simulation of the trench cell deviates more from the median experiment, but still falls within the large variability margins. A more detailed discussion on the model validation can be found in our previous publications [6], [7].

In the rest of this work, we assume the same memory stack between the GAA and trench cells (as shown in Fig. 1) and replace the polySi gates with metal to avoid depletion effects from convoluting the analysis of the memory operation in scaled cells. For the GAA cell, the structure is assumed to be cylindrically symmetrical to reduce computational burden. For the trench cell, a full 3-D simulation is carried out.

III. Airgap Impact on GAA Memory Operation

Fig. 3 shows that airgaps in the TOx can significantly reduce the programming voltage and improve the ISPP slope compared to the case without airgap, or with airgaps only in the IGS. This effect is stronger for more scaled cell dimensions (compare Fig. 3(a-b) to (c-d)). Extending the airgaps through the full memory stack shows an improvement over the no-airgap case, but it is smaller than for the TOx-only airgaps, and is accompanied by a degradation in the program saturation.

Fig. 4 explains these trends based on the impact of the airgaps on the electrostatics in the memory stack. Airgaps in the TOx increase the electric field between them, thereby exponentially enhancing the carrier tunneling probability into the CTL and hence the injection current at a given programming voltage (Fig. 4(b)). This enhancement is more pronounced closer to the airgap-TOx interfaces, so the impact on a scaled cell is larger. IGS-only airgaps, on the other hand, have negligeable effect on the ISPP behavior of the cell, as they show similar electric field to the no-airgap case near the TOx-channel interface (Fig. 4(c)). Extending the airgaps through the full stack enhances the TOx electric field, but less than the TOx-only airgaps, as fringing field lines from the gate are cut off (Fig. 4(d)). The reduction in available CTL volume explains the degradation in program saturation.

For ISPE from fresh, Fig. 5 shows that IGS airgaps result in a degradation, while TOx and full airgaps have a beneficial

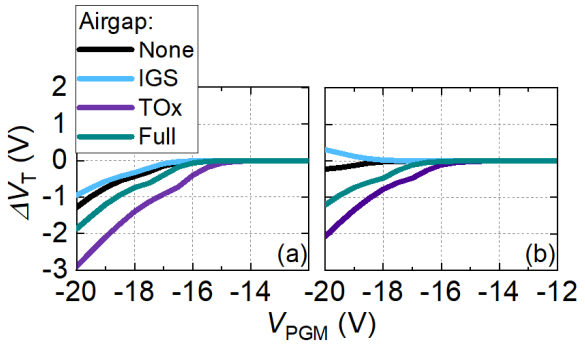

Fig. 5. Impact of airgap configuration on ISPE from fresh curves of a GAA 3-D NAND flash string as in Fig. 1(a-b). For IGS airgaps, AG_{EXT} is 4 nm only in the IGS, for TOx airgaps AG_{EXT} is 6 nm only in the TOx, for full airgaps, AG_{EXT} is 22 nm through entire memory stack. V_{DS} is 0.1 V and V_{SEL} is -7 V. Memhole diameter is 120 nm, BOx/CTL/TOx/channel thicknesses are 6/6/6/10 nm. (a) L_G=L_{IGS}=30 nm, (b) L_G=L_{IGS}=15 nm.

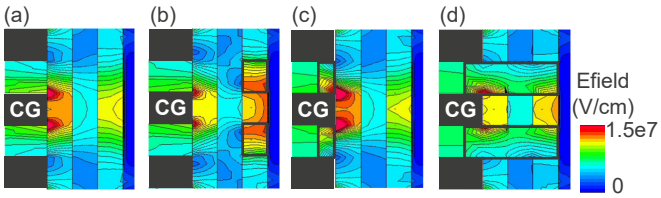

Fig. 6. Impact of airgaps on electric field magnitude in GAA string during ISPE from fresh operation for the same configurations as in Fig. 5. V_{PGM} is -18 V. L_G=L_{IGS}=15 nm. (a) No airgaps, (b) TOx airgaps, (c) IGS airgaps, (d) full airgaps.

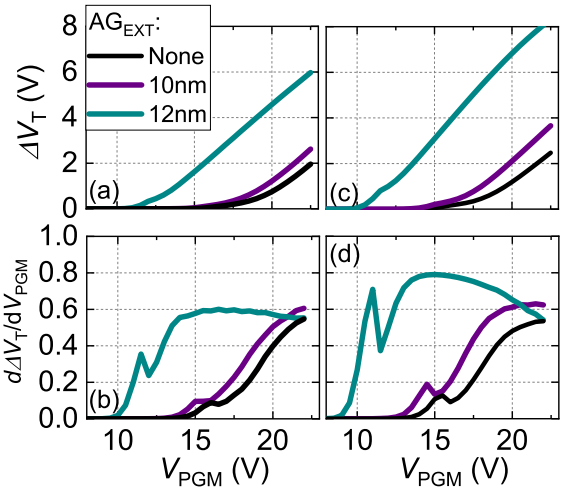

Fig. 7. Impact of airgaps in the inter-channel spacing with varying extension on ISPP curves and slopes of a 3-D trench cell as in Fig. 1(c-d). BOx/CTL/TOx/channel thicknesses are 6/6/6/10 nm. V_{DS} is 0.1 V and V_{SEL} is 7 V. L_G=L_{IGS}=15 nm. (a-b) W_{ch}=30 nm, (c-d) W_{ch}=10 nm.

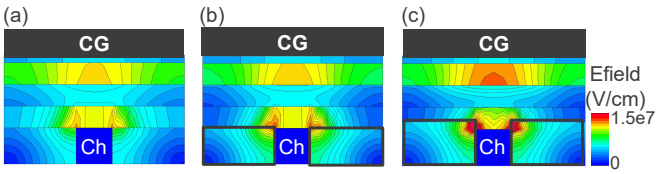

Fig. 8. Impact of airgaps in the inter-channel spacing on electric field magnitude of a 3-D trench cell for the same configurations as in Fig. 7. V_{PGM} is 18 V. L_G=L_{IGS}=15 nm. (a) No airgap, (b) AG_{EXT}=10 nm, (c) AG_{EXT}=12 nm.

effect on the erase onset. Fig. 6(a-b) shows that similar to the ISPP case, TOx airgaps increase the electric field close to the hole injection points, which explains the lower erase onset voltage. Fig. 6(c) shows, moreover, that IGS airgaps increases the unwanted electron injection from the gate, explaining the erase degradation in the corresponding ISPE curve. This differs from the ISPP, where the IGS airgaps have a negligeable effect on the ISPP curve, as hole injection from the gate is minimal due to the large valence band offset with the BOx. Finally, Fig. 6(d) shows that full airgaps increase both the electric field at the hole injection point and the electron injection point, resulting in an ISPE curve that lies between the TOx airgap and no-airgap case.

From these simulations, we can therefore conclude that to improve the memory operation, the airgaps should have some component in the TOx, with the optimal configuration an airgap that is only present in the TOx, close to the TOx-channel interface. Such airgaps are challenging to realize in practice, however, as they would have to be fabricated from the memory hole side. Full airgaps that extend through the entire stack would be easier to realize, but would reduce the ISPP and ISPE improvement.

IV. Inter-channel airgap for trench cell

The trench cell architecture offers the possibility to place airgaps directly next to the channel in the ICS, which does not exist in a GAA structure with cylindrical channel. Moreover, the ICS is readily accessible from the trench side after the channel patterning. This would allow to place airgaps close to the TOx-channel interface without the need to cut through the entire memory stack.

Fig. 7 shows that ICS airgaps can strongly reduce the programming voltage and improve the ISPP slope, especially when they extend into the TOx. If the top edge of the airgaps is aligned with the TOx-channel interface (AG_{EXT} = 10 nm), there is a noticeable improvement in the ISPP slope. If the airgaps extend slightly into the TOx (AG_{EXT} = 12 nm), the impact is even larger, with e.g. the V_{PGM} required to reach a ΔV_{th} of 4 V reduced with almost 5 V. We have verified that this effect remains for finer mesh size and is not an artifact of tunnel path placement (not shown). For a more narrow W_{ch} of 10 nm (see Fig. 7(c-d)), the airgap impact is even slightly larger, with a stronger improvement of the ISPP slope.

The electric field plots in Fig. 8 show that the ISPP improvement for the ICS airgaps has a similar origin as in the GAA cell: an increase of electric field around the carrier injection points. Previous research has shown that the dominant injection occurs around the channel corners because of the locally enhanced electric field [3]. It is also around these corners that the ICS airgaps enhance the electric field, which

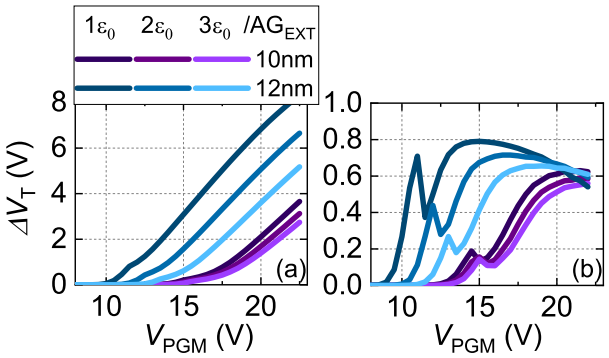

Fig. 9. Impact of permittivity of inter-channel spacer on ISPP curves and slopes of a 3-D trench cell for the same configurations as in Fig. 7. V_{DS} is 0.1 V and V_{SEL} is 7 V. L_G=L_{IGS}=15 nm. W_{ch}=10 nm.

means the majority of the injected carriers experience a strong field enhancement. This explains why the impact of the airgaps is significantly larger than in the GAA case, where the carriers are injected more uniformly along the TOx-channel interface. Scaling the channel width brings the channel corners closer together, amplifying the effect.

A further confirmation that the ISPP improvement has its origin in the electrostatics comes from Fig. 9, which shows that increasing the permittivity of the spacer reduces the improvement. This also indicates that low-k materials could be an alternative to airgaps to achieve ISPP improvement.

Finally, Fig. 10 shows an example process flow for inter-channel airgaps and emulated 3-D structures for illustration. The flow proceeds as a conventional 3-D trench cell flow up until the memory stack deposition and channel patterning (Fig. 10(a)) [3]. Next, the inter-channel spacing is filled up with a sacrificial material (Fig. 10(b)) and covered with an oxide liner. During subsequent thermal treatment, the sacrificial material decomposes and diffuses through the oxide liner, leaving behind airgaps between the channels (Fig. 10(c)).

V. Conclusions

We demonstrated through calibrated simulations that airgaps can improve the memory operation of 3-D NAND flash cells by enhancing the electric field around the carrier injection points. For the GAA configuration, introducing inter-gate airgaps that cut through the tunnel oxide significantly reduces the required programming voltage and erase onset. In the 3-D trench cell configuration, we proposed inter-channel airgaps and showed a substantial improvement of programming behavior, particularly when the airgaps extend into the tunnel oxide. This airgap concept highlights a potential pathway for high-bit-density trench cells to rival GAA configurations in memory performance. Our simulations assume sharp airgap corners and therefore show their maximal impact. Future work can explore airgap shapes that more closely replicate those obtained in experimental implementations.

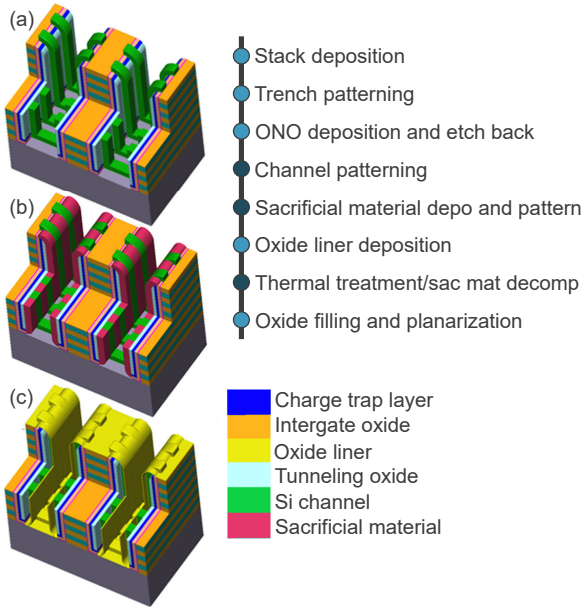

Fig. 10. Proposed process flow for inter-channel airgaps in 3-D trench cell architecture and 3-D emulated structures after selected process steps (indicated by dark nodes in flow).

Acknowledgment

This work was supported by imec's Industrial Affiliation Program for storage devices.

References

[1] J. Alsmeier, M. Higashitani, S. S. Paak, and S. Sivaram, "Past and Future of 3D Flash," in *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2020, pp. 6–1.

[2] A. Goda, "3-D NAND Technology Achievements and Future Scaling Perspectives," *IEEE Transactions on Electron Devices*, vol. 67, no. 4, pp. 1373–1381, 2020.

[3] S. Rachidi, S. Ramesh, L. Breuil, Z. Tao, D. Verreck, G. L. Donadio, A. Arreghini, G. V. D. Bosch, and M. Rosmeulen, "Enabling 3D NAND Trench Cells for Scaled Flash Memories," in *2023 IEEE International Memory Workshop (IMW)*, 2023, pp. 1–4.

[4] D. Resnati, G. Carnevale, S. Surthi, C. M. Carlson, M. Thorum, T. Kim, E. Camerlenghi, and R. Hill, "A Confined Storage Nitride 3D-NAND Cell with WL Airgap for Cell-To-Cell Interference Reduction and Improved Program Performances," in *2024 IEEE Symposium on VLSI Technology and Circuits*, 2024, pp. 1–2.

[5] A. Arreghini, K. Banerjee, D. Verreck, S. V. Palayam, E. Rosseel, L. Nyns, G. Van den bosch, and A. Furnémont, "Improvement of conduction in 3-D NAND memory devices by channel and junction optimization," in *2019 IEEE 11th International Memory Workshop (IMW)*, May 2019, pp. 1–4.

[6] F. Schanovsky, D. Verreck, Z. Stanojević, S. Schallert, A. Arreghini, G. van den Bosch, M. Rosmeulen, and M. Karner, "Modeling the Operation of Charge Trap Flash Memory–Part I: The Importance of Carrier Energy Relaxation," *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 547–553, 2024.

[7] D. Verreck, F. Schanovsky, A. Arreghini, G. Van den Bosch, Z. Stanojević, M. Karner, and M. Rosmeulen, "Modeling the Operation of Charge Trap Flash Memory—Part II: Understanding the ISPP Curve With a Semianalytical Model," *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 554–559, 2024.

[8] Global TCAD Solutions Rel.2022.03. [Online]. Available: http://www.globaltcad.com/